74HC574D-HX/74HC574N-HX OCTAL EDGE-TRIGGERED D-TYPE FLIP-FLOPS WITH 3-STATE OUTPUTS

Description

The 74HC574D-HX/74HC574N-HX is an octal, edge-triggered D-type flip-flop with three-state outputs, featuring eight independent channels.

Features

★ Operate from 2V to 6V

★ Max tpd of 66ns at 4.5 V

★ Typical V_{OL}< 0.17V at V_{CC}=4.5V, T_A=25°C

★ Typical V_{OH}> 4.3V at V_{CC}=4.5V, T_A=25°C

★ Latch-up performance ≤ 250 mA

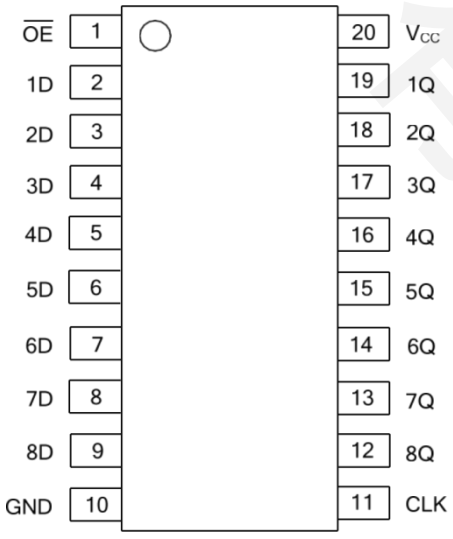
★ ESD protection:

- HBM: ANSI/ESDA/JEDEC JS-001 2023 exceeds 2000 V
- CDM: ANSI/ESDA/JEDEC JS-002 2022 exceeds 1000 V

★ Package Option:74HC574D-HX SOIC-20

74HC574N-HX DIP-20

Pin Configuration

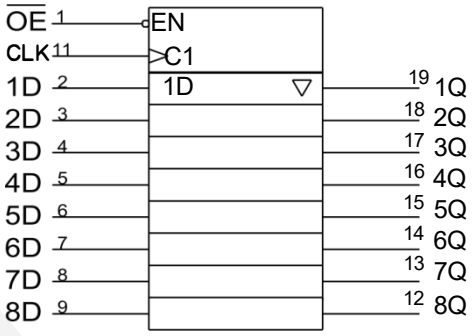


Function Table

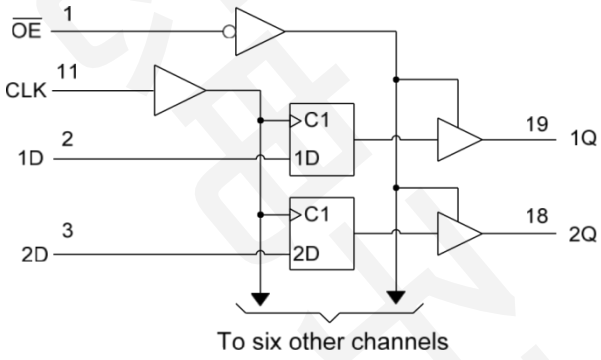
INPUTS(OE)	INPUTS(CLK)	INPUTS(D)	OUTPUT(Q)
L	↑	H	H
L	↑	L	L
L	L /H	X	Q0
H	X	X	Z

Note: H: HIGH voltage level; L: LOW voltage level.

Logic Symbol



Logic Diagram



Absolute Maximum Ratings (T_A=25°C, unless otherwise specified)

PARAMETER	SYMBOL	RATINGS	UNIT
Supply Voltage	V_{CC}	-0.5 ~ +7	V
VCC or GND Current	I_{CC}	±70	mA
Output Current	I_{OUT}	±35	mA
Input Clamp Current	I_{IK}	±20	mA
Output Clamp Current	I_{OK}	±20	mA
Storage Temperature	T_{STG}	-65 ~ + 150	°C

Note: Absolute maximum ratings are those values beyond which the device could be permanently damaged. Absolute maximum ratings are stress ratings only and functional device operation is not implied.

Recommended Operating Conditions

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Supply Voltage	V_{CC}	-	2	5	6	V
Input Voltage	V_{IN}	-	0	-	V_{CC}	V
Output Voltage	V_{OUT}	High or low state	0	-	V_{CC}	V
Input Rise or Fall Times	t_R, t_F	V_{CC}=2.0V	0	-	1	μs
		V_{CC}=4.5V	0	-	0.5	μs
		V_{CC}=6.0V	0	-	0.4	μs
Operating Temperature	T_A	-	-40	-	+125	°C

Thermal Data

PARAMETER		SYMBOL	RATINGS	UNIT
Junction to Ambient	DIP-20	θ_{JA}	52	°C/W
	SOIC-20		80	°C/W

Electrical Characteristics

PARAMETER	SYMBOL	TEST CONDITIONS	T_A=25°C			T_A=-40~+125°C			UNIT
			MIN	TYP	MAX	MIN	TYP	MAX	
High-level Input Voltage	V_{IH}	V_{CC}=2.0V	1.5	-		1.5	-	-	V
		V_{CC}=4.5V	3.15	-		3.15	-	-	V
		V_{CC}=6.0V	4.2	-		4.2	-	-	V
Low-level Input Voltage	V_{IL}	V_{CC}=2.0V	-	-	0.5	-	-	0.5	V
		V_{CC}=4.5V	-	-	1.35	-	-	1.35	V
		V_{CC}=6.0V	-	-	1.8	-	-	1.8	V
Output Voltage High- Level	V_{OH}	V_{CC}=2.0V, I_{OH}=-20μA	1.9	1.99	-	1.9	-	-	V
		V_{CC}=4.5V, I_{OH}=-20μA	4.4	4.49	-	4.4	-	-	V
		V_{CC}=6.0V, I_{OH}=-20μA	5.9	5.99	-	5.9	-	-	V
		V_{CC}=4.5V, I_{OH}=-6mA	3.98	4.32	-	3.7	-	-	V
		V_{CC}=6.0V, I_{OH}=-7.8mA	5.48	5.81	-	5.2	-	-	V
Output Voltage Low-Level	V_{OL}	V_{CC}=2.0V, I_{OL}=20μA	-	0.002	0.1	-	-	0.1	V
		V_{CC}=4.5V, I_{OL}=20μA	-	0.001	0.1	-	-	0.1	V
		V_{CC}=6.0V, I_{OL}=20μA	-	0.001	0.1	-	-	0.1	V
		V_{CC}=4.5V, I_{OL}=6mA	-	0.15	0.26	-	-	0.4	V
		V_{CC}=6.0V, I_{OL}=7.8mA	-	0.16	0.26	-	-	0.4	V
Input Leakage Current	$I_{I(LEAK)}$	V_{CC}=6.0V, V_{IN}=V_{CC} or GND	-	±0.1	±100	-	-	±1000	nA
Disable Output Leakage Current	I_{OZ}	V_{CC}=6.0V, V_{OUT}=V_{CC} or GND	-	±0.01	±1.0	-	-	±10	μA
Quiescent Supply Current	I_Q	V_{CC}=6.0V, V_{IN}=V_{CC} or GND, I_{OUT}=0	-	-	8	-	-	160	μA

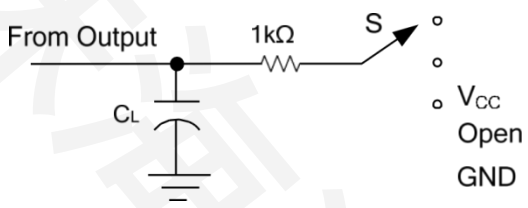
Switching Characteristics

PARAMETER	SYMBOL	TEST CONDITIONS	T_A=25°C			T_A=-40~+125°C			UNIT
			MIN	TYP	MAX	MIN	TYP	MAX	
Propagation delay from input (CLK) to output (Q)	t_{PLH}/t_{PHL}	V_{CC}=2.0V, C_L=50pF	-	47	180	-	-	225	ns
		V_{CC}=4.5V, C_L=50pF	-	17	36	-	-	45	ns
		V_{CC}=6.0V, C_L=50pF	-	14	31	-	-	38	ns
		V_{CC}=2.0V, C_L=150pF	-	105	265	-	-	330	ns
		V_{CC}=4.5V, C_L=150pF	-	36	53	-	-	66	ns
		V_{CC}=6.0V, C_L=150pF	-	31	46	-	-	57	ns
Output enable time from input (OE) to output (Q)	t_{PZL}/t_{PZH}	V_{CC}=2.0V, C_L=50pF	-	44	150	-	-	210	ns
		V_{CC}=4.5V, C_L=50pF	-	16	30	-	-	42	ns
		V_{CC}=6.0V, C_L=50pF	-	13	26	-	-	36	ns
		V_{CC}=2.0V, C_L=150pF	-	95	235	-	-	315	ns
		V_{CC}=4.5V, C_L=150pF	-	32	47	-	-	63	ns
		V_{CC}=6.0V, C_L=150pF	-	28	41	-	-	55	ns
Output disable time from input (OE) to output (Q)	t_{PLZ}/t_{PHZ}	V_{CC}=2.0V, C_L=50pF	-	39	150	-	-	190	ns
		V_{CC}=4.5V, C_L=50pF	-	14	30	-	-	38	ns
		V_{CC}=6.0V, C_L=50pF	-	11	26	-	-	32	ns
Maximum Clock Frequency	f_{MAX}	V_{CC}=2.0V, C_L=50pF	6	11	-	4	-	-	MHz
		V_{CC}=4.5V, C_L=50pF	30	36	-	20	-	-	MHz
		V_{CC}=6.0V, C_L=50pF	36	40	-	24	-	-	MHz
		V_{CC}=2.0V, C_L=150pF	6	-	-	4	-	-	MHz
		V_{CC}=4.5V, C_L=150pF	30	-	-	20	-	-	MHz
		V_{CC}=6.0V, C_L=150pF	36	-	-	24	-	-	MHz
Clock Frequency	f_{CLOCK}	V_{CC}=2.0V	-	-	6	-	-	4	MHz
		V_{CC}=4.5V	-	-	30	-	-	20	MHz
		V_{CC}=6.0V	-	-	38	-	-	24	MHz
Pulse Width	t_W	V_{CC}=2.0V	80	-	-	120	-	-	ns
		V_{CC}=4.5V	16	-	-	24	-	-	ns
		V_{CC}=6.0V	14	-	-	20	-	-	ns
Setup Time	t_{SU}	V_{CC}=2.0V	100	-	-	125	-	-	ns
		V_{CC}=4.5V	20	-	-	25	-	-	ns
		V_{CC}=6.0V	17	-	-	21	-	-	ns
Hold Time	t_H	V_{CC}=2.0V	5	-	-	5		-	ns
		V_{CC}=4.5V	5	-	-	5		-	ns
		V_{CC}=6.0V	5	-	-	5		-	ns

Operating Characteristics

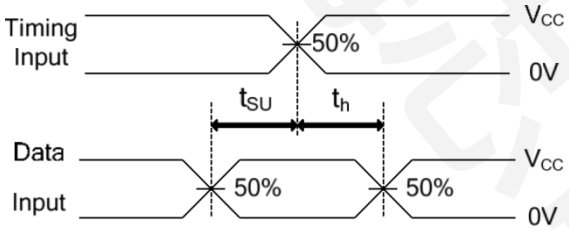
PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Input Capacitance	C_{IN}	V_{CC}=2.0V~ 6.0V	-	3	10	pF
Power Dissipation Capacitance	C_{PD}	No Load	-	100	-	pF

Test Circuit and Waveforms

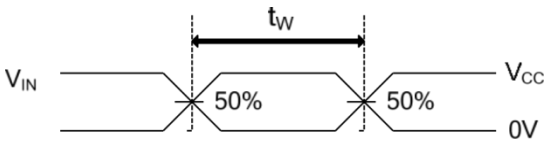


	S
t_{PLH}/t_{PHL}	Open
t_{PHZ}/t_{PZH}	GND
tpLZ/tpzL	VCC

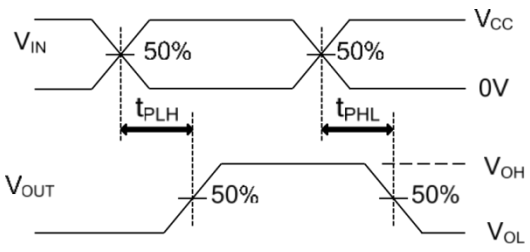
TEST CIRCUIT



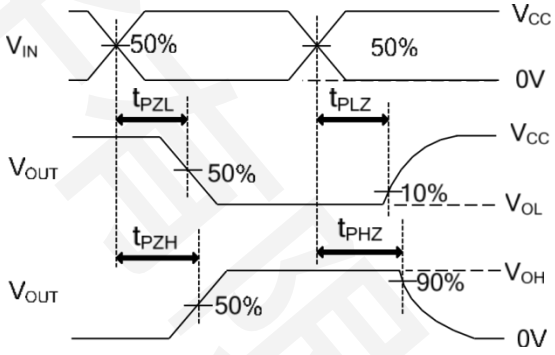
SETUP TIME AND HOLD TIME



PULSE WIDTH



PROPAGATION DELAY TIMES

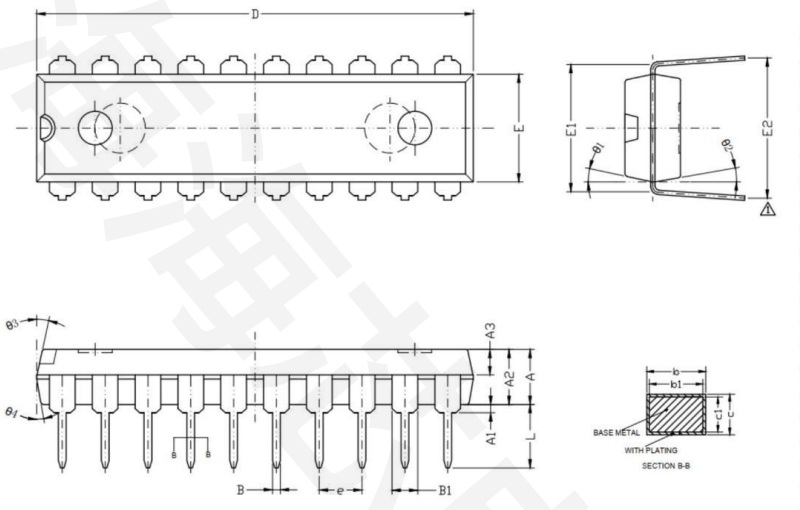


ENABLE AND DISABLE TIMES

Note: C_L includes probe and jig capacitance. PRR≤1MHz, Zo=50Ω, t_R ≤6ns, t_F ≤6ns.

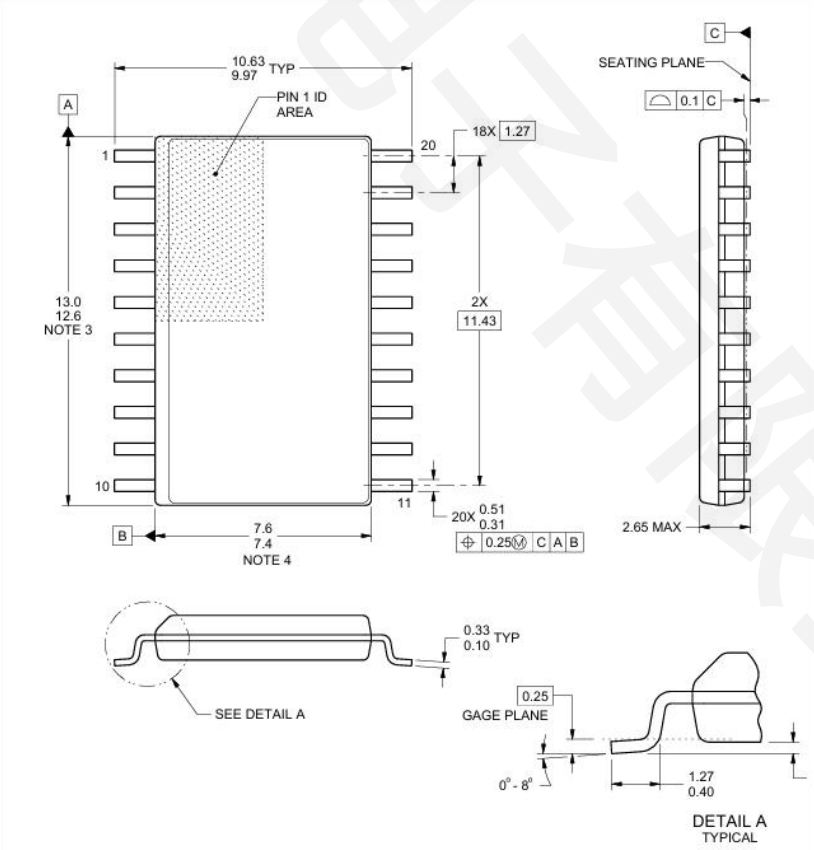
Package Information

74HC574N-HX DIP 20 package information



SYMBOL	MILLIMETER		
	MIN	MIN	MAX
A	3.60	3.80	4.00
A1	0.51	--	--
A2	3.20	3.30	3.40
A3	1.47	1.52	1.57
B	0.44	--	0.53
B1	1.52(BSC)		
b	0.44	--	0.53
b1	0.43	0.46	0.48
c	0.25	--	0.31
c1	0.24	0.25	0.26
D	25.7	25.9	26.1
E	6.35	6.55	6.75
E1	7.62(BSC)		
E2	8.00	8.40	8.80
e	2.54(BSC)		
L	3.00	--	3.60
θ1	8°	~	14°
θ2	6°	~	12°
θ3	8°	~	14°
θ4	6°	~	12°

74HC574D-HX SOIC 20 package information



NOTES:

1. All linear dimensions are in millimeters. Dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.43 mm per side.
5. Reference JEDEC registration MS-013.