

## 74HC273D-HX/74HC273D-HX OCTAL D-TYPE FLIP-FLOPS WITH CLEAR

### DESCRIPTION

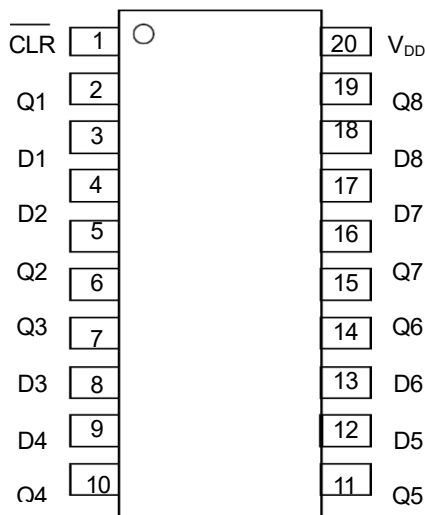
The 74HC273D-HX/74HC273D-HX devices are positive-edge-triggered D-type flip-flops with a direct active low clear (CLR) input.

Information at the data (D) inputs meeting the setup time requirements is transferred to the Q outputs on the positive-going edge of the clock (CLK) pulse. Clock triggering occurs at a particular voltage level and is not related directly to the transition time of the positive-going pulse. When CLK is at either the high or low level, the D input has no effect at the output.

### FEATURES

- ★ Wide Operating Voltage Range of 2V to 6V
- ★ Low Power Consumption, 80- $\mu$ A Maximum ICC
- ★ Typical  $t_{PD} = 12$ ns
- ★  $\pm 4$ mA Output Drive at 5V
- ★ Low Input Current of 1 $\mu$ A Maximum
- ★ Contain Eight Flip-Flops With Single-Rail Outputs
- ★ Direct Clear Input
- ★ Individual Data Input to Each Flip-Flop
- ★ Latch-up performance  $\leq 250$  mA
- ★ ESD protection:
  - HBM: ANSI/ESDA/JEDEC JS-001 2023 exceeds 2000 V
  - CDM: ANSI/ESDA/JEDEC JS-002 2022 exceeds 1500 V
- ★ Package Option: DIP-20 and SOP-20

### PIN CONFIGURATION





**ABSOLUTE MAXIMUM RATING** ( $T_A=25^{\circ}\text{C}$ , unless otherwise specified)

PARAMETER	SYMBOL	CONDITIONS	RATINGS	UNIT
Supply Voltage	$V_{CC}$	-	-0.5 ~ 7.0	V
$V_{CC}$ or GND Current	$I_{CC}$	-	$\pm 50$	mA
Continuous Output Current	$I_{OUT}$	$V_{OUT}=0 \sim V_{CC}$	$\pm 25$	mA
Input Clamp Current	$I_{IK}$	$V_{IN}<0$ or $V_{IN}<V_{CC}$	$\pm 20$	mA
Output Clamp Current	$I_{OK}$	$V_{IN}<0$ or $V_{OUT}>V_{CC}$	$\pm 20$	mA
Storage Temperature Range	$T_{STG}$	-	-65 ~ +150	$^{\circ}\text{C}$

Note: Absolute maximum ratings are those values beyond which the device could be permanently damaged.

Absolute maximum ratings are stress ratings only and functional device operation is not implied.

**RECOMMENDED OPERATING CONDITIONS**

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNIT
Supply Voltage	$V_{CC}$	-	2	5	6	V
High-Level Input Voltage	$V_{IH}$	$V_{CC}=2\text{V}$	1.5	-	-	V
		$V_{CC}=4.5\text{V}$	3.15	-	-	V
		$V_{CC}=6\text{V}$	4.2	-	-	V
Low-Level Input Voltage	$V_{IL}$	$V_{CC}=2\text{V}$	-	-	0.5	V
		$V_{CC}=4.5\text{V}$	-	-	1.35	V
		$V_{CC}=6\text{V}$	-	-	1.8	V
Input Voltage	$V_{IN}$	-	0	-	$V_{CC}$	V
Output Voltage	$V_{OUT}$	-	0	-	$V_{CC}$	V
Input Transition Rise or Fall Rate	$t_r, t_f$	$V_{CC}=2\text{V}$	-	-	1000	ns
		$V_{CC}=4.5\text{V}$	-	-	500	ns
		$V_{CC}=6\text{V}$	-	-	400	ns
Operating Temperature	$T_A$	-	-40	-	+125	$^{\circ}\text{C}$

**ELECTRICAL CHARACTERISTICS** ( $T_A=25^{\circ}\text{C}$ , unless otherwise specified)

PARAMETER	SYMBOL	TEST CONDITIONS	$T_A=25^{\circ}\text{C}$			$T_A=-40\sim+125^{\circ}\text{C}$			UNIT
			MIN	TYP	MAX	MIN	TYP	MAX	
High-Level Output Voltage	$V_{OH}$	$V_{CC}=2\text{V}, I_{OH}=-20\mu\text{A}$	1.9	1.998	-	1.9	-	-	V
		$V_{CC}=4.5\text{V}, I_{OH}=-20\mu\text{A}$	4.4	4.499	-	4.4	-	-	V
		$V_{CC}=6\text{V}, I_{OH}=-20\mu\text{A}$	5.9	5.999	-	5.9	-	-	V
		$V_{CC}=4.5\text{V}, I_{OH}=-4\text{mA}$	3.98	4.32	-	3.7	-	-	V
		$V_{CC}=6\text{V}, I_{OH}=-5.2\text{mA}$	5.48	5.81	-	5.2	-	-	V
Low-Level Output Voltage	$V_{OL}$	$V_{CC}=2\text{V}, I_{OL}=20\mu\text{A}$	-	0.002	0.1	-	-	0.1	V
		$V_{CC}=4.5\text{V}, I_{OL}=20\mu\text{A}$	-	0.003	0.1	-	-	0.1	V
		$V_{CC}=6\text{V}, I_{OL}=20\mu\text{A}$	-	0.003	0.1	-	-	0.1	V
		$V_{CC}=4.5\text{V}, I_{OL}=4\text{mA}$	-	0.15	0.26	-	-	0.4	V
		$V_{CC}=6\text{V}, I_{OL}=5.2\text{mA}$	-	0.16	0.26	-	-	0.4	V
Input Leakage Current	$I_{I(LEAK)}$	$V_{CC}=6\text{V}, V_I=V_{CC}$ or 0	-	$\pm 0.1$	$\pm 100$	-	-	$\pm 100$	$\mu\text{A}$
Quiescent Supply Current	$I_{CC}$	$V_{CC}=6\text{V}, V_I=V_{CC}$ or 0, $I_{OUT}=0$	-	-	8	-	-	160	$\mu\text{A}$

## SWITCHING CHARACTERISTICS (C<sub>L</sub>=50pF, unless otherwise specified)

PARAMETER	SYMBOL	TEST CONDITIONS	T <sub>A</sub> =25°C			T <sub>A</sub> =-40~+125°C			UNIT
			MIN	TYP	MAX	MIN	TYP	MAX	
Maximum clock pulse frequency	f <sub>MAX</sub>	V <sub>CC</sub> =2.0V	5	11	-	4	-	-	MHz
		V <sub>CC</sub> =4.5V	27	50	-	20	-	-	MHz
		V <sub>CC</sub> =6.0V	32	60	-	24	-	-	MHz
Propagation delay from input ( CLR ) to output (Any)	t <sub>PHL</sub>	V <sub>CC</sub> =2.0V	-	41	160	-	-	225	ns
		V <sub>CC</sub> =4.5V	-	15	32	-	-	45	ns
		V <sub>CC</sub> =6.0V	-	12	27	-	-	38	ns
Propagation delay from input (CLK) to output (Any)	t <sub>PD</sub>	V <sub>CC</sub> =2.0V	-	44	160	-	-	225	ns
		V <sub>CC</sub> =4.5V	-	15	32	-	-	45	ns
		V <sub>CC</sub> =6.0V	-	13	27	-	-	38	ns
Propagation delay to output (Any)	t <sub>t</sub>	V <sub>CC</sub> =2.0V	-	19	75	-	-	110	ns
		V <sub>CC</sub> =4.5V	-	7	15	-	-	22	ns
		V <sub>CC</sub> =6.0V	-	6	13	-	-	19	ns

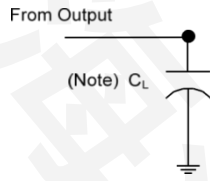
## TIMING REQUIREMENTS (Input: t<sub>r</sub>, t<sub>f</sub>≤2.5ns; P<sub>RR</sub>≤1MHz)

PARAMETER	SYMBOL	Conditions	T <sub>A</sub> =25°C			T <sub>A</sub> =-40~+125°C			UNIT
			MIN	TYP	MAX	MIN	TYP	MAX	
Clock frequency	f <sub>CLOCK</sub>	V <sub>CC</sub> = 2V	-	-	5	-	-	4	MHz
		V <sub>CC</sub> =4.5V	-	-	27	-	-	20	MHz
		V <sub>CC</sub> =6V	-	-	32	-	-	24	MHz
Pulse duration	CLK high or low	V <sub>CC</sub> = 2V	-	80	-	120	-	-	ns
		V <sub>CC</sub> =4.5V	-	16	-	24	-	-	ns
		V <sub>CC</sub> =6V	-	14	-	20	-	-	ns
	CLR low	V <sub>CC</sub> = 2V	-	80	-	120	-	-	ns
		V <sub>CC</sub> =4.5V	-	16	-	24	-	-	ns
		V <sub>CC</sub> =6V	-	14	-	20	-	-	ns
Setup time before CLK↑	Data	V <sub>CC</sub> = 2V	-	100	-	120	-	-	ns
		V <sub>CC</sub> =4.5V	-	20	-	24	-	-	ns
		V <sub>CC</sub> =6V	-	17	-	20	-	-	ns
	CLR inactive	V <sub>CC</sub> = 2V	-	100	-	120	-	-	ns
		V <sub>CC</sub> =4.5V	-	20	-	24	-	-	ns
		V <sub>CC</sub> =6V	-	17	-	20	-	-	ns
Hold time after CLK↑, data	t <sub>H</sub>	V <sub>CC</sub> = 2V	-	0	-	-6	-	-	ns
		V <sub>CC</sub> =4.5V	-	0	-	-2	-	-	ns
		V <sub>CC</sub> =6V	-	0	-	-2	-	-	ns

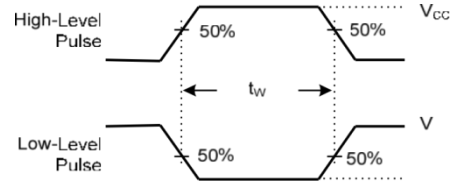
## OPERATING CHARACTERISTICS (T<sub>A</sub>=25°C, unless otherwise specified)

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Input Capacitance	C <sub>I</sub>	V <sub>CC</sub> =2V~6V	-	3	10	pF
Power Dissipation Capacitance per flip-flop	C <sub>PD</sub>	No load.	-	35	-	pF

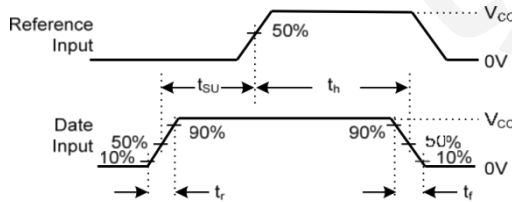
## TEST CIRCUIT AND WAVEFORMS



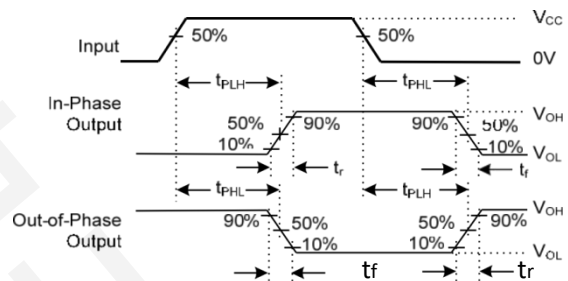
Load circuit



voltage waveforms pulse Durations



voltage waveforms setup and Hold Times



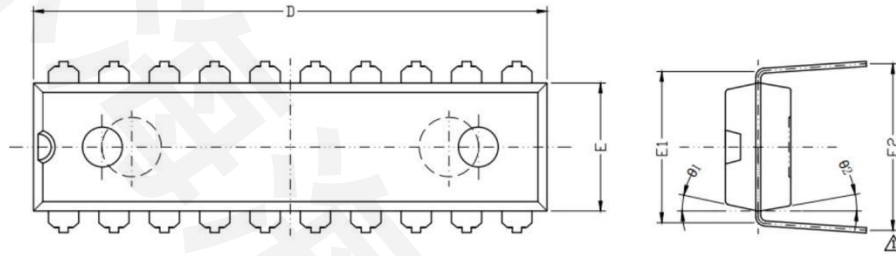
Voltage Waveforms Propagation Delay and Output Transition Times

Notes:

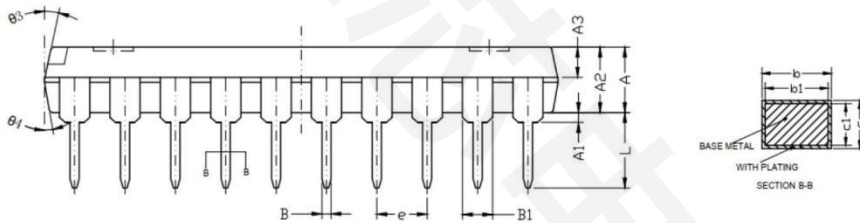
1.  $C_L$  includes probe and jig capacitance.
2. All input pulses are supplied by generators having the following characteristics:  $PRR \leq 1MHz$ ,  $Z_o = 50\Omega$ ,  $t_r = 6ns$ ,  $t_f = 6ns$ .
3. For clock inputs,  $f_{max}$  is measured when the input duty cycle is 50%.
4. The outputs are measured one at a time with one input transition per measurement.

## PACKAGE INFORMATION

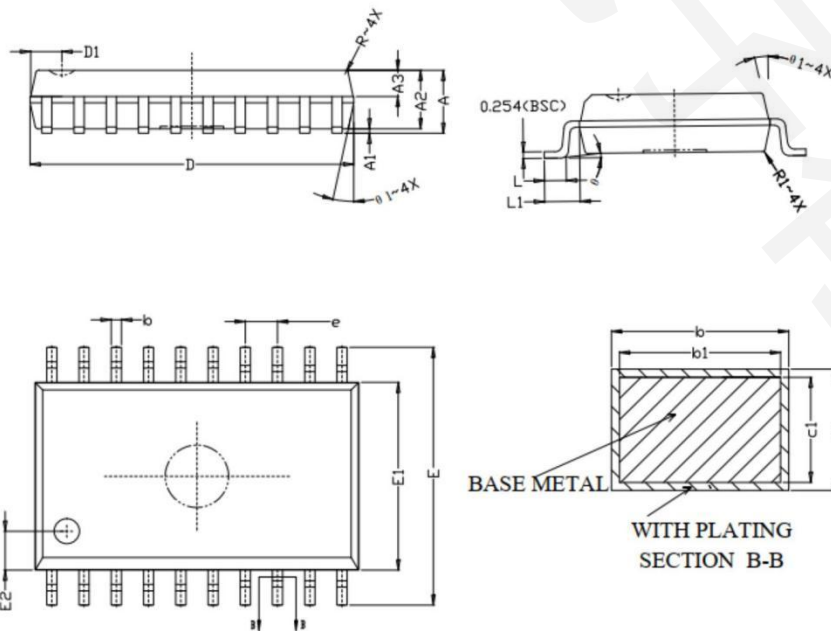
### 74HC273N-HX DIP 20 package information



SYMBOL	MILLIMETER		
	MIN	MIN	MAX
A	3.60	3.80	4.00
A1	0.51	--	--
A2	3.20	3.30	3.40
A3	1.47	1.52	1.57
B	0.44	--	0.53
B1	1.52(BSC)		
b	0.44	--	0.53
b1	0.43	0.46	0.48
c	0.25	--	0.31
c1	0.24	0.25	0.26
D	25.7	25.9	26.1
E	6.35	6.55	6.75
E1	7.62(BSC)		
E2	8.00	8.40	8.80
e	2.54(BSC)		
L	3.00	--	3.60
theta1	8°	~	14°
theta2	6°	~	12°
theta3	8°	~	14°
theta4	6°	~	12°



### 74HC273D-HX SOP 20 package information



SYMBOL	MILLIMETER		
	MIN	MIN	MAX
A	--	--	2.615
A1	0.10	--	0.30
A2	2.29	2.34	2.39
A3	0.99	1.043	1.07
b	0.39	--	0.47
b1	0.38	0.41	0.44
c	0.25	--	0.29
c1	0.24	0.25	0.26
D	12.65	12.75	12.85
D1	1.225(BSC)		
E	10.10	10.30	10.50
E1	7.40	7.50	7.60
E2	1.55(BSC)		
e	1.27(BSC)		
L	0.854	0.864	0.874
L1	1.403(REF)		
theta	0°	~	8°
theta1	6°	~	15°
R/R1	R1.27(BSC)		