

Description:

This N+P Channel MOSFET uses advanced trench technology and design to provide excellent $R_{DS(on)}$ with low gate charge.

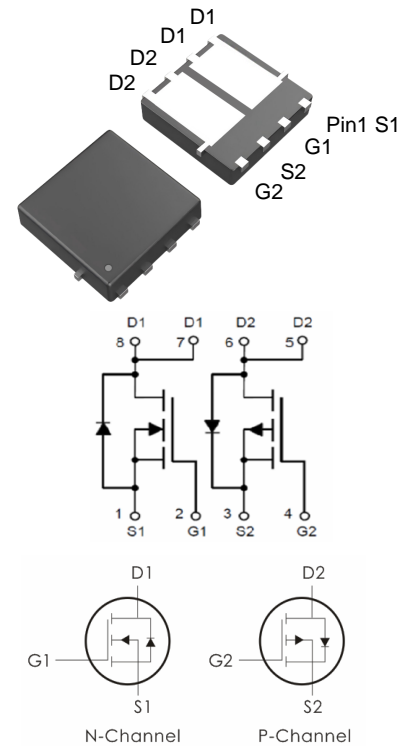
It can be used in a wide variety of applications.

Features:

N-Channel: $V_{DS}=30V, I_D=25A, R_{DS(on)} < 13m\Omega @ V_{GS}=10V$ (Typ: $10m\Omega$)

P-Channel: $V_{DS}=-30V, I_D=-20A, R_{DS(on)} < 26m\Omega @ V_{GS}=-10V$ (Typ: $20m\Omega$)

- 1) Low gate charge.
- 2) Green device available.
- 3) Advanced high cell density trench technology for ultra low $R_{DS(on)}$.
- 4) Excellent package for good heat dissipation.
- 5) MSL3



Package Marking and Ordering Information:

Part NO.	Marking	Package	Packing
DOZ4606C	Z4606C	DFN3*3-8D	5000 pcs/Reel

Absolute Maximum Ratings: ($T_C=25^\circ C$ unless otherwise noted)

Symbol	Parameter	N-Channel	P-Channel	Units
V_{DS}	Drain-Source Voltage	30	-30	V
V_{GS}	Gate-Source Voltage	± 20	± 20	V
I_D	Continuous Drain Current- $T_C=25^\circ C$ ¹	25	-20	A
	Continuous Drain Current- $T_C=100^\circ C$ ¹	17.5	-14	
I_{DM}	Pulsed Drain Current ²	100	-80	A
E_{AS}	Single pulse avalanche energy ³	49	45	mJ
P_D	Power Dissipation - $T_C=25^\circ C$	17.9	17	W
T_J, T_{STG}	Operating and Storage Junction Temperature Range	-55 to +150		$^\circ C$

Thermal Characteristics:

Symbol	Parameter	N-CH	P-CH	Units
$R_{\theta JC}$	Thermal Resistance, Junction to Case	7	7.2	$^\circ C/W$

N-Channel Electrical Characteristics: ($T_C=25^\circ\text{C}$ unless otherwise noted)

Symbol	Parameter	Conditions	Min	Typ	Max	Units
Off Characteristics						
BV_{DSS}	Drain-Source Breakdown Voltage	$V_{GS}=0V, I_D=250\ \mu\text{A}$	30	---	---	V
I_{DSS}	Zero Gate Voltage Drain Current	$V_{GS}=0V, V_{DS}=30V$	---	---	1	μA
I_{GSS}	Gate-Source Leakage Current	$V_{GS}=\pm 20V, V_{DS}=0A$	---	---	± 100	nA
On Characteristics						
$V_{GS(th)}$	Gate-Source Threshold Voltage	$V_{GS}=V_{DS}, I_D=250\ \mu\text{A}$	1	1.5	2.5	V
$R_{DS(on)}$	Drain-Source On Resistance ⁴	$V_{GS}=10V, I_D=10A$	---	10	13	$\text{m}\Omega$
		$V_{GS}=4.5V, I_D=5A$	---	16.5	21	
Dynamic Characteristics						
C_{iss}	Input Capacitance	$V_{DS}=15V, V_{GS}=0V, f=1\text{MHz}$	---	870	---	pF
C_{oss}	Output Capacitance		---	118	---	
C_{rss}	Reverse Transfer Capacitance		---	98.7	---	
Switching Characteristics⁴						
$t_{d(on)}$	Turn-On Delay Time	$V_{DS}=15V, I_D=20A,$ $R_{REN}=10\ \Omega, V_{GS}=10V$	---	9	---	ns
t_r	Rise Time		---	14.7	---	ns
$t_{d(off)}$	Turn-Off Delay Time		---	37.8	---	ns
t_f	Fall Time		---	16.8	---	ns
Q_g	Total Gate Charge		$V_{GS}=4.5V, V_{DS}=24V,$ $I_D=10A$	---	18	---
Q_{gs}	Gate-Source Charge	---		5	---	nC
Q_{gd}	Gate-Drain "Miller" Charge	---		4	---	nC
Drain-Source Diode Characteristics						
I_S	Continuous Drain to Source Diode	$V_D=V_G=0V$	---	---	20.8	A
I_{SM}	Pulsed Drain to Source Diode		---	---	83.3	A
V_{SD}	Source-Drain Diode Forward Voltage	$V_{GS}=0V, I_S=20A$	---	---	1.2	V
T_{rr}	Reverse Recovery Time	$I_f=3A, T_J=25^\circ\text{C}$	---	16	---	ns
Q_{rr}	Reverse Recovery Charge	$di/dt=100A/\mu\text{s}$	---	10	---	nC

Notes:

1. Computed continuous current assumes the condition of $T_{j,Max}$ while the actual continuous current depends on the thermal & electro-mechanical application board design
2. Repetitive Rating: Pulse Width Limited by Maximum Junction Temperature
3. EAS condition : $T_J=25^{\circ}C, V_{DD}=15V, V_G=10V, L=0.5mH$
4. Pulse Test: Pulse Width $\leq 300\mu s$, Duty Cycle $\leq 0.5\%$

Test Circuit

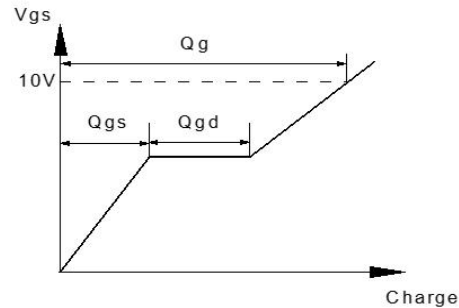
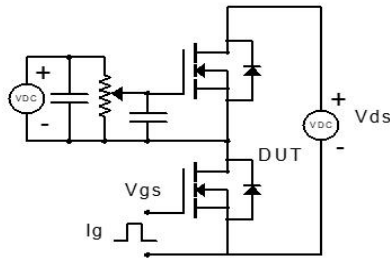


Figure 1: Gate Charge Test Circuit & Waveform

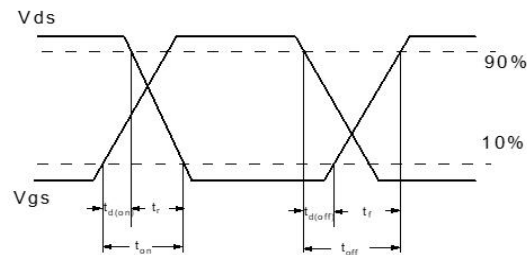
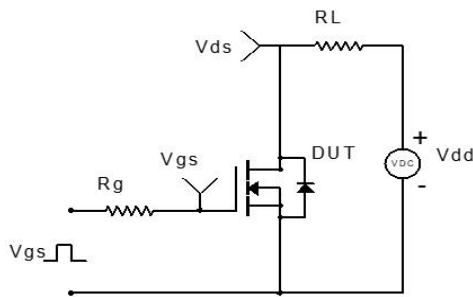


Figure 2: Resistive Switching Test Circuit & Waveform

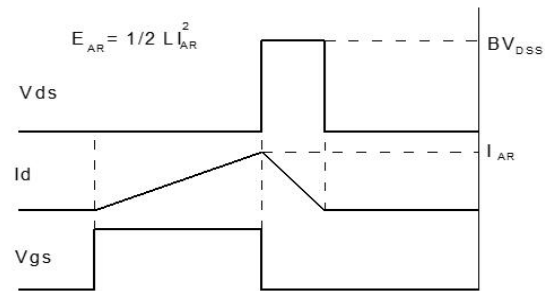
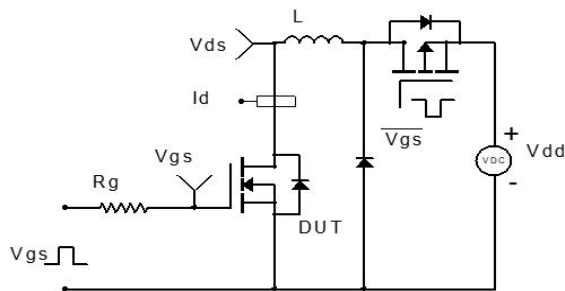


Figure 3: Unclamped Inductive Switching Test Circuit & Waveform

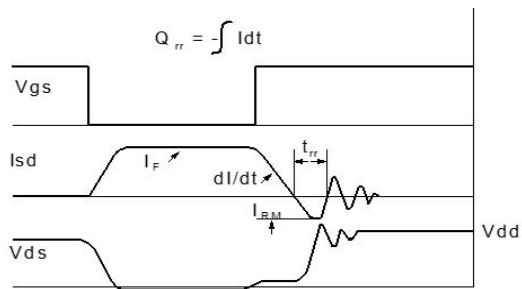
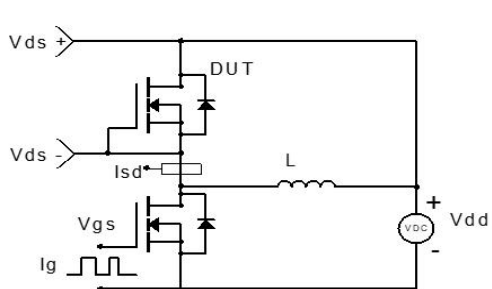


Figure 4: Diode Recovery Test Circuit & Waveform

P-Channel Electrical Characteristics: ($T_A=25^\circ\text{C}$ unless otherwise noted)

Symbol	Parameter	Conditions	Min	Typ	Max	Units
Off Characteristics						
BV_{DSS}	Drain-Source Breakdown Voltage	$V_{GS}=0V, I_D=250\ \mu\text{A}$	-30	---	---	V
I_{DSS}	Zero Gate Voltage Drain Current	$V_{GS}=0V, V_{DS}=-30V$	---	---	-1	μA
I_{GSS}	Gate-Source Leakage Current	$V_{GS}=\pm 20V, V_{DS}=0A$	---	---	± 100	nA
On Characteristics						
$V_{GS(th)}$	Gate-Source Threshold Voltage	$V_{GS}=V_{DS}, I_D=250\ \mu\text{A}$	-1	-1.6	-2.5	V
$R_{DS(on)}$	Drain-Source On Resistance ⁴	$V_{GS}=-10V, I_D=-10A$	---	20	26	m Ω
		$V_{GS}=-4.5V, I_D=-5A$	---	30	40	
Dynamic Characteristics						
C_{iss}	Input Capacitance	$V_{DS}=-15V, V_{GS}=0V, f=1\text{MHz}$	---	670	---	pF
C_{oss}	Output Capacitance		---	121	---	
C_{rss}	Reverse Transfer Capacitance		---	99	---	
Switching Characteristics						
$t_{d(on)}$	Turn-On Delay Time	$V_{DD}=-15V, I_D=-6A$ $V_{GS}=-10V, R_{GEN}=6\ \Omega$	---	13	---	ns
t_r	Rise Time		---	15.7	---	ns
$t_{d(off)}$	Turn-Off Delay Time		---	207	---	ns
t_f	Fall Time		---	102	---	ns
Q_g	Total Gate Charge		---	51	---	nC
Q_{gs}	Gate-Source Charge	$V_{GS}=-10V, V_{DS}=-15V,$ $I_D=-6A$	---	9.8	---	nC
Q_{gd}	Gate-Drain "Miller" Charge		---	8.6	---	nC
Drain-Source Diode Characteristics						
I_S	Continuous Drain to Source Diode	$V_D=V_G=0V$	---	---	-16.6	A
I_{SM}	Pulsed Drain to Source Diode		---	---	-66.6	---
T_{rr}	Reverse Recovery Time	$I_F=-2A, T_J=25^\circ\text{C}$	---	37	---	ns
Q_{rr}	Reverse Recovery Charge	$dI/dt=100A/\mu\text{s}$	---	36	---	nC
V_{SD}	Source-Drain Diode Forward Voltage	$V_{GS}=0V, I_S=-5A$	---	---	-1.2	V

Notes:

1. Computed continuous current assumes the condition of $T_{j,Max}$ while the actual continuous current depends on the thermal & electro-mechanical application board design
2. Repetitive Rating: Pulse Width Limited by Maximum Junction Temperature
3. EAS condition : $T_J=25^{\circ}C, V_{DD}=-15V, V_G=-10V, L=0.5mH$
4. Pulse Test: Pulse Width $\leq 300\mu s$, Duty Cycle $\leq 0.5\%$

Test Circuit

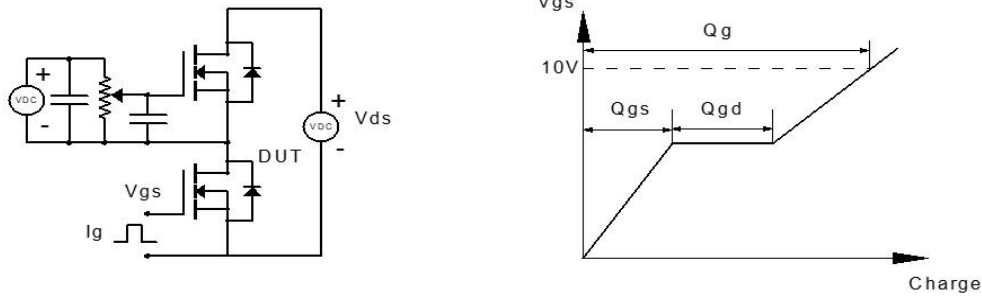


Figure 1: Gate Charge Test Circuit & Waveform

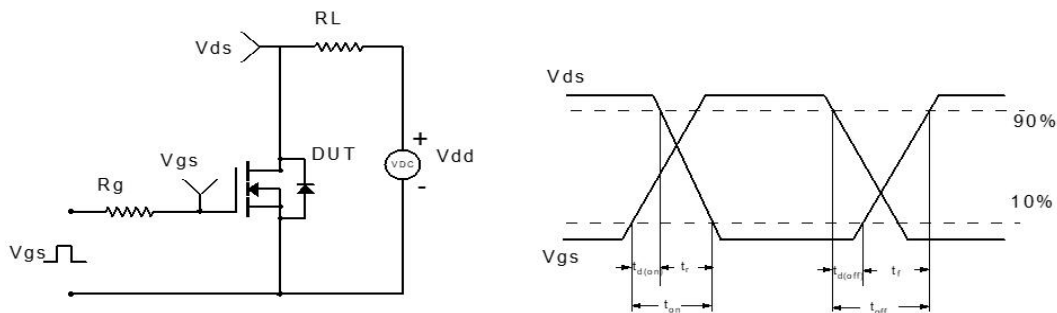


Figure 2: Resistive Switching Test Circuit & Waveform

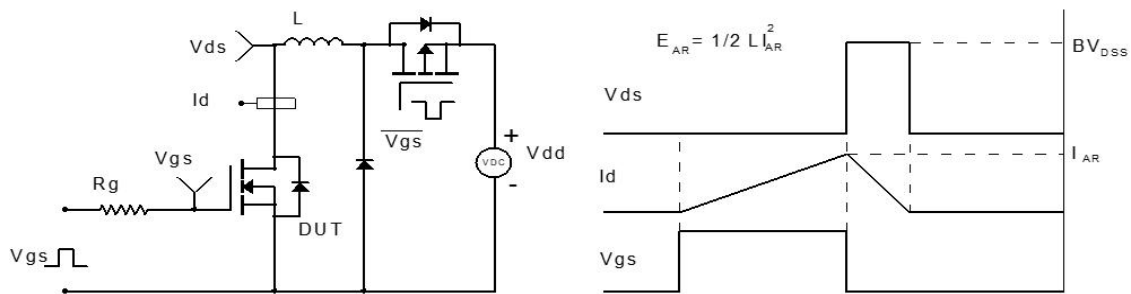


Figure 3: Unclamped Inductive Switching Test Circuit & Waveform

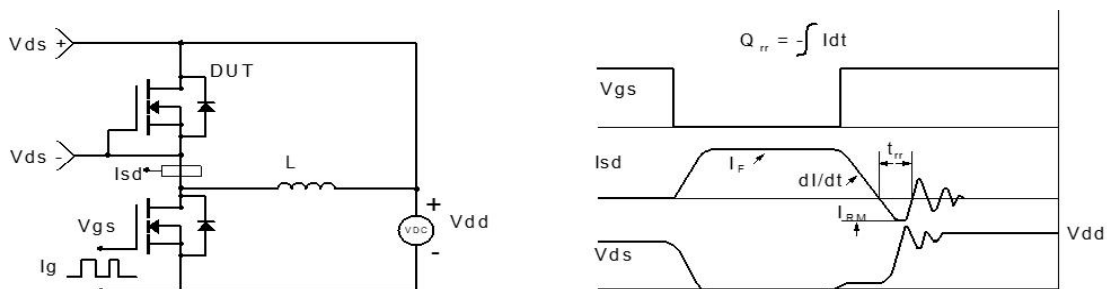
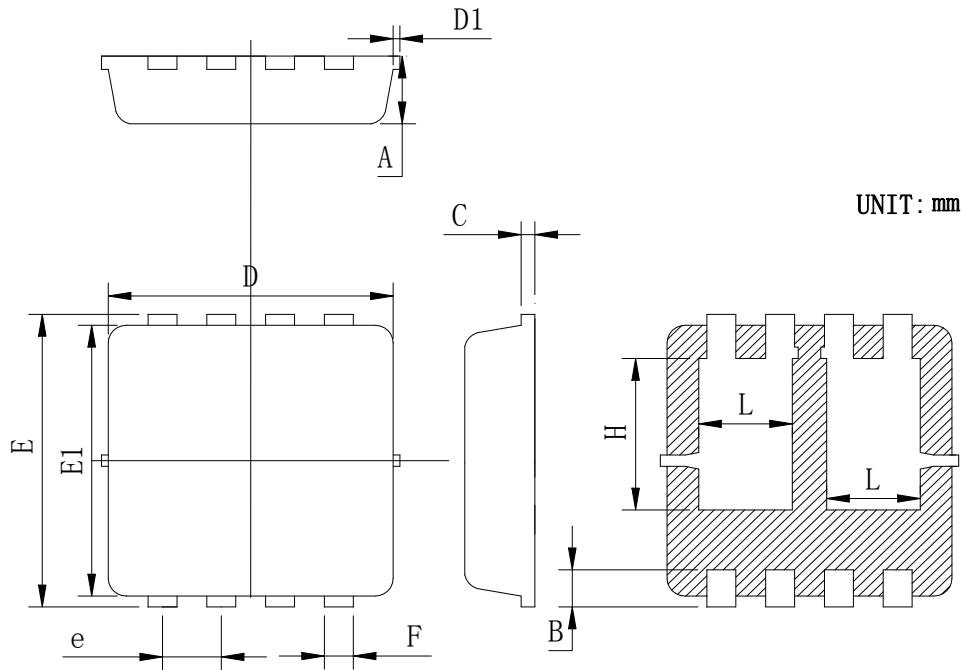


Figure 4: Diode Recovery Test Circuit & Waveform

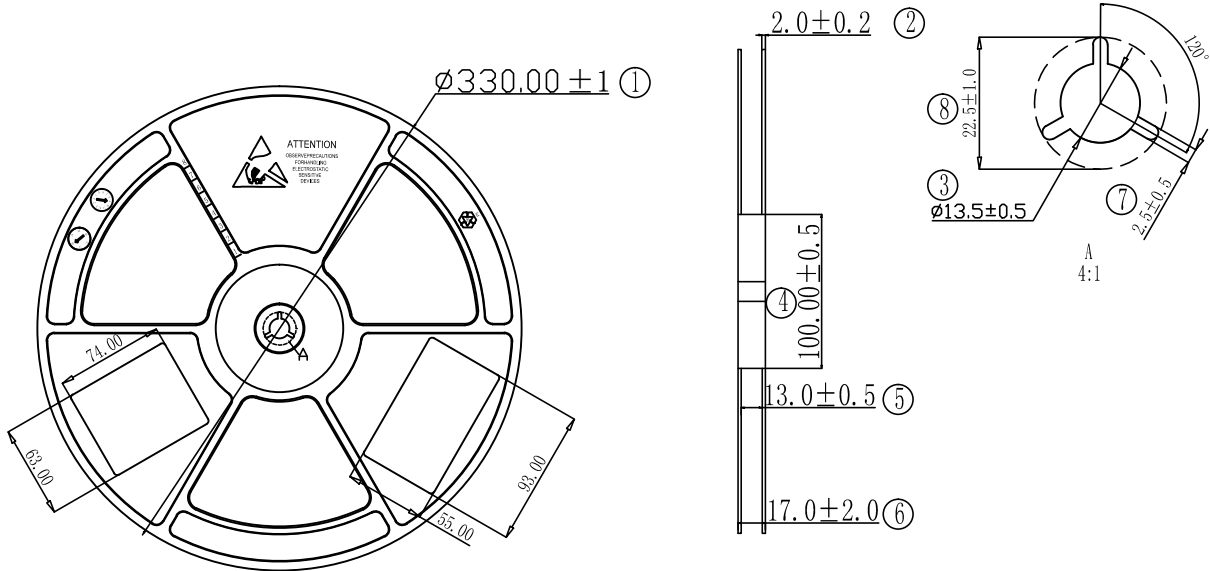
DFN3X3-8D Package Outline Data



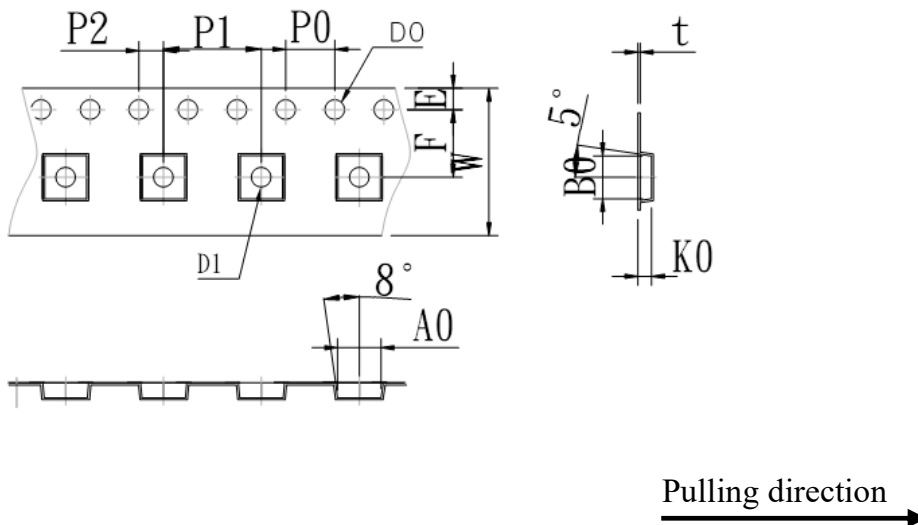
Symbol	Min	Typ	Max
A	0.725	0.775	0.825
B	0.28	0.38	0.48
C	0.13	0.15	0.20
D	3.05	3.15	3.25
D1			0.10
E	3.25	3.35	3.45
E1	3.0	3.1	3.2
e	0.60	0.65	0.70
F	0.27	0.32	0.37
H	1.63	1.73	1.83
L	0.93	1.03	1.13

Tape & Reel Information

Dimensions in mm



Symbol	A0	B0	K0	D0	D1	P0	P1	10*P0
Spec	3.55±0.10	3.45±0.10	1.13±0.10	1.55±0.10	1.55±0.10	4.00±0.10	8.00±0.10	40.0±0.10
Symbol	W	E	F	P2	t			
Spec	12.00±0.10	1.75±0.10	5.50±0.10	2.00±0.10	0.20±0.05			



Marking Information:

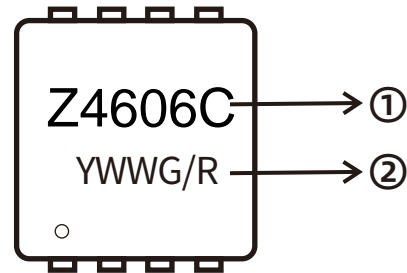
①:Part NO.

② : Date Code (YWWG / R)

Y: Year Code , last digit of the year

WW : Week Code (01-53)

G/R: G(Green) R(L/ead Free)



Previous Version

Version	Date	Subjects (major changes since last revision)
1.0	2025-09-14	Release of final version

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