1.General Description

The 74HC125; 74HCT125 is a quad buffer/line driver with 3-state outputs controlled by the output enable inputs ($n\overline{OE}$). A HIGH on $n\overline{OE}$ causes the outputs to assume a high impedance OFF-state. Inputs include clamp diodes. This enables the use of current limiting resistors to interface inputs to voltages in excess of V_{CC}.

2.Features and Benefits

- Wide supply voltage range from 2.0 V to 6.0 V
- High noise immunity
- CMOS low power dissipation
- Latch-up performance exceeds 250 mA
- Complies with JEDEC standards:
  - JESD8C (2.7 V to 3.6 V)
  - JESD7A (2.0 V to 6.0 V)
- Input levels:
  - For 74HC125: CMOS level
  - For 74HCT125: TTL level
- ESD protection:
  - HBM ANSI/ESDA/JEDEC JS-001 Class 2 exceeds 3500 V
  - CDM ANSI/ESDA/JEDEC JS-002 Class C3 exceeds 2000 V
- Multiple package options

3. Ordering Information

Table 1. Ordering information

Type number	Package		
	Name	Description	Quantity
74HC125D	SOP-14L	plastic small outline package; 14 leads; body width 3.9 mm	2500
74HCT125D			
74HC125PW	TSSOP-14L	plastic thin shrink small outline package; 14 leads; body width 4.4 mm	2500
74HCT125PW			

4. Function Diagram

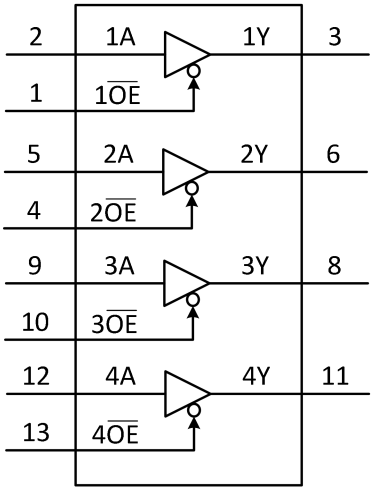


Fig. 1. Logic symbol

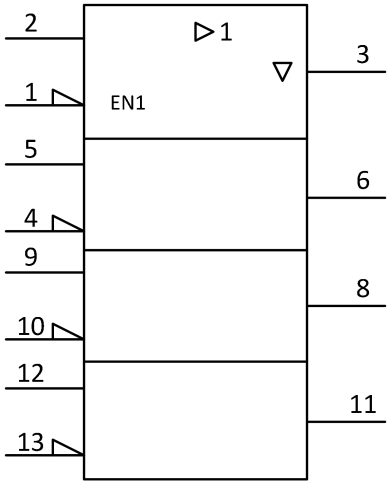


Fig. 2. IEC logic symbol

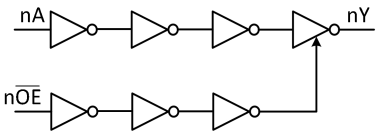


Fig. 3. Logic diagram(one gate)

5. Pinning Information

5.1. Pinning

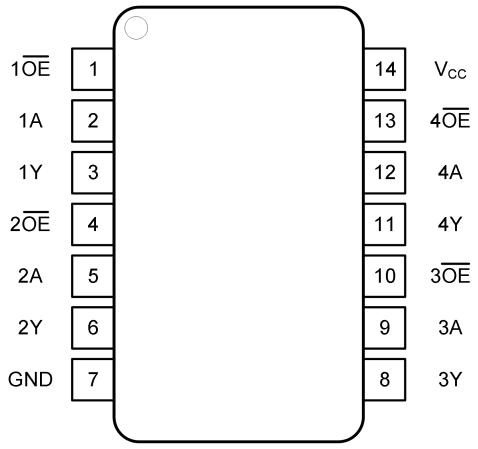


Fig. 4. Top view pin configuration SOP and TSSOP

5.2. Pin description

Table 2. Pin description

Symbol	Pin	Description
1$\overline{OE}$, 2$\overline{OE}$, 3$\overline{OE}$, 4$\overline{OE}$	1, 4, 10, 13	Data enable input(active LOW)
1A, 2A, 3A, 4A	2, 5, 9, 12	Data input
1Y, 2Y, 3Y, 4Y	3, 6, 8, 11	Data output
GND	7	Ground (0V)
V_{CC}	14	Supply voltage

6. Functional Description

Table 3. Function table

H = HIGH voltage level; L = LOW voltage level; X = don't care; Z = high-impedance OFF-state.

Input		Output
n$\overline{OE}$	nA	nY
L	L	L
L	H	H
H	X	Z

7. Absolute Maximum Ratings

Stresses exceeding the absolute maximum ratings may damage the device. The device may not function or be operable above the recommended operating conditions and stressing the parts to these levels is not recommended. In addition, extended exposure to stresses above the recommended operating conditions may affect device reliability. The absolute maximum ratings are stress ratings only.

Table 4. Absolute Maximum Ratings

In accordance with the Absolute Maximum Rating System (IEC 60134). Voltages are referenced to GND.

Symbol	Parameter	Conditions	Min	Max	Unit
V_{CC}	supply voltage		-0.5	7.0	V
I_{IK}	input clamping current	$V_I < -0.5$ V or $V_I > V_{CC} + 0.5$ V [1]		±20	mA
I_{OK}	output clamping current	$V_O < -0.5$ V or $V_O > V_{CC} + 0.5$ V [1]		±20	mA
I_O	output current	V_O = -0.5 V to (V_{CC} + 0.5 V)		±35	mA
I_{CC}	supply current			70	mA
I_{GND}	ground current		-70		mA
P_{tot}	total power dissipation			500	mW
T_{stg}	storage temperature		-65	150	°C

[1] The input and output voltage ratings may be exceeded if the input and output current ratings are observed.

8. Recommended Operating Conditions

The Recommended Operating Conditions table defines the conditions for actual device operation. Recommended operating conditions are specified to ensure optimal performance to the datasheet specifications. EnergyMath does not recommend exceeding them or designing to Absolute Maximum Ratings.

Table 5. Recommended Operating Conditions

Symbol	Parameter	Conditions	74HC125			74HCT125			Unit
			Min	Typ	Max	Min	Typ	Max	
V_{CC}	supply voltage		2.0	5.0	6.0	4.5	5.0	5.5	V
V_I	input voltage		0		V_{CC}	0		V_{CC}	V
V_O	output voltage		0		V_{CC}	0		V_{CC}	V
T_{amb}	ambient temperature		-40		125	-40		125	°C
Δt/ΔV	input transition rise and fall rate	V_{CC} = 2.0 V			625				ns/V
		V_{CC} = 4.5 V		1.67	139		1.67	139	ns/V
		V_{CC} = 6.0 V			83				ns/V

9.Static Characteristics

Table 6. Static characteristics

At recommended operating conditions. Voltages are referenced to GND (ground = 0 V). Typical values measured at T_{amb} = 25°C (unless otherwise noted).

Symbol	Parameter	Conditions	-40 °C to +85 °C			-40 °C to +125 °C		Unit
			Min	Typ	Max	Min	Max	
74HC125								
V_{IH}	HIGH-level input voltage	V_{CC} = 2.0 V	1.5			1.5		V
		V_{CC} = 4.5 V	3.15			3.15		V
		V_{CC} = 6.0 V	4.2			4.2		V
V_{IL}	LOW-level input voltage	V_{CC} = 2.0 V			0.5		0.5	V
		V_{CC} = 4.5 V			1.35		1.35	V
		V_{CC} = 6.0 V			1.8		1.8	V
V_{OH}	HIGH-level output voltage	V_I = V_{IH} or V_{IL}						
		I_O = -20 µA; V_{CC} = 2.0 V	1.9			1.9		V
		I_O = -20 µA; V_{CC} = 4.5 V	4.4			4.4		V
		I_O = -20 µA; V_{CC} = 6.0 V	5.9			5.9		V
		I_O = -6.0 mA; V_{CC} = 4.5 V	3.84			3.7		V
		I_O = -7.8 mA; V_{CC} = 6.0 V	5.34			5.2		V
V_{OL}	LOW-level output voltage	V_I = V_{IH} or V_{IL}						
		I_O = 20 µA; V_{CC} = 2.0 V			0.1		0.1	V
		I_O = 20 µA; V_{CC} = 4.5 V			0.1		0.1	V
		I_O = 20 µA; V_{CC} = 6.0 V			0.1		0.1	V
		I_O = 6.0 mA; V_{CC} = 4.5 V			0.33		0.4	V
		I_O = 7.8 mA; V_{CC} = 6.0 V			0.33		0.4	V
I_I	input leakage current	V_I = V_{CC} or GND ; V_{CC} = 6.0 V			±1		±1	µA
I_{OZ}	OFF-state output current	V_I = V_{IH} or V_{IL} ; V_{CC} = 6.0 V ; V_O = V_{CC} or GND			±5		±10	µA
I_{CC}	supply current	V_I = V_{CC} or GND ; I_O = 0 A ; V_{CC} = 6.0 V			20		40	µA
C_I	input capacitance			7				pF

Symbol	Parameter	Conditions	-40 °C to +85 °C			-40 °C to +125 °C		Unit
			Min	Typ	Max	Min	Max	
74HCT125								
V_{IH}	HIGH-level input voltage	V_{CC} = 4.5 V to 5.5 V	2.0			2.0		V
V_{IL}	LOW-level input voltage	V_{CC} = 4.5 V to 5.5 V			0.8		0.8	V
V_{OH}	HIGH-level output voltage	V_I = V_{IH} or V_{IL}; V_{CC} = 4.5 V						
		I_O = -20 µA;	4.4			4.4		V
		I_O = -6.0 mA;	3.84			3.7		V
V_{OL}	LOW-level output voltage	V_I = V_{IH} or V_{IL}; V_{CC} = 4.5 V						
		I_O = 20 µA;			0.1		0.1	V
		I_O = 6.0 mA;			0.33		0.4	V
I_I	input leakage current	V_I = V_{CC} or GND ; V_{CC} = 5.5 V			±1		±1	µA
I_{OZ}	OFF-state output current	V_I = V_{IH} or V_{IL} ; V_{CC} = 5.5 V ; V_O = V_{CC} or GND			±5		±10	µA
I_{CC}	supply current	V_I = V_{CC} or GND; I_O = 0 A; V_{CC} = 5.5 V			20		40	µA
ΔI_{CC}	additional supply current	per pin ; V_I = V_{CC} - 2.1 V; I_O = 0 A; other inputs at V_{CC} or GND; V_{CC} = 4.5 V to 5.5 V			1.55		1.85	mA
C_I	input capacitance			10				pF

10. Dynamic Characteristics

Table 7. Dynamic characteristics

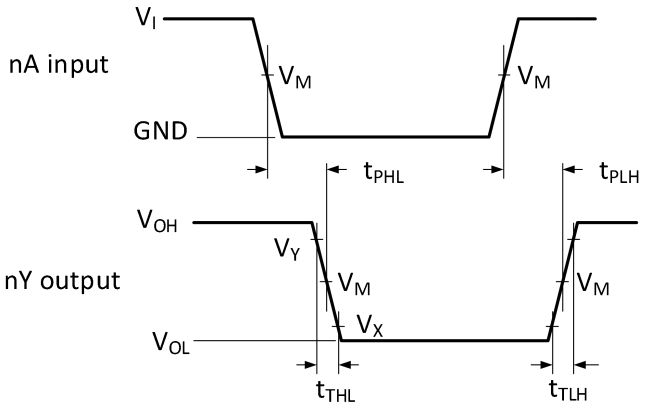
Voltages are referenced to GND (ground = 0 V); for test circuit see Fig. 7. Typical values measured at T_{amb} = 25°C (unless otherwise noted).

Symbol	Parameter	Conditions	-40 °C to +85 °C			-40 °C to +125 °C		Unit
			Min	Typ	Max	Min	Max	
74HC125								
t_{pd}	propagation delay	nA to nY; see Fig. 5 [1]						
		V_{CC} = 2.0 V			35		40	ns
		V_{CC} = 4.5 V			20		25	ns
		V_{CC} = 6.0 V			15		20	ns
t_{en}	enable time	$n\overline{OE}$ to nY; see Fig. 6 [2]						
		V_{CC} = 2.0 V			35		40	ns
		V_{CC} = 4.5 V			20		25	ns
		V_{CC} = 6.0 V			15		20	ns
t_{dis}	disable time	$n\overline{OE}$ to nY; see Fig. 6 [3]						
		V_{CC} = 2.0 V			35		40	ns
		V_{CC} = 4.5 V			20		25	ns
		V_{CC} = 6.0 V			15		20	ns
t_t	transition time	see Fig. 5 [4]						
		V_{CC} = 2.0 V			9		11	ns
		V_{CC} = 4.5 V			6		8	ns
		V_{CC} = 6.0 V			4		5	ns
C_{PD}	power dissipation capacitance	C_L = 15 pF; f = 1 MHz; V_I = GND to V_{CC} [5]		18				pF

Symbol	Parameter	Conditions	-40 °C to +85 °C			-40 °C to +125 °C		Unit
			Min	Typ	Max	Min	Max	
74HCT125								
t_{pd}	propagation delay	nA to nY; V_{CC} = 4.5 V; see Fig. 5 [1]			20		25	ns
t_{en}	enable time	n$\overline{OE}$ to nY; V_{CC} = 4.5 V; see Fig. 6 [2]			20		25	ns
t_{dis}	disable time	n$\overline{OE}$ to nY; V_{CC} = 4.5 V; see Fig. 6 [3]			20		25	ns
t_t	transition time	V_{CC} = 4.5 V; see Fig. 5 [4]			6		8	ns
C_{PD}	power dissipation capacitance	C_L = 15 pF; f = 1 MHz; V_I = GND to (V_{CC} -1.5 V) [5]		37				pF

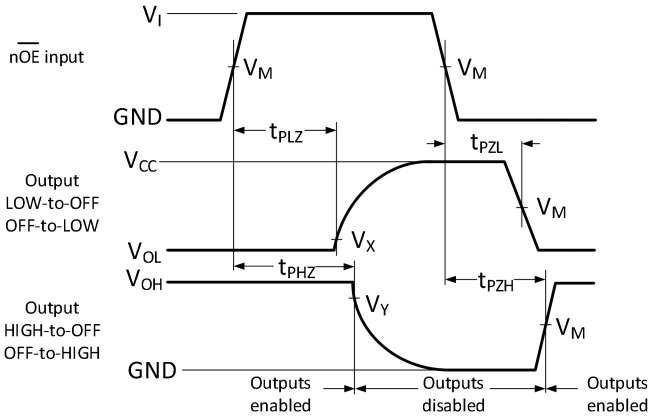
[1] t_{pd} is the same as t_{PHL} and t_{PLH}.
[2] t_{en} is the same as t_{PZH} and t_{PZL}.
[3] t_{dis} is the same as t_{PLZ} and t_{PHZ}.
[4] t_t is the same as t_{THL} and t_{TLH}.
[5] C_{PD} is used to determine the dynamic power dissipation (P_D in µW).
$P_D = C_{PD} \times V_{CC}^2 \times f_i \times N + \Sigma(C_L \times V_{CC}^2 \times f_o)$ where:
f_i = input frequency in MHz;
f_o = output frequency in MHz;
C_L = output load capacitance in pF;
V_{CC} = supply voltage in V;
N = number of inputs switching;
$\Sigma(C_L \times V_{CC}^2 \times f_o)$ = sum of outputs.

10.1. Waveforms and test circuit



Measurement points are given in Table 8.
V_{OL} and V_{OH} are typical output voltage levels that occur with the output load.

Fig. 5. The input nA to output nY propagation delays

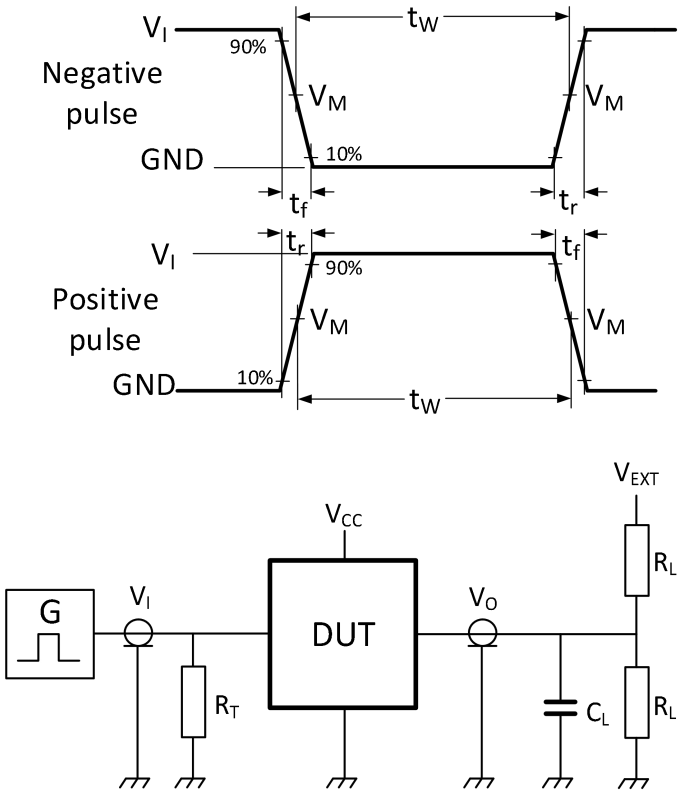


Measurement points are given in Table 8.
V_{OL} and V_{OH} are typical output voltage levels that occur with the output load.

Fig. 6. 3-state enable and disable times

Table 8. Measurement points

Type	Input	Output		
	V_M	V_M	V_X	V_Y
74HC125	$0.5V_{CC}$	$0.5V_{CC}$	$0.1V_{CC}$	$0.9V_{CC}$
74HCT125	1.3 V	1.3 V	$0.1V_{CC}$	$0.9V_{CC}$



Test data is given in Table 9.
Definitions for test circuit:
R_L = Load resistance.
C_L = Load capacitance including jig and probe capacitance.
R_T = Termination resistance should be equal to the output impedance Z_o of the pulse generator.
V_{EXT} = External voltage for measuring switching times.

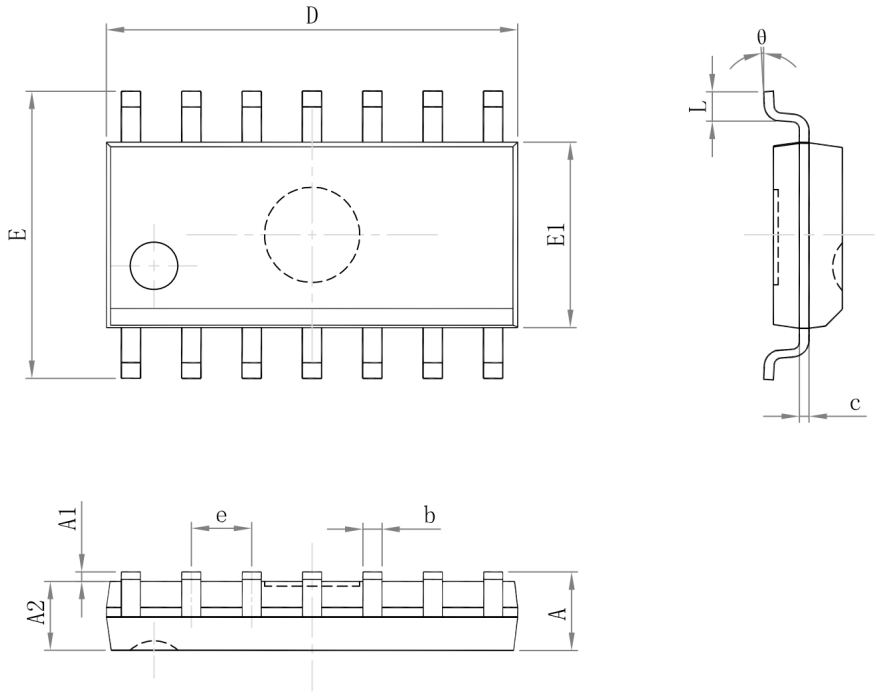
Fig. 7. Test circuit for measuring switching times

Table 9. Test data

Type	Input		Load		V_{EXT}		
	V_I	$t_r = t_f$	C_L	R_L	t_{PLH}, t_{PHL}	t_{PZH}, t_{PHZ}	t_{PZL}, t_{PLZ}
74HC125	V_{CC}	≤ 2.5 ns	15 pF	500Ω	open	GND	$2V_{CC}$
74HCT125	3 V	≤ 2.5 ns	15 pF	500Ω	open	GND	$2V_{CC}$

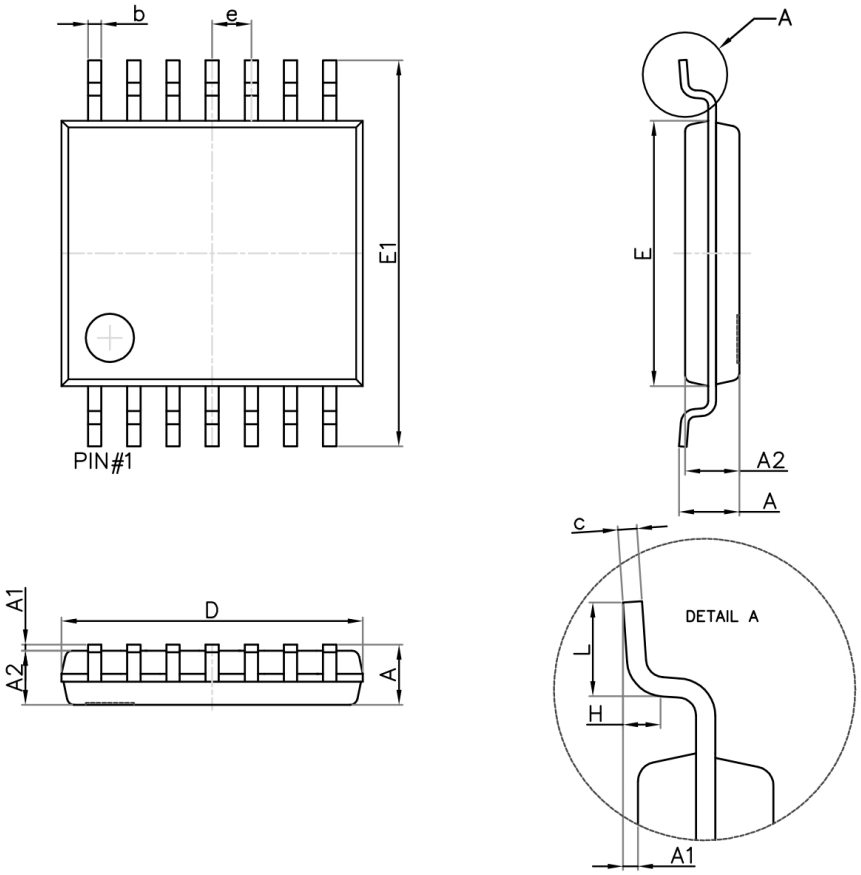
11. Package Outline

SOP-14L



Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min	Max	Min	Max
A	— —	1.750	— —	0.069
A1	0.100	0.250	0.004	0.010
A2	1.250	— —	0.049	— —
b	0.310	0.510	0.012	0.020
c	0.100	0.250	0.004	0.010
D	8.450	8.850	0.333	0.348
E	5.800	6.200	0.228	0.244
E1	3.800	4.000	0.150	0.157
e	1.270(BSC)		0.050(BSC)	
L	0.400	1.270	0.016	0.050
θ	0°	8°	0°	8°

TSSOP-14L



Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min.	Max.	Min.	Max.
D	4.900	5.100	0.193	0.201
E	4.300	4.500	0.169	0.177
b	0.190	0.300	0.007	0.012
c	0.090	0.200	0.004	0.008
E1	6.250	6.550	0.246	0.258
A	—	1.200	—	0.047
A2	0.800	1.000	0.031	0.039
A1	0.050	0.150	0.002	0.006
e	0.65 (BSC)		0.026 (BSC)	
L	0.500	0.700	0.020	0.028
H	0.25(TYP)		0.01(TYP)	
θ	1°	7°	1°	7°

12. Abbreviations

Table 10. Abbreviations

Acronym	Description
CMOS	Complementary Metal-Oxide Semiconductor
DUT	Device Under Test
ESD	ElectroStatic Discharge
HBM	Human Body Model
CDM	Charged Device Model
TTL	Transistor-Transistor Logic

13. Revision History

Table 11. Revision history

Document ID	Release Date	Data sheet status	Change notice	Supersedes
74HC_HCT125 Rev. 1.0	Aug 08, 2024	Product datasheet		