1.General Description

The 74HC74 and 74HCT74 are dual positive edge triggered D-type flip-flop. They have individual data (nD), clock (nCP), set ($n\overline{SD}$) and reset ($n\overline{RD}$) inputs, and complementary nQ and $n\overline{Q}$ outputs. Data at the nD-input, that meets the set-up and hold time requirements on the LOW-to-HIGH clock transition, is stored in the flip-flop and appears at the nQ output. Schmitt-trigger action in the clock input, makes the circuit highly tolerant to slower clock rise and fall times. Inputs include clamp diodes that enable the use of current limiting resistors to interface inputs to voltages in excess of V_{CC}.

2.Features and Benefits

- Wide operating voltage 2.0 V to 6.0 V
- High noise immunity
- CMOS low power dissipation
- Input levels:
  - For 74HC74: CMOS level
  - For 74HCT74: TTL level
- Symmetrical output impedance
- Balanced propagation delays
- Latch-up performance exceeds 250 mA
- Complies with JEDEC standard:
  - JESD8C (2.7 V to 3.6 V)
  - JESD7A (2.0 V to 6.0 V)
- ESD protection:
  - HBM ANSI/ESDA/JEDEC JS-001 Class 3A exceeds 3500 V
  - CDM ANSI/ESDA/JEDEC JS-002 Class C3 exceeds 2000 V
- Multiple package options

3. Ordering Information

Table 1. Ordering information

Type number	Package		
	Name	Description	Quantity
74HC74D	SOP-14L	plastic small outline package; 14 leads; body width 3.9 mm	2500
74HCT74D			
74HC74PW	TSSOP14L	plastic thin shrink small outline package; 14 leads; body width 4.4 mm	2500
74HCT74PW			

4. Function Diagram

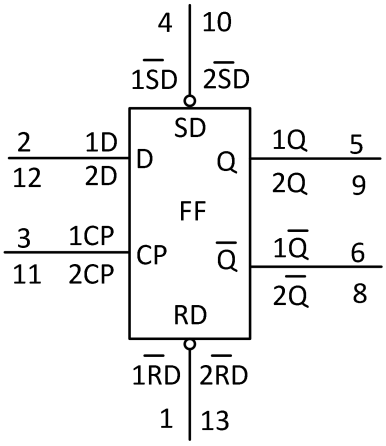


Fig. 1. Logic symbol

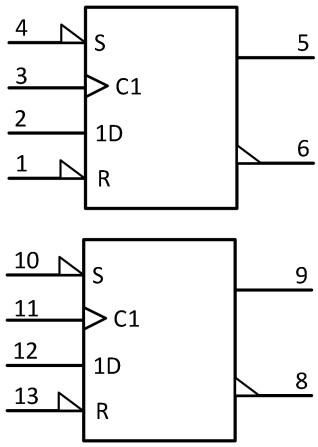


Fig. 2. IEC logic symbol

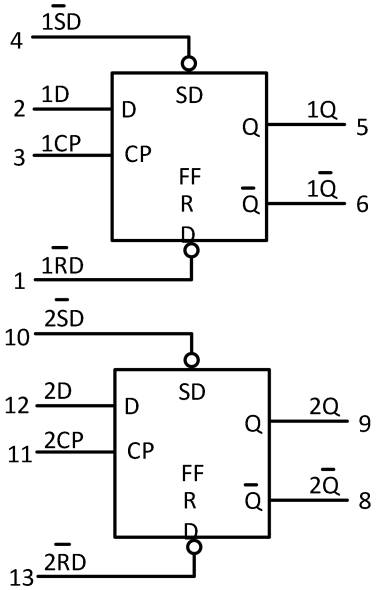


Fig. 3. Logic diagram

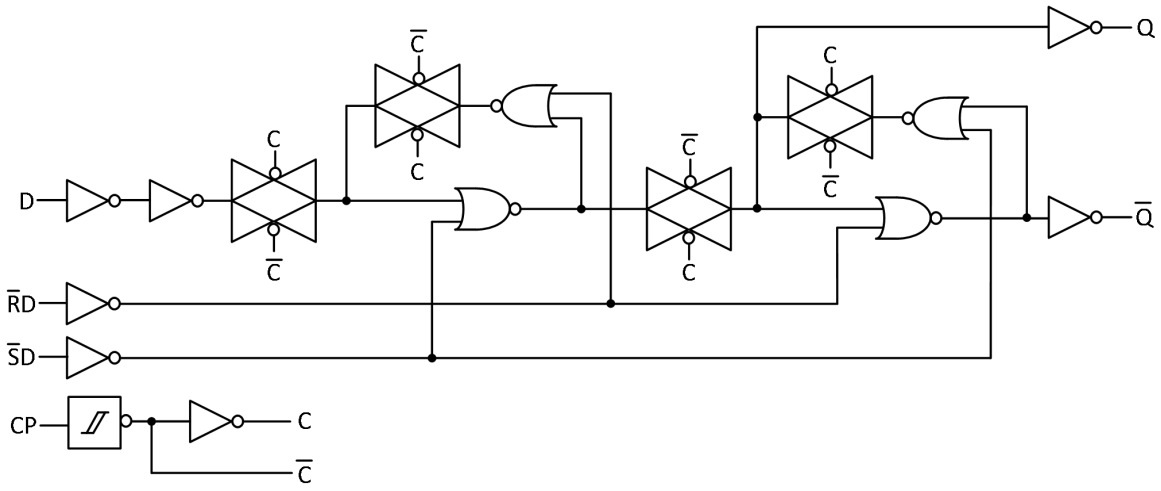


Fig. 4. Logic diagram for one flip-flop

5. Pinning Information

5.1. Pinning

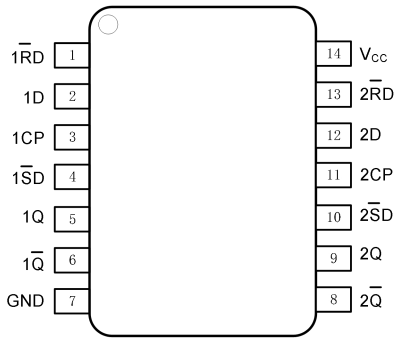


Fig. 5. Top view pin configuration SOP-14L and TSSOP14L

5.2. Pin description

Table 2. Pin description

Symbol	Pin	Description
$1\overline{R}D$, $2\overline{R}D$	1, 13	asynchronous reset-direct input (active LOW)
1D, 2D	2, 12	data output
1CP, 2CP	3,11	clock input (LOW-to-HIGH, edge-triggered)
$1\overline{S}D$, $2\overline{S}D$	4,10	asynchronous set-direct input (active LOW)
1Q, 2Q	5,9	output
$1\overline{Q}$, $2\overline{Q}$	6,8	complement output
GND	7	ground (0 V)
V_{CC}	14	supply voltage

6.Functional Description

Table 3. Function table

H = HIGH voltage level; L = LOW voltage level; X = don't care.

Input				Output	
$n\overline{S}D$	$n\overline{R}D$	nCP	nD	nQ	$n\overline{Q}$
L	H	X	X	H	L
H	L	X	X	L	H
L	L	X	X	H	H

Table 4. Function table

H = HIGH voltage level; L = LOW voltage level; X = don't care;

↑ = LOW-to-HIGH transition; Q_{n+1} = state after the next LOW-to-HIGH CP transition.

Input				Output	
$n\overline{S}D$	$n\overline{R}D$	nCP	nD	nQ_{n+1}	$n\overline{Q}_{n+1}$
H	H	↑	L	L	H
H	H	↑	H	H	L

7. Absolute Maximum Ratings

Stresses exceeding the absolute maximum ratings may damage the device. The device may not function or be operable above the recommended operating conditions and stressing the parts to these levels is not recommended. In addition, extended exposure to stresses above the recommended operating conditions may affect device reliability. The absolute maximum ratings are stress ratings only.

Table 5. Absolute Maximum Ratings

In accordance with the Absolute Maximum Rating System (IEC 60134). Voltages are referenced to GND.

Symbol	Parameter	Conditions	Min	Max	Unit
V_{CC}	supply voltage		-0.5	7	V
I_{IK}	input clamping current	$V_I < -0.5$ V or $V_I > V_{CC} + 0.5$ V		±20	mA
I_{OK}	output clamping current	$V_O < -0.5$ V or $V_O > V_{CC} + 0.5$ V		±20	mA
I_O	output current	$-0.5V < V_O < V_{CC} + 0.5$ V		±25	mA
I_{CC}	supply current			100	mA
I_{GND}	ground current		-100		mA
P_{tot}	total power dissipation	Tamb = -40 °C to + 125 °C		500	mW
T_{stg}	storage temperature		-65	+150	°C

8. Recommended Operating Conditions

The Recommended Operating Conditions table defines the conditions for actual device operation. Recommended operating conditions are specified to ensure optimal performance to the datasheet specifications. EnergyMath does not recommend exceeding them or designing to Absolute Maximum Ratings.

Table 6. Recommended Operating Conditions

Symbol	Parameter	Conditions	74HC74			74HCT74			Unit
			Min	Typ	Max	Min	Typ	Max	
V_{CC}	supply voltage		2.0	5.0	6.0	4.5	5.0	5.5	V
V_I	input voltage		0		V_{CC}	0		V_{CC}	V
V_O	output voltage		0		V_{CC}	0		V_{CC}	V
T_{amb}	ambient temperature		-40	+25	+125	-40	+25	+125	°C
Δt/ΔV	input transition rise and fall rate	V_{CC} = 2.0 V			625				ns/V
		V_{CC} = 4.5 V		1.67	139		1.67	139	ns/V
		V_{CC} = 6.0 V			83				ns/V

9.Static Characteristics

Table 7. Static characteristics

At recommended operating conditions. Voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions	-40 °C to +85 °C			-40 °C to +125 °C		Unit
			Min	Typ[1]	Max	Min	Max	
74HC74								
V_{IH}	HIGH-level input voltage	V_{CC} = 2.0 V	1.5	1.2		1.5		V
		V_{CC} = 4.5 V	3.15	2.5		3.15		V
		V_{CC} = 6.0 V	4.2	3.3		4.2		V
V_{IL}	LOW-level input voltage	V_{CC} = 2.0 V		0.8	0.5		0.5	V
		V_{CC} = 4.5 V		2.1	1.35		1.35	V
		V_{CC} = 6.0 V		2.8	1.8		1.8	V
V_{OH}	HIGH-level output voltage	V_I = V_{IH} or V_{IL}						
		I_O = -4.0 mA; V_{CC} = 4.5 V	3.84	4.4		3.7		V
		I_O = -5.2 mA; V_{CC} = 6.0 V	5.34	5.9		5.2		V
V_{OL}	LOW-level output voltage	V_I = V_{IH} or V_{IL}						
		I_O = 4.0 mA; V_{CC} = 4.5 V		0.03	0.33		0.4	V
		I_O = 5.2 mA; V_{CC} = 6.0 V		0.04	0.33		0.4	V
I_I	Input leakage current	V_I = V_{CC} or GND ; V_{CC} = 6.0 V		0.01	±1		±1	µA
I_{CC}	supply current	V_I = V_{CC} or GND ; I_O = 0A ; V_{CC} = 6.0 V		0.01	20		40	µA
C_I	input capacitance			7				pF

Symbol	Parameter	Conditions	-40 °C to +85 °C			-40 °C to +125 °C		Unit
			Min	Typ[1]	Max	Min	Max	
74HCT74								
V_{IH}	HIGH-level input voltage	V_{CC} = 4.5 V to 5.5 V	2.0	1.7		2.0		V
V_{IL}	LOW-level input voltage	V_{CC} = 4.5 V to 5.5 V		1.3	0.8		0.8	V
V_{OH}	HIGH-level output voltage	V_I = V_{IH} or V_{IL}; V_{CC} = 4.5 V						
		I_O = -4.0 mA	3.84	4.4	-	3.7		V
V_{OL}	LOW-level output voltage	V_I = V_{IH} or V_{IL}; V_{CC} = 4.5 V						
		I_O = 4.0 mA		0.03	0.33		0.4	V
I_I	Input leakage current	V_I = V_{CC} or GND ; V_{CC} = 5.5 V		0.01	±1		±1	µA
I_{CC}	supply current	V_I = V_{CC} or GND ; I_O = 0A ; V_{CC} = 5.5 V		0.01	20		40	µA
ΔI_{CC}	additional supply current	V_I = V_{CC} - 2.1 V; I_O = 0 A; other inputs at V_{CC} or GND;V_{CC} = 4.5 V to 5.5 V						
		per input pin; nD,n$\overline{R}$D inputs		350	500		550	µA
		per input pin; n$\overline{S}$D inputs		640	850		950	µA
		per input pin; nCP inputs		1130	1550		1650	µA
C_I	input capacitance			7				pF

[1]All typical values are measured at T_{amb} = 25℃.

10. Dynamic Characteristics

Table 8. Dynamic characteristics

Voltages are referenced to GND (ground = 0 V); for test circuit see Fig. 8.

Symbol	Parameter	Conditions	-40 °C to +85 °C			-40 °C to +125 °C		Unit
			Min	Typ[1]	Max	Min	Max	
74HC74								
t_{pd}	propagation delay	nCP to nQ, nQ̄; see Fig. 6 [2]						
		V_{CC} = 2.0 V			30		33	ns
		V_{CC} = 4.5 V			16		19	ns
		V_{CC} = 6.0 V			12		14	ns
		nS̄D to nQ, nQ̄; see Fig. 7 [2]						
		V_{CC} = 2.0 V			30		33	ns
		V_{CC} = 4.5 V			16		19	ns
		V_{CC} = 6.0 V			12		14	ns
		nR̄D to nQ, nQ̄; see Fig. 7 [2]						
		V_{CC} = 2.0 V			30		33	ns
		V_{CC} = 4.5 V			16		19	ns
		V_{CC} = 6.0 V			12		14	ns
t_t	transition time	nQ, nQ̄;see Fig. 6 [3]						
		V_{CC} = 2.0 V			9		11	ns
		V_{CC} = 4.5 V			6		8	ns
		V_{CC} = 6.0 V			4		5	ns
t_w	pulse width	nCP HIGH or LOW; see Fig. 6						
		V_{CC} = 2.0 V	100			120		ns
		V_{CC} = 4.5 V	20			24		ns
		V_{CC} = 6.0 V	17			20		ns
		nS̄D, nR̄D LOW;see Fig. 7						
		V_{CC} = 2.0 V	100			120		ns
		V_{CC} = 4.5 V	20			24		ns
		V_{CC} = 6.0 V	17			20		ns

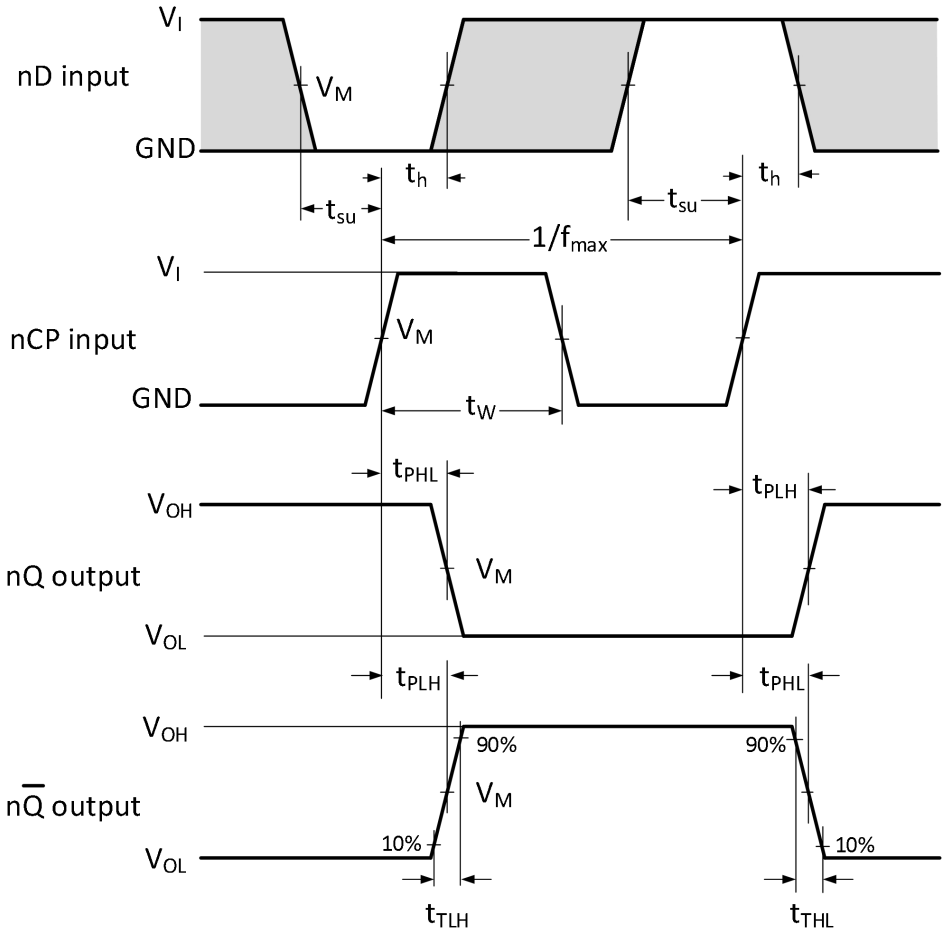
Symbol	Parameter	Conditions	-40 °C to +85 °C			-40 °C to +125 °C		Unit
			Min	Typ[1]	Max	Min	Max	
t_{rec}	recovery time	$n\overline{SD}$, $n\overline{RD}$;see Fig. 7						
		V_{CC} = 2.0 V	40			45		ns
		V_{CC} = 4.5 V	8			9		ns
		V_{CC} = 6.0 V	7			8		ns
t_{su}	set-up time	nD to nCP; see Fig. 6						
		V_{CC} = 2.0 V	75			90		ns
		V_{CC} = 4.5 V	15			18		ns
		V_{CC} = 6.0 V	13			15		ns
t_h	hold time	nD to nCP; see Fig. 6						
		V_{CC} = 2.0 V	3			3		ns
		V_{CC} = 4.5 V	3			3		ns
		V_{CC} = 6.0 V	3			3		ns
f_{max}	maximum frequency	nCP; see Fig. 6						
		V_{CC} = 2.0 V	4.8			4.0		MHz
		V_{CC} = 4.5 V	24			20		MHz
		V_{CC} = 6.0 V	28			24		MHz
C_{PD}	power dissipation capacitance	V_I = GND to V_{CC} ; [4] f = 1MHz		23				pF
74HCT74								
t_{pd}	propagation delay	nCP to nQ, $n\overline{Q}$; see Fig. 6 [2]						
		V_{CC} = 4.5 V			16		19	ns
		$n\overline{SD}$ to nQ, $n\overline{Q}$; see Fig. 7 [2]						
		V_{CC} = 4.5 V			16		19	ns
		$n\overline{RD}$ to nQ, $n\overline{Q}$; see Fig. 7 [2]						
		V_{CC} = 4.5 V			16		19	ns
t_t	transition time	nQ, $n\overline{Q}$;see Fig. 6 [3]						
		V_{CC} = 4.5 V			6		8	ns
t_w	pulse width	nCP HIGH or LOW; see Fig. 6						
		V_{CC} = 4.5 V	23			27		ns
		$n\overline{SD}$, $n\overline{RD}$ LOW;see Fig. 7						

		V_{CC} = 4.5 V	20			24		ns

Symbol	Parameter	Conditions	-40 °C to +85 °C			-40 °C to +125 °C		Unit
			Min	Typ[1]	Max	Min	Max	
t_{rec}	recovery time	$n\overline{SD}$, $n\overline{RD}$;see Fig. 7						
		V_{CC} = 4.5 V	8			9		ns
t_{su}	set-up time	nD to nCP; see Fig. 6						
		V_{CC} = 4.5 V	15			18		ns
t_h	hold time	nD to nCP; see Fig. 6						
		V_{CC} = 4.5 V	3			3		ns
f_{max}	maximum frequency	nCP; see Fig. 6						
		V_{CC} = 4.5 V	22			18		MHz
C_{PD}	power dissipation capacitance	V_I = GND to V_{CC} ; [4] f = 1MHz		24				pF

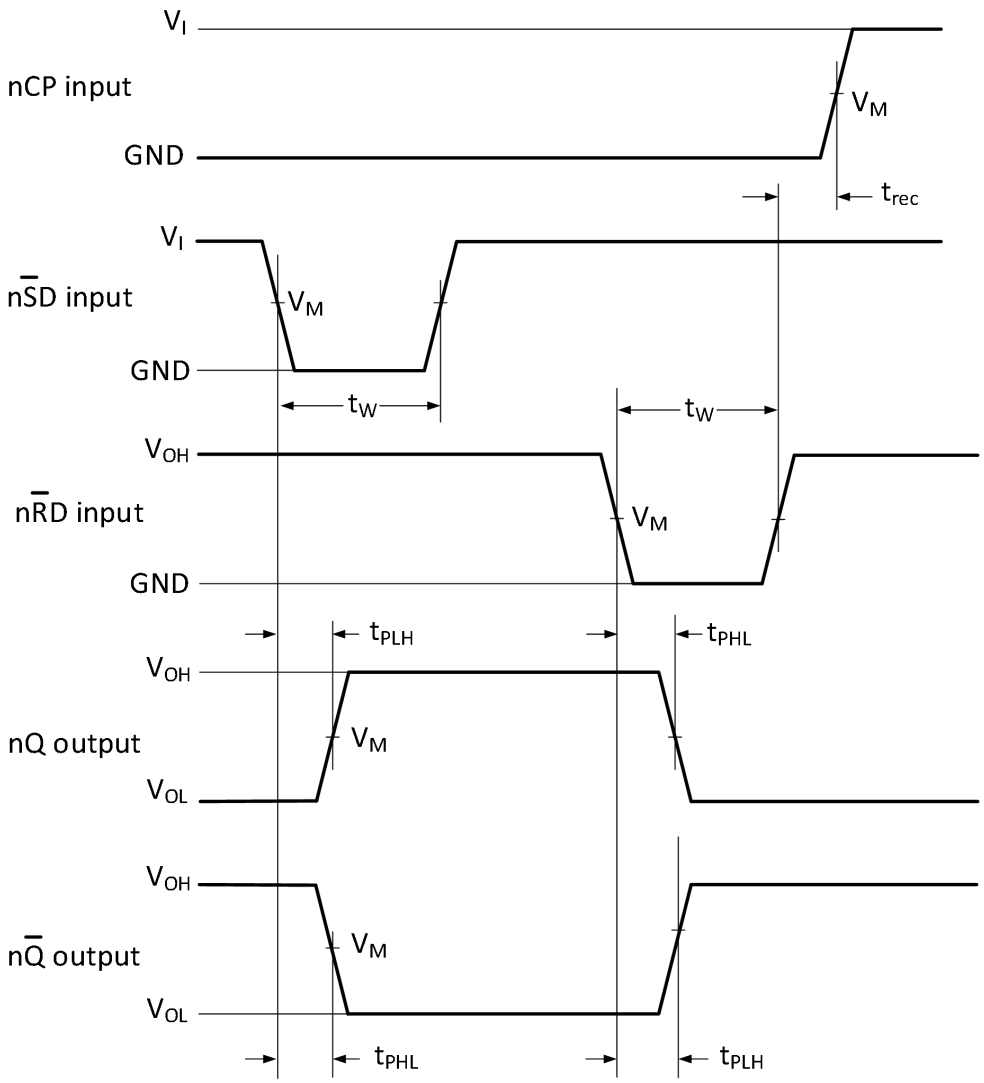
[1] Typical values are measured at T_{amb} = 25 °C.
[2] t_{pd} is the same as t_{PLH} and t_{PHL}.
[3] t_t is the same as t_{THL} and t_{TLH}.
[4] C_{PD} is used to determine the dynamic power dissipation (P_D in µW).
$P_D = C_{PD} \times V_{CC}^2 \times f_i \times N + \Sigma(C_L \times V_{CC}^2 \times f_o)$ where:
f_i = input frequency in MHz;
f_o = output frequency in MHz;
C_L = output load capacitance in pF;
V_{CC} = supply voltage in V;
N = number of inputs switching;
$\Sigma(C_L \times V_{CC}^2 \times f_o)$ = sum of outputs.

10.1. Waveforms and test circuit



Measurement points are given in Table 9.
V_{OL} and V_{OH} are typical output voltage levels that occur with the output load.

Fig. 6. The Propagation delay input (CP) to output (Qn), output transition time, clock input (CP) pulse width and the maximum frequency (CP)

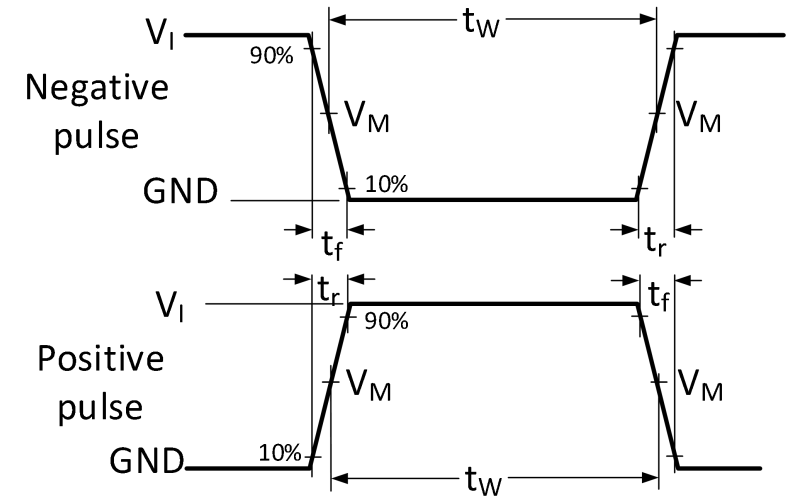


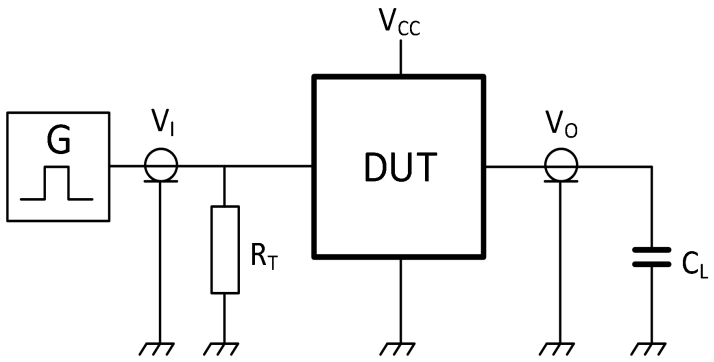
Measurement points are given in Table 9.
V_{OL} and V_{OH} are typical output voltage levels that occur with the output load.

Fig. 7. The set ($n\overline{SD}$) and reset ($n\overline{RD}$) input to output (nQ,$n\overline{Q}$) propagation delays, set and reset pulse widths and the $n\overline{SD}$, $n\overline{RD}$ to nCP recovery time

Table 9. Measurement points

Type	Input	Output
	V_M	V_M
74HC74	$0.5V_{CC}$	$0.5V_{CC}$
74HCT74	1.3V	1.3V





Test data is given in Table 10.
Definitions for test circuit:
R_L = Load resistance.
C_L = Load capacitance including jig and probe capacitance.
R_T = Termination resistance should be equal to the output impedance Z_o of the pulse generator..

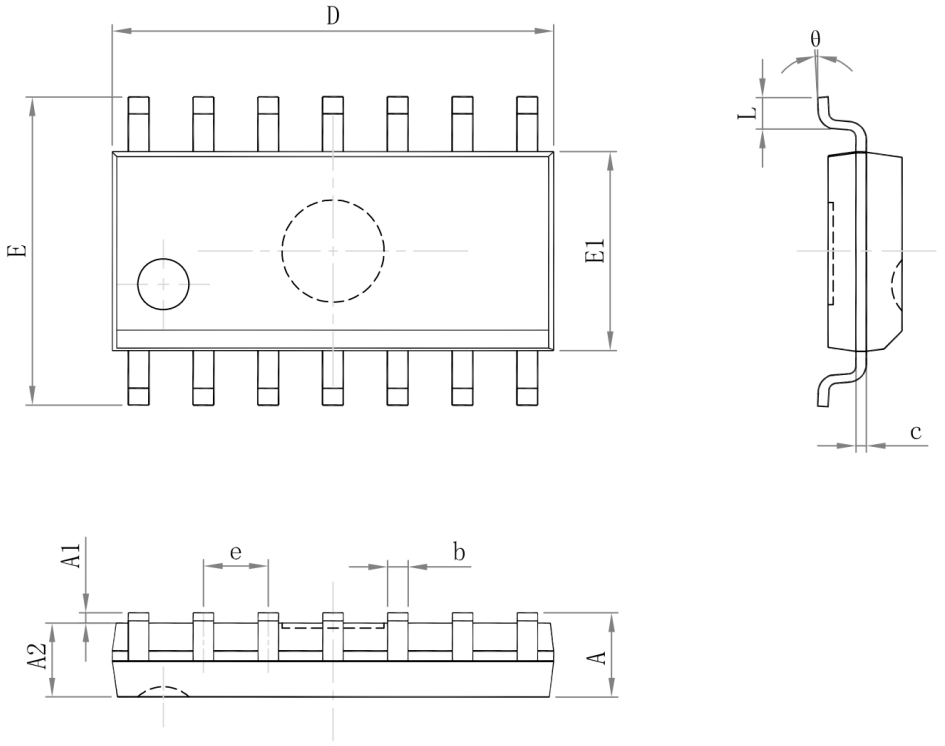
Fig. 8. Test circuit for measuring switching times

Table 10. Test data

Type	Input		Load	Test
	V_I	$t_r = t_f$	C_L	
74HC74	V_{CC}	≤ 2.5 ns	15 pF	t_{PLH}, t_{PHL}
74HCT74	3 V	≤ 2.5 ns	15 pF	t_{PLH}, t_{PHL}

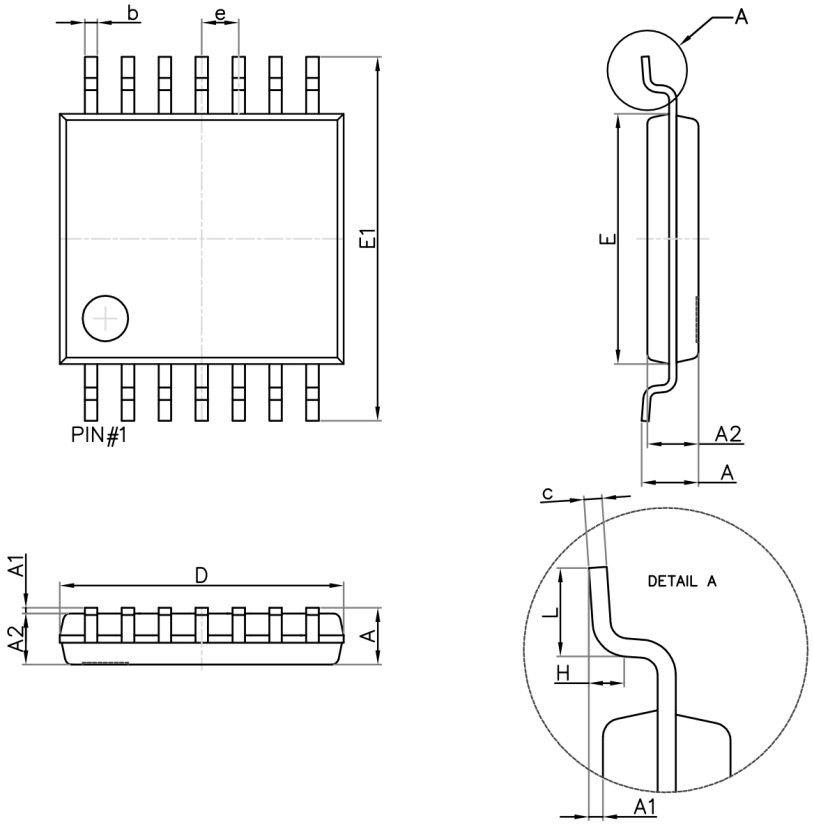
11. Package Outline

SOP-14L



Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min	Max	Min	Max
A	— —	1.750	— —	0.069
A1	0.100	0.250	0.004	0.010
A2	1.250	— —	0.049	— —
b	0.310	0.510	0.012	0.020
c	0.100	0.250	0.004	0.010
D	8.450	8.850	0.333	0.348
E	5.800	6.200	0.228	0.244
E1	3.800	4.000	0.150	0.157
e	1.270(BSC)		0.050(BSC)	
L	0.400	1.270	0.016	0.050
θ	0°	8°	0°	8°

TSSOP-14L



Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min.	Max.	Min.	Max.
D	4.900	5.100	0.193	0.201
E	4.300	4.500	0.169	0.177
b	0.190	0.300	0.007	0.012
c	0.090	0.200	0.004	0.008
E1	6.250	6.550	0.246	0.258
A	—	1.200	—	0.047
A2	0.800	1.000	0.031	0.039
A1	0.050	0.150	0.002	0.006
e	0.65 (BSC)		0.026 (BSC)	
L	0.500	0.700	0.020	0.028
H	0.25(TYP)		0.01(TYP)	
θ	1°	7°	1°	7°

12. Abbreviations

Table 11. Abbreviations

Acronym	Description
CMOS	Complementary Metal-Oxide Semiconductor
DUT	Device Under Test
ESD	ElectroStatic Discharge
HBM	Human Body Model
CDM	Charged Device Model
TTL	Transistor-Transistor Logic

13. Revision History

Table 12. Revision history

Document ID	Release Date	Data sheet status	Change notice	Supersedes
74HC74_HCT74 Rev. 1.0	Aug 08, 2024	Product datasheet		