

基本描述

MX5050S6030A1 高侧理想二极管电路内部集成 MOSFET，当与电源串联时用作理想二极管整流器。该理想二极管电路可使内部 MOSFET 替换主回路中的防反二极管，从而降低功耗和压降。

MX5050S6030A1 控制器为内部 N 沟道 MOSFET 和快速响应比较器提供电荷泵栅极驱动，在电流反向时关断 MOSFET。MX5050S6030A1 可连接 5V 至 40V 的电源，当输入电压在 1V 到 4V 之间时，VS 需要另外接 5V 以上的供电。

特性

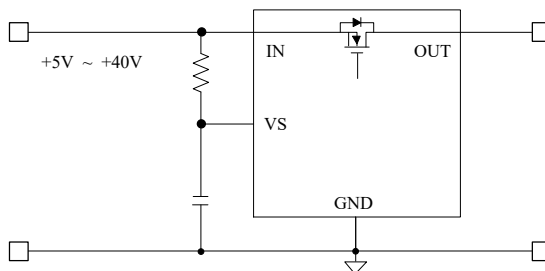
- ◆ 宽工作输入电压范围 VIN: 1V 到 40V (VIN < 5V 时需要 VBIAS)
- ◆ 50V 瞬态电压
- ◆ 电流反向时可快速响应
- ◆ 内部 2A 峰值栅极关断电流
- ◆ 超小 V_{DS} 关断电压，缩短关断时间
- ◆ ESOP8 封装

应用

冗余 (N+1) 电源的有源 OR-ings

基本信息

典型应用



器件信息

型号	描述
MX5050S6030A1	ESOP8L
MPQ	3000pcs

封装耗散值

Package	RθJA (°C/W)
ESOP8L	60

极限值

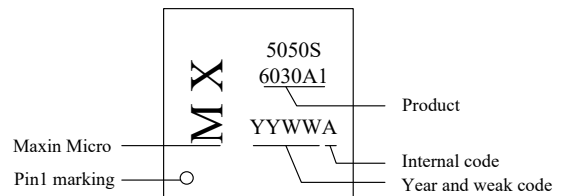
参数	值
IN, OUT Pins to GND	-0.3 to 60V
VS Pin to Ground	-0.3 to 60V
Internal MOSFET VDS	≥60V
Junction temperature	150°C
Storage temperature, Tstg	-50 to 150°C
Leading temperature (soldering, 10secs)	260°C
ESD Susceptibility HBM	±2000V

Stresses beyond those listed in Absolute Maximum Ratings may cause permanent damage to the device. Exposure to absolute maximum rating conditions for extended periods may affect reliability. Functional operation of the device at any conditions beyond those indicated in the Recommended Operating Conditions section is not implied.

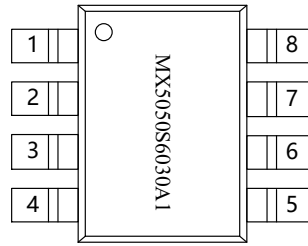
推荐工作条件

项目	范围
IN, OUT Pins (VS ≥ 4.5V for IN < 4V)	1-40V
VS Pin	5-40V
Operating temperature	-40~125°C

丝印信息



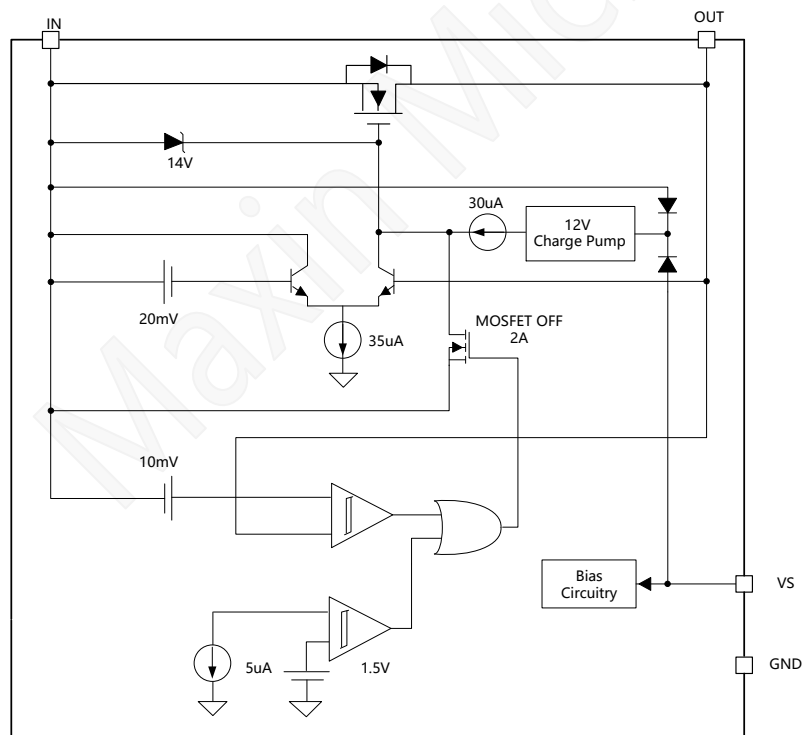
Terminal assignments



Pin information

PIN NO.	PIN name	Description
1、 2	IN	Voltage sense connection to the internal MOSFET source pin.
3	GND	Ground.
4	VS	The main supply pin for all internal biasing and an auxiliary supply for the internal gate drive charge pump. Typically connected to either V_{OUT} or V_{IN} ; VS is connected to V_{IN} is recommended to reduce leakage current during reverse shutdown mode. A separate supply can also be used.
5、 6、 7、 8	NC	Not connect.
THERMAL PAD	OUT	Voltage sense connection to the external MOSFET drain pin.

Block diagram



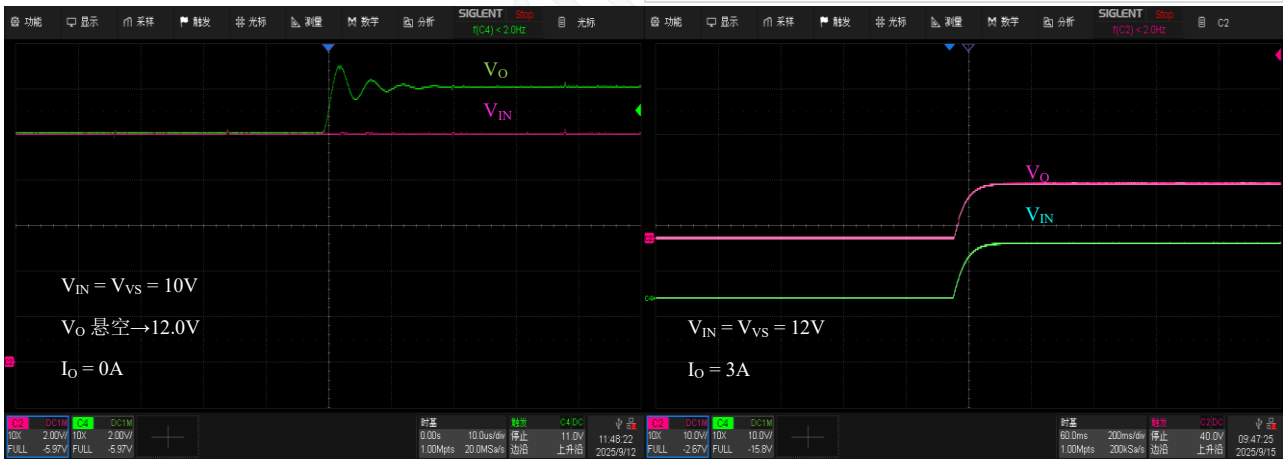
Electrical characteristics

($V_{IN} = 12V$, $V_{VS} = V_{IN}$, $T_A = 25^\circ C$, unless otherwise noted)

Symbol	Parameter	Test condition	Min	Typ.	Max	Unit
VS PIN						
V_{VS}	Operating Supply Voltage Range		5		40	V
I_{VS}	Operating Supply Current	$V_{VS} = 5V, V_{IN} = V_{VS}, V_{OUT} = V_{IN} - 100\text{ mV}$		50	70	uA
		$V_{VS} = 12V, V_{IN} = V_{VS}, V_{OUT} = V_{IN} - 100\text{ mV}$		52	70	
		$V_{VS} = 40V, V_{IN} = V_{VS}, V_{OUT} = V_{IN} - 100\text{ mV}$		56	100	
IN PIN						
V_{IN}	Operating Input Voltage Range		5		40	V
I_{IN}	IN Pin current	$V_{IN} = 5V, V_{VS} = V_{IN}, V_{OUT} = V_{IN} - 100\text{ mV}$	150	240	300	uA
		$V_{IN} = 12V\text{ to }40V, V_{OUT} = V_{IN} - 100\text{ mV}$	200	300	400	
OUT PIN						
V_{OUT}	Operating Output Voltage Range		5		40	V
I_{OUT}	OUT Pin Current	$V_{IN} = 5V\text{ to }40V, V_{VS} = V_{IN}$		4.1		uA
INTERNAL REGULATOR						
$I_{GATE(OFF)}$	Internal Sink Current	$V_{GATE} = V_{IN} + 3V, V_{OUT} > V_{IN} + 100\text{mV},$ $t \leq 10\text{ms}$		2		A
$V_{SD(REV)}$	Reverse V_{SD} Threshold $V_{IN} < V_{OUT}$	$V_{IN} - V_{OUT}$	-20	-10	0	mV
$V_{SD(REG)}$	Regulated Forward V_{SD} Threshold $V_{IN} > V_{OUT}$	$V_{IN} = 5V, V_{VS} = V_{IN}, V_{IN} - V_{OUT}$	0	20	30	mV
		$V_{IN} = 12V, V_{VS} = V_{IN}, V_{IN} - V_{OUT}$	10	40	60	
INTERNAL MOSFET						
V_{DS}	Drain to source voltage	$I_{DS} = 250\text{uA}$	60			V
R_{ON}	On resistance	$I_D = 1A$		30.0	45.0	mΩ

Characteristic plots

($V_{IN} = V_{VS} = V_{OUT}$, $T_A = 25^\circ\text{C}$, unless otherwise noted)



Operation description

IN and OUT Pins

When power is initially applied, the load current will flow from source to drain through the body diode of the MOSFET. Once the voltage across the body diode exceeds $V_{SD(REG)}$ then the MX5050S6030A1 begins charging the internal MOSFET gate through a $30\mu A$ (typical) charge pump current source. In forward operation, the gate of the internal MOSFET is charged. The MX5050S6030A1 is designed to regulate the internal MOSFET gate-to-source voltage. If the MOSFET current decreases to the point that the voltage across the MOSFET falls below the $V_{SD(REG)}$ voltage regulation point of 20mV (typical), the internal MOSFET gate voltage will be decreased until the voltage across the MOSFET is regulated at 20mV. If the source-to-drain voltage is greater than the $V_{SD(REG)}$ voltage, the gate-to-source voltage will increase and eventually reach the 12V gate to IN pin Zener clamp level.

If the MOSFET current reverses, possibly due to failure of the input supply, such that the voltage across the MX5050S6030A1 IN and OUT pins is more negative than the $V_{SD(REV)}$ voltage of -10mV (typical), the MX5050S6030A1 will quickly discharge the internal MOSFET gate through a strong gate to IN pin discharge transistor. If the input supply fails abruptly, as would occur if the supply was shorted directly to ground, a reverse current will temporarily flow through the MOSFET until the gate can be fully discharged. This reverse current is sourced from the load capacitance and from the parallel connected supplies. The MX5050S6030A1 responds to a voltage reversal condition typically within 50ns. The actual time required to turn off the MOSFET will depend on the charge held by the gate capacitance of the MOSFET being used. For MX5050S6030A1, the gate capacitance of the internal MOSFET is 4.6nF and the typical turn off time is 25ns. This fast turnoff time minimizes voltage disturbances at the output, as well as the current transients from the redundant supplies.

VS Pin

The VS pin of MX5050S6030A1 is the main supply pin for all internal biasing and an auxiliary supply for the internal gate drive charge pump.

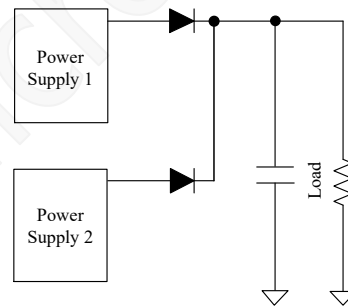
For typical MX5050S6030A1 applications, the VS pin can be connected directly to the OUT pin. The capacitor value should

be the lowest value that produces acceptable filtering of the voltage noise.

Application and Implementation

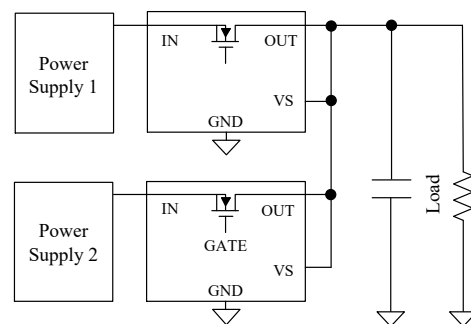
Application Information

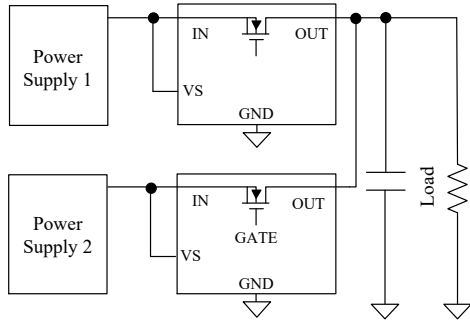
Systems that require high availability often use multiple, parallel-connected redundant power supplies to improve reliability. Schottky OR-ing diodes are typically used to connect these redundant power supplies to a common point at the load. The disadvantage of using OR-ing diodes is the forward voltage drop, which reduces the available voltage and the associated power losses as load currents increase. Using an N-channel MOSFET to replace the OR-ing diode requires a small increase in the level of complexity, but reduces, or eliminates, the need for diode heat sinks or large thermal copper area in circuit board layouts for high power applications.



OR-ing with Diodes

The MX5050S6030A1 is a positive voltage (that is, high-side) OR-ing circuit that will drive an external N-channel MOSFET to replace an OR-ing diode. The voltage across the MOSFET source and drain pins is monitored by the MX5050S6030A1 at the IN and OUT pins, while the internal MOSFET gate drives the MOSFET to control its operation based on the monitored source-drain voltage. The resulting behavior is that of an ideal rectifier with source and drain pins of the MOSFET acting as the anode and cathode pins of a diode respectively.





OR-ing with internal MOSFETs

Short Circuit Failure of an Input Supply

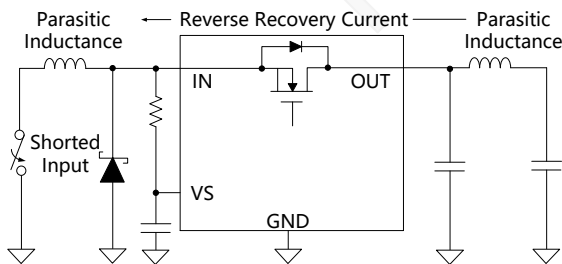
An abrupt 0Ω short circuit across the input supply will cause the highest possible reverse current to flow while the internal MX5050S6030A1 control circuitry discharges the gate of the MOSFET. During this time, the reverse current is limited only by the $R_{DS(ON)}$ of the MOSFET, along with parasitic wiring resistances and inductances. Worst case instantaneous reverse current would be limited to:

$$I_{D(REV)} = (V_{OUT} - V_{IN}) / R_{DS(ON)} \quad (1)$$

The internal Reverse Comparator will react, and will start the process of discharging the internal MOSFET gate, when the reverse current reaches:

$$I_{D(REV)} = V_{SD(REV)} / R_{DS(ON)} \quad (2)$$

When the MOSFET is finally switched off, the energy stored in the parasitic wiring inductances will be transferred to the rest of the circuit. As a result, the MX5050S6030A1 IN pin will see a negative voltage spike while the OUT pin will see a positive voltage spike. The IN pin can be protected by diode clamping the pin to GND in the negative direction. The OUT pin can be protected with a TVS protection diode, a local bypass capacitor, or both.

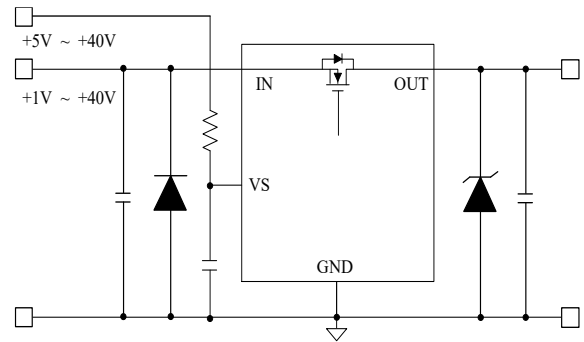


Reverse Recovery Current Generates Spikes at V_{IN} and V_{OUT}

A Separate VS Supply for Low V_{IN} Operation

In some applications, it is desired to operate MX5050S6030A1 from low supply voltage. The MX5050S6030A1 can operate with a 1V rail voltage, provides its VS pin is biased from 5V to 40V. The detail of such application is depicted in the

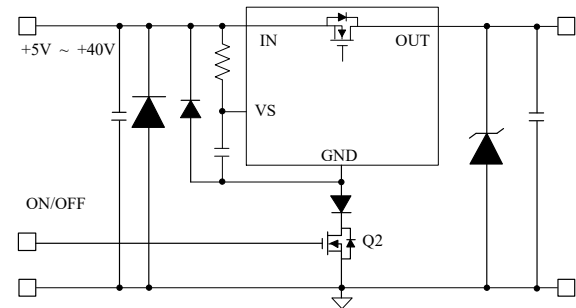
following figure.



Reverse Input Voltage Protection with IQ Reduction

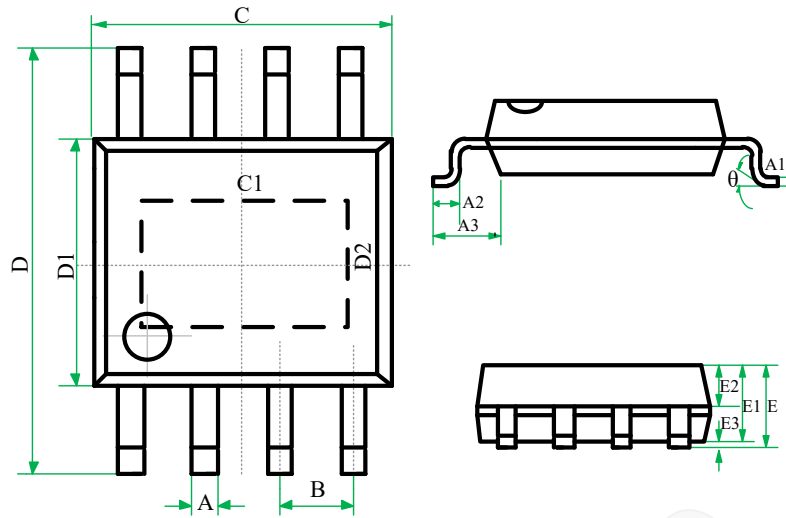
If VS is powered while IN is floating or grounded, then about 0.5mA will leak from the VS pin into the IC and about 3mA will leak from the OUT pin into the IC. From this leakage, about 0.05mA will flow out of the IN pin and the rest will flow to ground. This does not affect long term reliability of the IC but may influence circuit design.

In battery powered applications, whenever MX5050S6030A1 functionality is not needed, the supply to the MX5050S6030A1 can be disconnected by turning off Q2, as shown in the following figure. This disconnects to the ground path of the MX5050S6030A1 and eliminates the current leakage from the battery.



Reverse input voltage protection with IQ reduction schematic

Package information ESOP8



SYMBOL	MILLIMETERS			INCHES		
	MIN	NOM	MAX	MIN	NOM	MAX
A	0.39	-	0.48	0.0154	-	0.0189
A1	0.21	-	0.28	0.008	-	0.011
A2	0.50	-	0.80	0.020	-	0.031
A3	1.05BSC			0.041BSC		
B	1.27BSC			0.050BSC		
C	4.70	4.90	5.10	0.185	0.193	0.201
C1	3.202		3.402	0.126		0.134
D	5.80	6.00	6.20	0.228	0.236	0.244
D1	3.70	3.90	4.10	0.146	0.154	0.161
D2	2.313		2.513	0.091		0.099
E	-	-	1.75	-	-	0.069
E1	1.30	1.40	1.50	0.051	0.055	0.059
E2	0.60	0.65	0.70	0.024	0.026	0.028
E3	0.10	-	0.225	0.004	-	0.009
θ	0	-	8°	0	-	8°

ESOP8 for MX5050S6030A1

Restrictions on Product Use

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Version update record:

V1.0 The original version .

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