

### Features

- 4.5 to 15-V Single Supply Range
- Outputs Held Low During VDD UVLO
- TTL and CMOS Compatible Input-Logic Threshold
- Input Design Output Held Low when Input Pins are Floating
- Fast Rise and Fall Times (9ns and 7ns typical)
- Fast Propagation Delays (13ns typical)
- Split Output Configuration
- Strong Sink Current Offers Enhanced Immunity Against Miller Turn on
- Input Pins Capable of Withstanding - 5 V Below GND pin
- Compact package: SOP-8

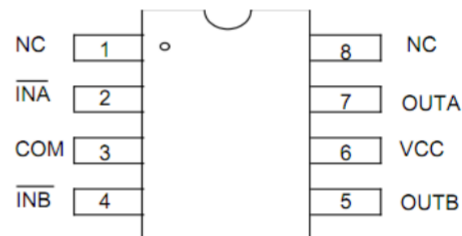
### Applications

- DC-to-DC Converters
- Desktop PC Power
- Switch-Mode Power Supplies
- Companion Gate-Driver Devices for Digital Power Controllers
- Gate Driver for Emerging Wide Band-Gap Power Devices (such as GaN)

### General Description

The device is a compact gate driver that offers superior replacement of NPN and PNP discrete driver (buffer circuit) solutions. driver rated for MOSFETs, IGBTs, and emerging wide-bandgap power devices such as GaN. suitable for high-speed applications. Its asymmetrical 4-A peak source and 8-A peak sink currents boost immunity against parasitic Miller turn on effect. Features including wide input hysteresis and negative input voltage handling enhance transient immunity.

### Pin out (top view)



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### Pin Configurations

Pin	Name	Function
1	NC	N/C No internal connection
2	INA	Channel A Logic Input
3	COM	Ground,Common ground reference for input and output circuits.
4	INB	Channel B Logic Input
5	OUTB	Channel B Output - Sources or sinks current to turn-on or turn-off a discrete MOSFET or IGBT,OUTB INVERTING.
6	VCC	Supply Voltage.
7	OUTA	Channel A Output - Sources or sinks current to turn-on or turn-off a discrete MOSFET or IGBT,OUTA INVERTING.
8	N/A	N/C No internal connection

### Absolute Maximum Ratings (Note1)

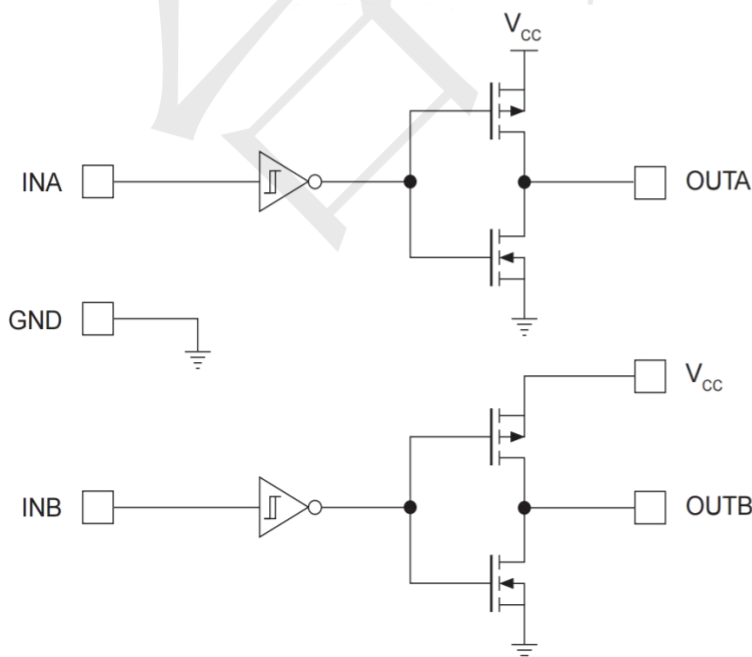
Description	Min	Max	Unit
Supply Voltage, VDD	-0.3	18	V
Output Voltage, OUT	-0.3	18	V
Input, IN	-6.0	18	V
Output continuous source current	0.3		A
Output continuous sink current	0.6		A
Output pulsed (0.5us) source current	4.0		A
Output pulsed (0.5us) sink current	8.0		A
Junction Temperature	125		°C
Storage Temperature	-40	150	°C
Lead Temperature (Soldering, 10s)	300		°C

**Note 1:** Absolute Maximum Ratings are those values beyond which the life of a device may be impaired.

### Recommended Operating Conditions

Description	Min	Max	Unit
Supply Voltage, VDD	4.5	15	V
Input, IN	-5.0	15	V
Operating Junction Temperature	0	125	°C

### Internal Block Diagram



### OUTPUT LOGIC

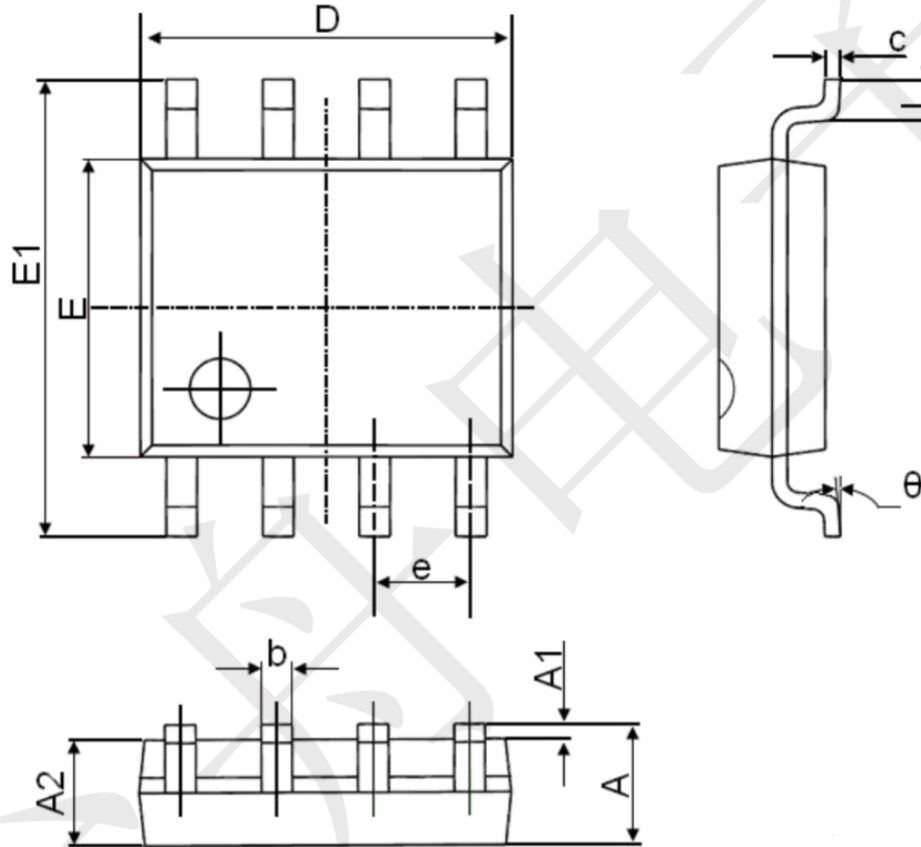
IN <sub>x</sub>	OUT <sub>x</sub>
0	1
1	0

### Electrical Characteristics (VDD=12V, T<sub>J</sub>=25°C, unless otherwise specified)

Parameter	Symbol	Test Conditions	Min	Typ	Max	Units
Startup Current	I <sub>START</sub>	VDD=3.4V, IN+=VDD, IN-=GND	40	100	160	uA
		VDD=3.4V, IN+=IN-=GND	25	75	145	
		VDD=3.4V, IN+=GND, IN-=VDD	20	60	115	
VDD Start Threshold	V <sub>ON</sub>		3.9	4.2	4.5	V
VDD OFF Threshold	V <sub>OFF</sub>		3.0	3.5	4.0	V
VDD Hysteresis	V <sub>HYS</sub>			0.7		V
Input Signal High Threshold	V <sub>H(IN)</sub>		--	2.4	2.6	V
Input Signal Low Threshold	V <sub>L(IN)</sub>		1.0	1.2	--	V
Source Peak Current	I <sub>PSRC</sub>	C <sub>load</sub> =0.22uF, f <sub>S</sub> =1kHz	--	-4	--	A
Sink Peak Current	I <sub>PSNK</sub>	C <sub>load</sub> =0.22uF, f <sub>S</sub> =1kHz	--	8	--	A
High Output Voltage	V <sub>OH</sub>	VDD=12V, I <sub>OUTH</sub> = -10mA	--	50	90	mV
		VDD=4.5V, I <sub>OUTH</sub> = -10mA	--	60	130	mV
Low Output Voltage	V <sub>OL</sub>	VDD=12V, I <sub>OUTL</sub> = 10mA	--	5	6.5	mV
		VDD=4.5V, I <sub>OUTL</sub> = 10mA	--	5.5	10	mV
Output Pullup Resistance	R <sub>OH</sub>	VDD=12V, I <sub>OUTH</sub> = -10mA	--	5	7.5	Ω
		VDD=4.5V, I <sub>OUTH</sub> = -10mA	--	5	11	Ω
Output Resistance Pulllow	R <sub>OL</sub>	VDD=12V, I <sub>OUTL</sub> = 10mA	--	0.375	0.65	Ω
		VDD=4.5V, I <sub>OUTL</sub> = 10mA	--	0.45	0.75	Ω
Rise Time	T <sub>RISE</sub>	VDD=12V, C <sub>LOAD</sub> =1.8nF, OUTH, OUTL tied together	--	8	12	nS
		VDD=4.5V, C <sub>LOAD</sub> =1.8nF, OUTH, OUTL tied together	--	16	22	nS
Fall Time	T <sub>FALL</sub>	VDD=12V, C <sub>LOAD</sub> =1.8nF, OUTH, OUTL tied together	--	7	11	nS
		VDD=4.5V, C <sub>LOAD</sub> =1.8nF, OUTH, OUTL tied together	--	7	11	nS
IN+ to output propagation delay	T <sub>DELAY+</sub>	VDD=12V, C <sub>LOAD</sub> =1.8nF, OUTH, OUTL tied together	9	23	33	nS
		VDD=4.5V, C <sub>LOAD</sub> =1.8nF, OUTH, OUTL tied together	9	25	36	nS
IN- to output propagation delay	T <sub>DELAY-</sub>	VDD=12V, C <sub>LOAD</sub> =1.8nF, OUTH, OUTL tied together	9	23	33	nS
		VDD=4.5V, C <sub>LOAD</sub> =1.8nF, OUTH, OUTL tied together	9	29	40	nS

### Package Information

#### SOP-8



Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min.	Max.	Min.	Max.
A	1.350	1.750	0.053	0.069
A1	0.100	0.250	0.004	0.010
A2	1.350	1.550	0.053	0.061
b	0.330	0.510	0.013	0.020
c	0.170	0.250	0.006	0.010
D	4.700	5.100	0.185	0.200
E	3.800	4.000	0.150	0.157
E1	5.800	6.200	0.228	0.244
e	1.270(BSC)		0.050(BSC)	
L	0.400	1.270	0.016	0.050
theta	0°	8°	0°	8°