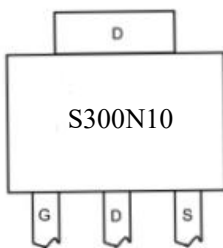
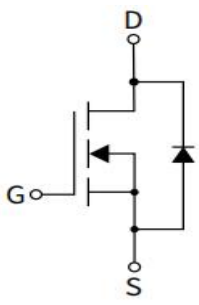




Features <ul style="list-style-type: none"> ➤ Split Gate Trench MOSFET technology ➤ Excellent package for heat dissipation ➤ High density cell design for low $R_{DS(ON)}$ 	<i>Bvdss</i>	<i>Rdson</i>	<i>ID</i>
	100V	2mΩ	300A
Package		Application	
 <p>Marking and pin assignment</p>		<ul style="list-style-type: none"> ➤ DC-DC Converters ➤ Synchronous-rectification applications ➤ Power management functions 	
		 <p>Schematic diagram</p>	

RoHS

Package Marking and Ordering Information

Device Marking	Device	Device Package	Quantity
S300N10	S300N10H	TO247	50

Absolute Maximum Ratings ($T_C=25^\circ\text{C}$ unless otherwise specified)

Parameter	Symbol	Value	Unit
Drain-Source Voltage	V_{DS}	100	V
Gate-Source Voltage	V_{GS}	± 20	V
Continuous Drain Current, $V_{GS}@10V^1$	I_D	$T_C=25^\circ\text{C}$	300
		$T_C=100^\circ\text{C}$	163
Pulsed Drain Current ²	I_{DM}	1028	A
Single Pulse Avalanche Energy ³	EAS	583	mJ
Power Dissipation	$T_C=25^\circ\text{C}$	P_D	379
Operating junction and storage temperature	T_J, T_{STG}	-55 ~ 150	$^\circ\text{C}$
Maximum Temperature for Soldering	T_L	-	$^\circ\text{C}$

Thermal Resistance Ratings

Parameter	Symbol	Value	Unit
Thermal Resistance Junction-Case ¹	$R_{\theta JC}$	0.33	$^\circ\text{C}/\text{W}$
Thermal Resistance, Junction -to-Ambient ¹	$R_{\theta JA}$	59	$^\circ\text{C}/\text{W}$



Ordering Information

Ordering Number	Package	Pin Assignment			Packing
Halogen Free		G	D	S	
HLS300N10H	TO247	1	2	3	Tube

Electrical Characteristics (T_J=25°C unless otherwise noted)

Parameter	Symbol	Test Conditions	Min.	Typ.	Max.	Unit
Drain-Source Breakdown Voltage	V _{(BR)DSS}	V _{GS} =0V, I _D =250μA	100	-	-	V
Drain to Source Leakage Current	I _{DSS}	V _{DS} =100V, V _{GS} =0V	-	-	1	μA
Gate to Source Forward Leakage	I _{GSS}	V _{GS} =±20V, V _{DS} =0V	-	-	±100	nA
Gate-Threshold Voltage	V _{GS(th)}	V _{DS} =V _{GS} , I _D =250μA	2	3	4	V
Drain-Source On-Resistance ²	R _{DS(on)}	V _{GS} =10V, I _D =20A	-	2	2.6	mΩ
Input Capacitance	C _{iss}	V _{DS} =50V, V _{GS} =0V, f=1MHz	-	9030	-	pF
Output Capacitance	C _{oss}		-	1505	-	
Reverse Transfer Capacitance	C _{rss}		-	40	-	
Total Gate Charge	Q _g	V _{GS} =10V, V _{DS} =50V, I _D =20A	-	150	-	nC
Gate-Source Charge	Q _{gs}		-	32.5	-	
Gate-Drain Charge	Q _{gd}		-	49	-	
Turn-On Delay Time	t _{d(on)}	V _{GS} =10V, V _{DD} =50V, R _G =3Ω, I _D =20A	-	27	-	ns
Rise Time	t _r		-	78.5	-	
Turn-Off Delay Time	t _{d(off)}		-	110	-	
Fall Time	t _f		-	86	-	
Diode Forward Current ^{1,4}	I _S	V _G =V _D =0V, Force Current	-	-	300	A
Pulsed Source Current ^{2,4}	I _{SM}		-	-	1000	
Diode Forward Voltage	V _{SD}	I _S =1A, V _{GS} =0V	-	-	-1.2	V
Reverse Recovery time	T _{rr}	I _F =20A, dI/dt=100A/μs	-	90	-	ns
Reverse Recovery Charge	Q _{rr}		-	175	-	nC
Forward Transconductance	g _{fs}	V _{DS} =10V, I _D =20A	-	76	-	S
Gate Resistance	R _g	V _{DS} =0V, V _{GS} =0V, f=1MHz	-	2.3	-	Ω

Note :

- 1.The data tested by surface mounted on a 1 inch² FR-4 board with 20Z copper.
- 2.The data tested by pulsed , pulse width ≤ 300us , duty cycle ≤ 2%.
- 3.The EAS data shows Max. rating . The test condition is T_J=25°C, V_{DD}=50V, V_{GS}=10V, L=0.4mH, I_{AS}=54A.
- 4.The power dissipation is limited by 150°C junction temperature.
- 5.The data is theoretically the same as I_D and I_{DM} , in real applications , should be limited by total power dissipation.



Typical Performance Characteristics

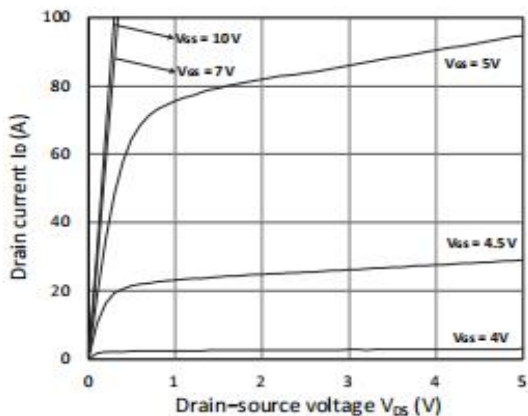


Figure 1. Output Characteristics

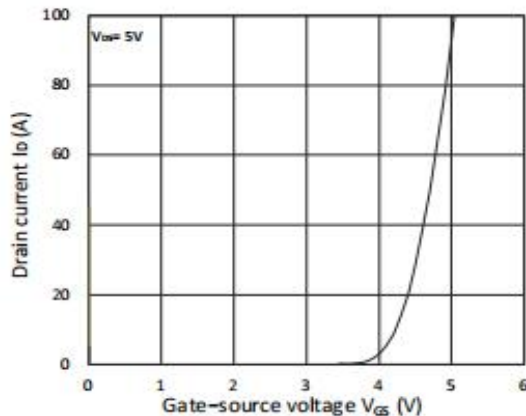


Figure 2. Transfer Characteristics

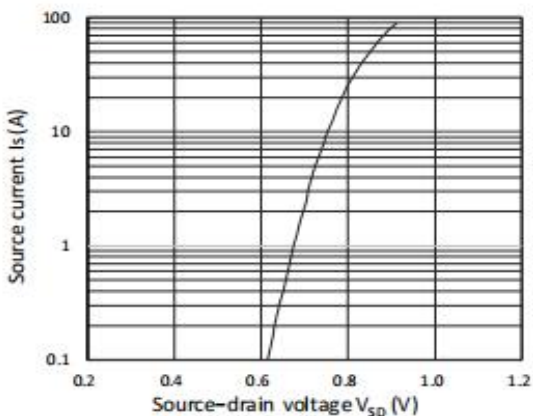


Figure 3. Forward Characteristics of Reverse

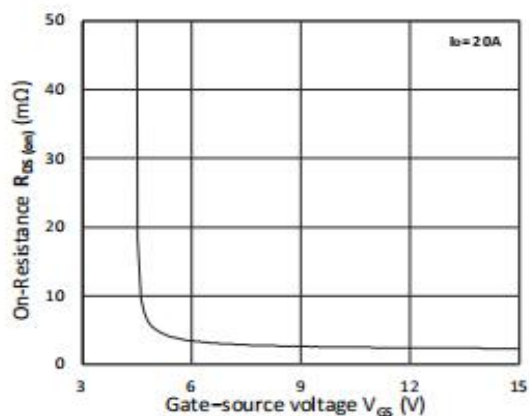


Figure 4. $R_{DS(on)}$ vs. V_{GS}

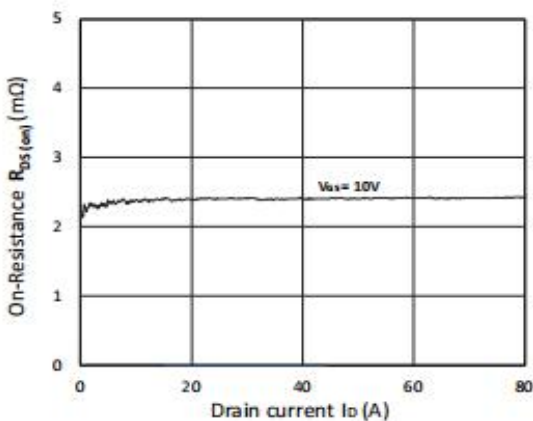


Figure 5. $R_{DS(on)}$ vs. I_D

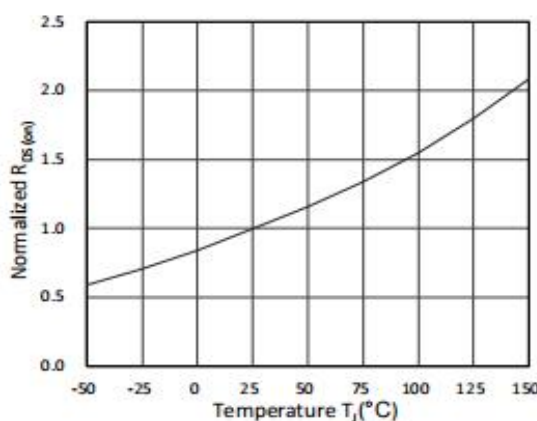


Figure 6. Normalized $R_{DS(on)}$ vs. Temperature

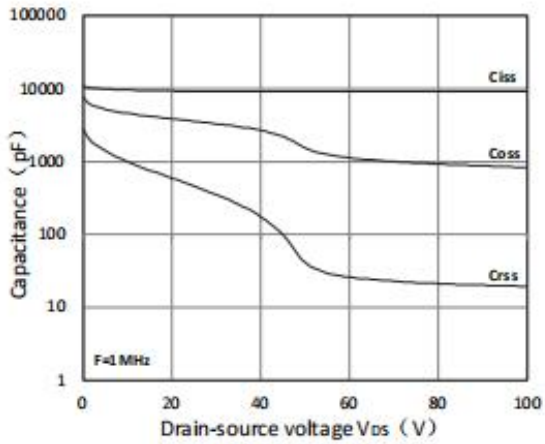


Figure 7. Capacitance Characteristics

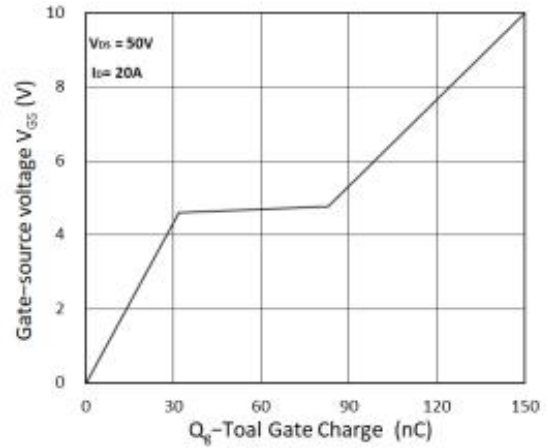


Figure 8. Gate Charge Characteristics

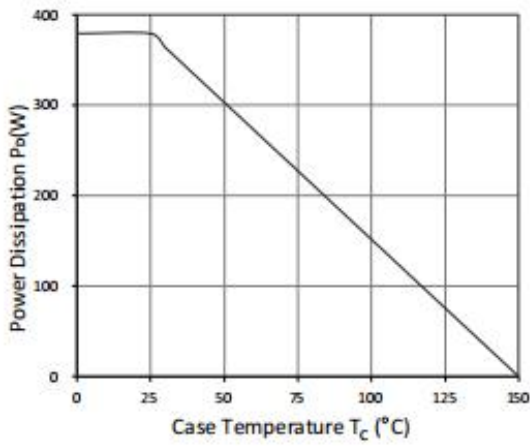


Figure 9. Power Dissipation

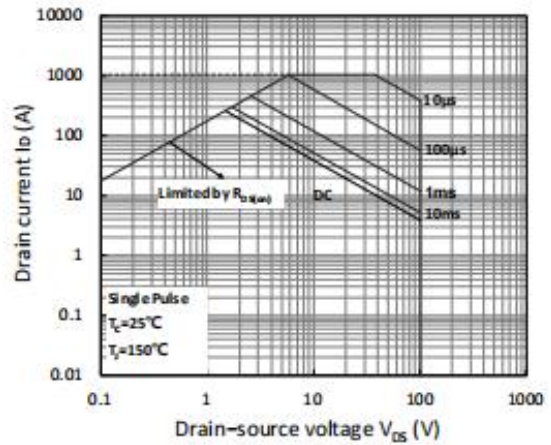


Figure 10. Safe Operating Area

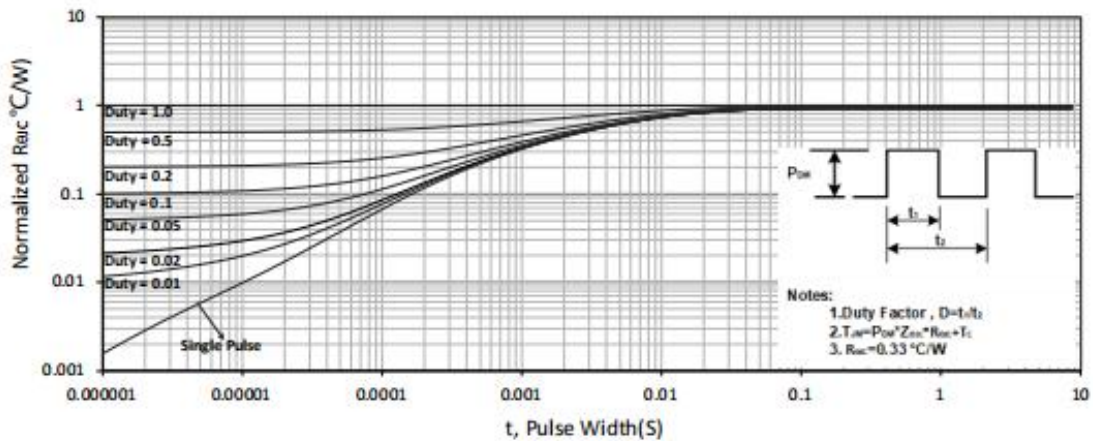


Figure 11. Normalized Maximum Transient Thermal Impedance



Test Circuit and Waveform

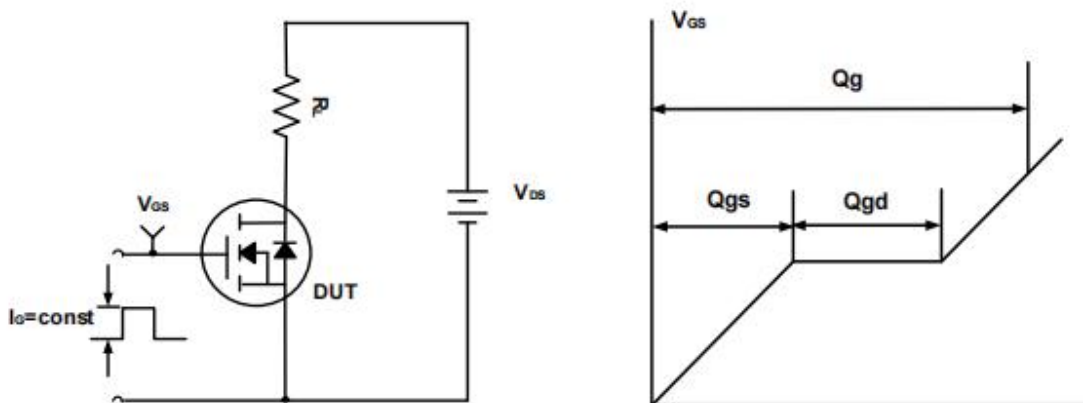


Figure A. Gate Charge Test Circuit & Waveforms

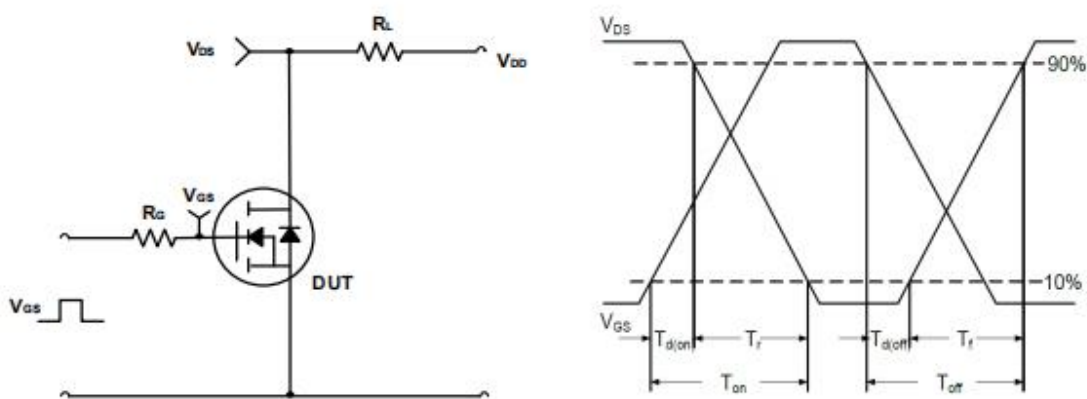
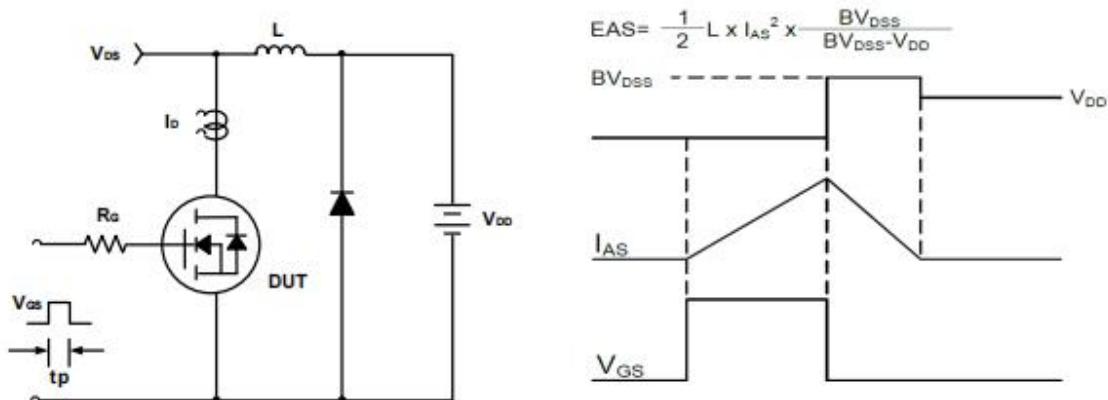


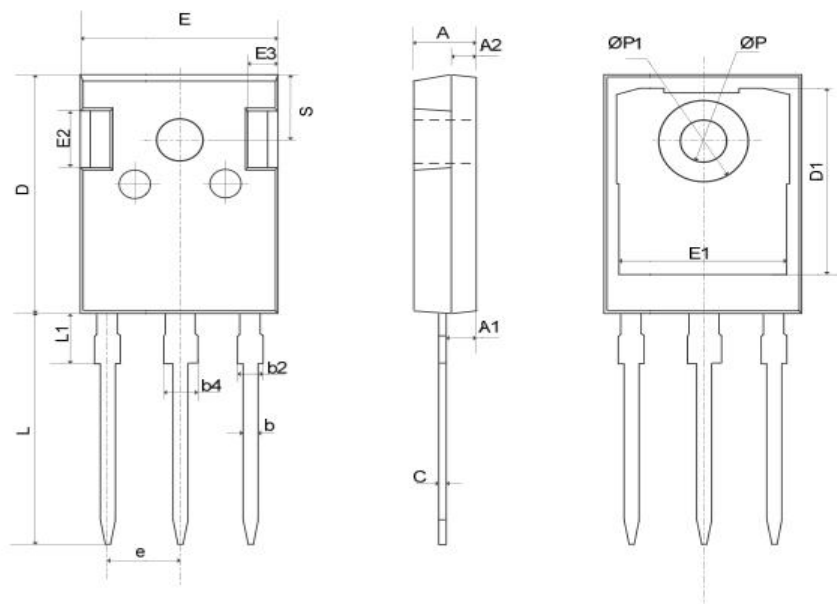
Figure B. Switching Test Circuit & Waveforms





Package Dimensions TO247

COMMON DIMENSIONS



SYMBOL	MM	
	MIN	MAX
A	4.80	5.20
A1	2.21	2.61
A2	1.85	2.15
b	1.11	1.36
b2	1.91	2.21
b4	2.91	3.21
c	0.51	0.75
D	20.70	21.30
D1	16.25	16.85
E	15.50	16.10
E1	13.00	13.60
E2	4.80	5.20
E3	2.30	2.70
e	5.44BSC	
L	19.62	20.22
L1	—	4.30
ØP	3.40	3.80
ØP1	—	7.30
S	6.15BSC	



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