
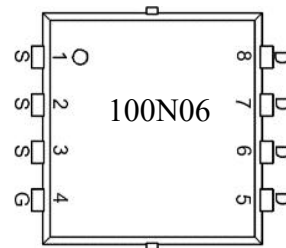
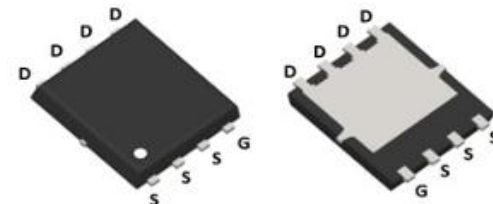
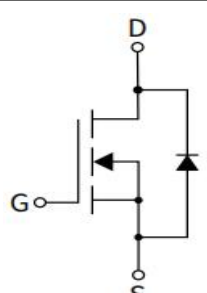




<b>Features</b> ➤ Split Gate Trench MOSFET technology ➤ Excellent package for heat dissipation ➤ High density cell design for low $R_{DS(ON)}$	<b><math>B_{vds}</math></b>	<b><math>R_{dson}</math></b>	<b><math>I_D</math></b>
	<b>65V</b>	<b>3.7mΩ</b>	<b>100A</b>
	<b>Application</b> ➤ DC-DC converter ➤ Power management functions ➤ Synchronous-rectification applications		
<b>Package</b>	  		
	Marking and pin assignment	PDFN5x6-8L top view	Schematic diagram

### Package Marking and Ordering Information

Device Marking	Device	Device Package	Quantity
100N06	S100N06HF	PDFN5x6-8L	5000

### Absolute Maximum Ratings ( $T_C=25^\circ\text{C}$ unless otherwise specified)

Parameter	Symbol	Limit	Unit
Drain-Source Voltage	$V_{DS}$	65	V
Gate-Source Voltage	$V_{GS}$	$\pm 20$	V
Continuous Drain Current	$T_C=25^\circ\text{C}$	100	A
	$T_C=100^\circ\text{C}$	61	A
Pulsed Drain Current <sup>1</sup>	$I_{DM}$	380	A
Single Pulsed Avalanche Energy <sup>2</sup>	EAS	80	mJ
Power Dissipation	$P_D$	73.5	W
Junction Temperature	$T_J$	-55 ~ 150	$^\circ\text{C}$
Storage Temperature	$T_{STG}$	-55 ~ 150	$^\circ\text{C}$

### Thermal Resistance Ratings

Parameter	Symbol	Typ.	Max.	Unit
Thermal Resistance, Junction-to-Ambient <sup>3</sup>	$R_{\theta JA}$	--	51	$^\circ\text{C}/\text{W}$
Thermal Resistance, Junction-to-Case	$R_{\theta JC}$	--	1.7	$^\circ\text{C}/\text{W}$



## Ordering Information

Ordering Number	Package	Pin Assignment			Packing
Halogen Free		G	D	S	
HLS100N06HF	PDFN5x6-8L	4	5,6,7,8	1,2,3	Tape Reel

Electrical Characteristics ( $T_J=25^{\circ}\text{C}$  unless otherwise specified)

Parameter	Symbol	Condition	Min	Typ	Max	Unit
Drain-Source Breakdown Voltage	$V_{DS}$	$V_{GS}=0V, I_D=250\mu A$	65	-	-	V
Zero-Gate Voltage Drain Current	$I_{DSS}$	$V_{DS}=65V, V_{GS}=0V$	-	-	1	$\mu A$
Gate-Source Forward Leakage	$I_{GSS}$	$V_{GS}=\pm 20V$	-	-	100	nA
Gate Threshold Voltage	$V_{GS(th)}$	$V_{GS}=V_{DS}, I_D=250\mu A$	2	2.9	4	V
Drain-Source On-State Resistance <sup>4</sup>	$R_{DS(on)}$	$V_{GS}=10V, I_D=20A$	-	3.7	5	m $\Omega$
Forward Transconductance <sup>4</sup>	$g_{fs}$	$V_{DS}=10V, I_D=20A$	-	89	-	S
Input Capacitance	$C_{iss}$	$V_{DS}=30V, V_{GS}=0V,$ $f=1\text{MHz}$	-	1673	-	pF
Output Capacitance	$C_{oss}$		-	773	-	
Reverse Transfer Capacitance	$C_{rss}$		-	46.8	-	
gate resistance	$R_g$	$f=1.0\text{MHz}$	-	1.8	-	$\Omega$
Turn-on Delay Time	$T_{d(on)}$	$V_{GS}=10V, V_{DD}=30V,$ $R_G=3\Omega, I_D=20A$	-	11.2	-	nS
Turn-on Rise Time	$t_r$		-	8.2	-	
Turn-Off Delay Time	$T_{d(off)}$		-	19.6	-	
Turn-Off Fall Time	$T_f$		-	6.2	-	
Total Gate Charge	$Q_g$	$V_{DS}=30V, V_{GS}=10V,$ $I_D=20A$	-	28.5	-	nC
Gate-Source Charge	$Q_{gs}$		-	7.8	-	
Gate-Drain Charge	$Q_{gd}$		-	8.4	-	
Diode Forward Voltage <sup>4</sup>	$V_{SD}$	$V_{GS}=0V, I_S=20A$	-	-	1.2	V
Continuous Diode Forward Current	$I_S$	-	-	-	100	A
Reverse Recovery Time	$t_{rr}$	$I_F=20A, di/dt = 100A/\mu s$	-	50	-	nS
Reverse Recovery Charge	$Q_{rr}$		-	20	-	nC

Notes:

1. Repetitive rating, pulse width limited by junction temperature  $T_{J(MAX)}=150^{\circ}\text{C}$
2. The EAS data shows Max. rating . The test condition is  $V_{DD}=25V, V_{GS}=10V, L=0.1\text{mH}, I_{AS}=40A$ .
3. The data tested by surface mounted on a 1 inch<sup>2</sup> FR-4 board with 2OZ copper, The value in any given application depends on the user's specific board design.
4. The data tested by pulsed , pulse width  $\leq 300\mu s$  , duty cycle  $\leq 2\%$ .
5. This value is guaranteed by design hence it is not included in the production test.



Typical Characteristics

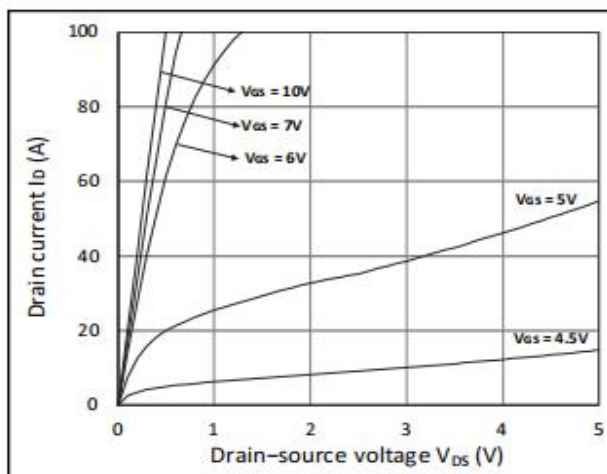


Figure 1. Output Characteristics

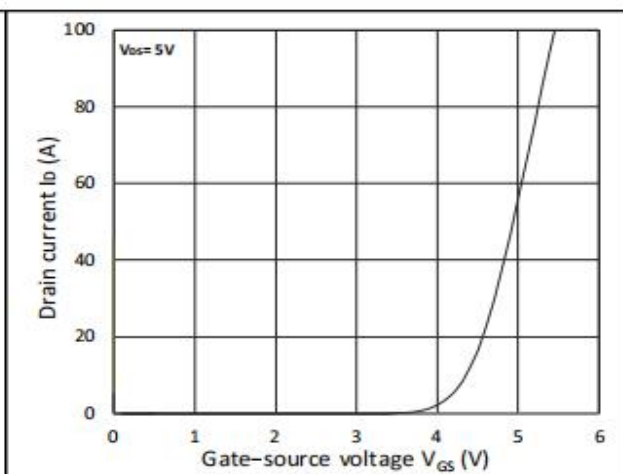


Figure 2. Transfer Characteristics

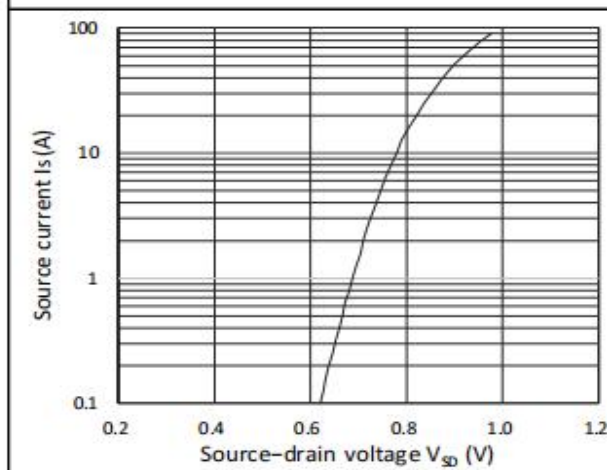


Figure 3. Forward Characteristics of Reverse

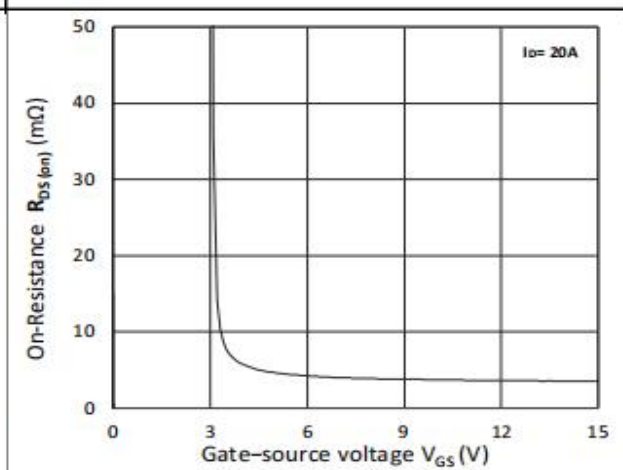


Figure 4.  $R_{DS(on)}$  vs.  $V_{GS}$

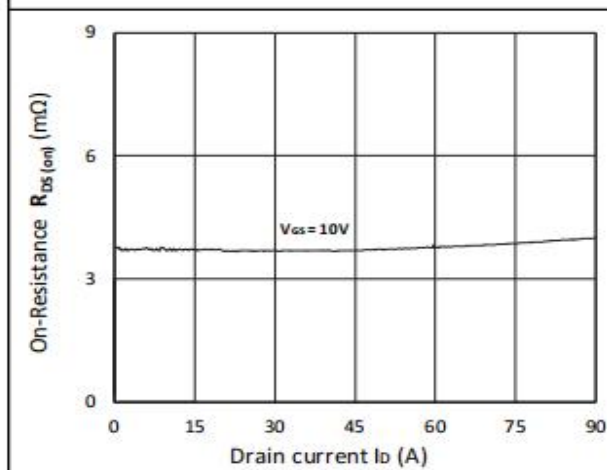


Figure 5.  $R_{DS(on)}$  vs.  $I_D$

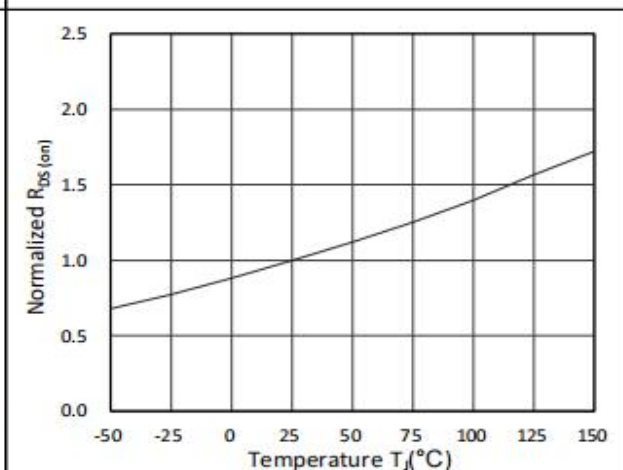


Figure 6. Normalized  $R_{DS(on)}$  vs. Temperature

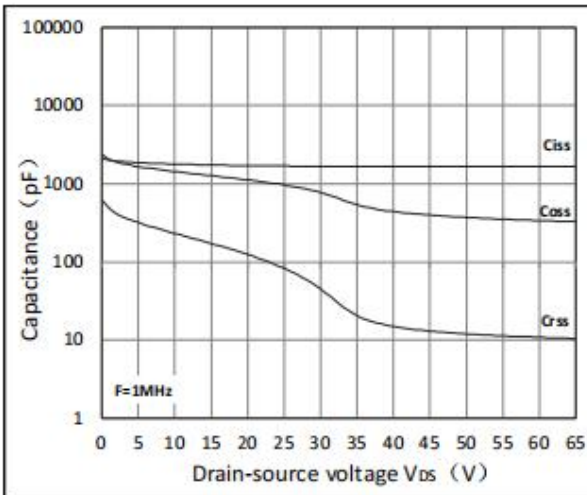


Figure 7. Capacitance Characteristics

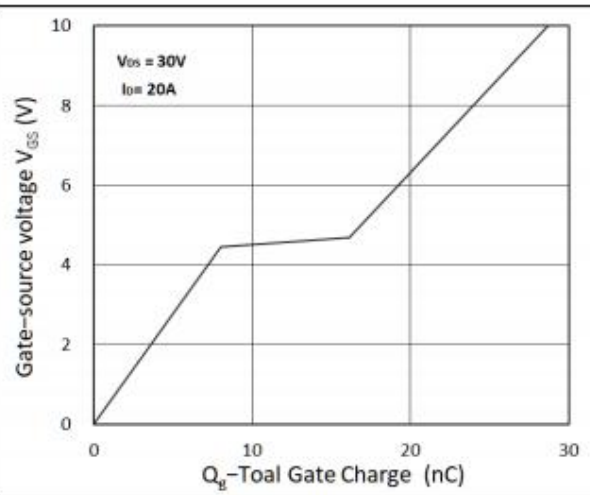


Figure 8. Gate Charge Characteristics

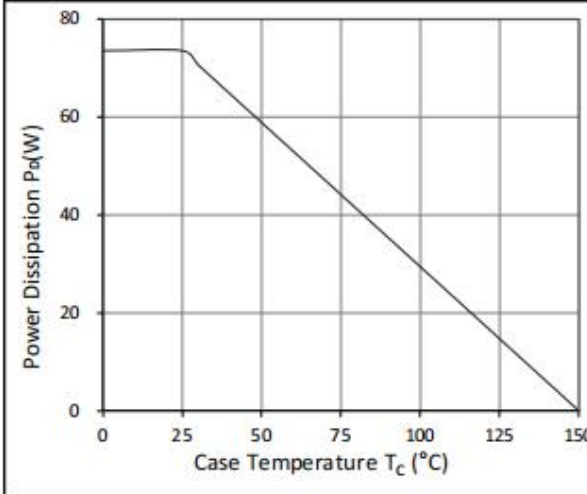


Figure 9. Power Dissipation

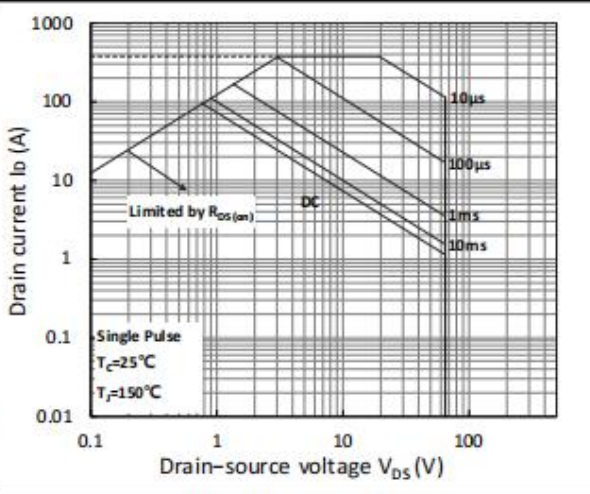


Figure 10. Safe Operating Area

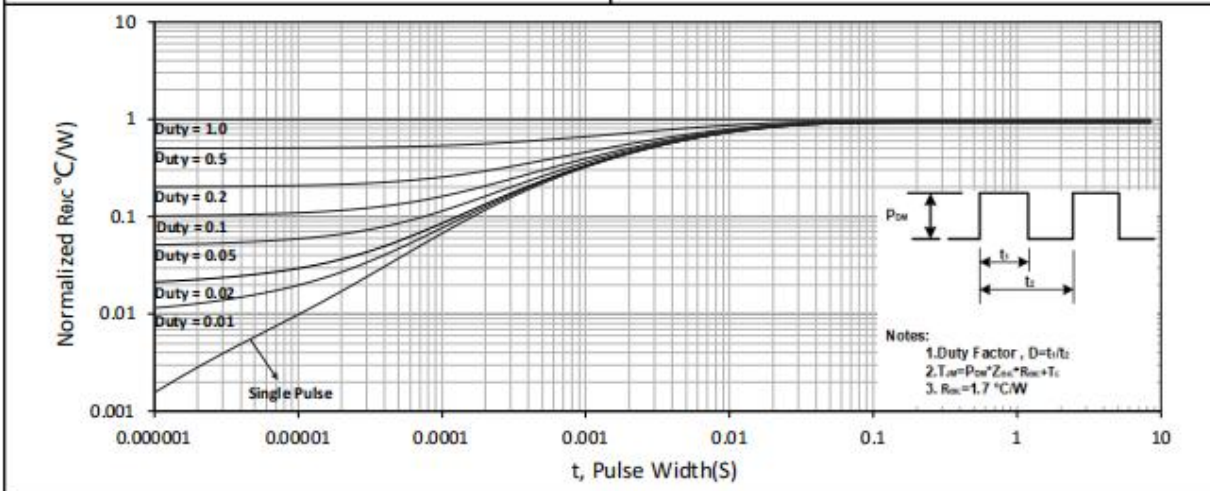


Figure 11. Normalized Maximum Transient Thermal Impedance



Test Circuit

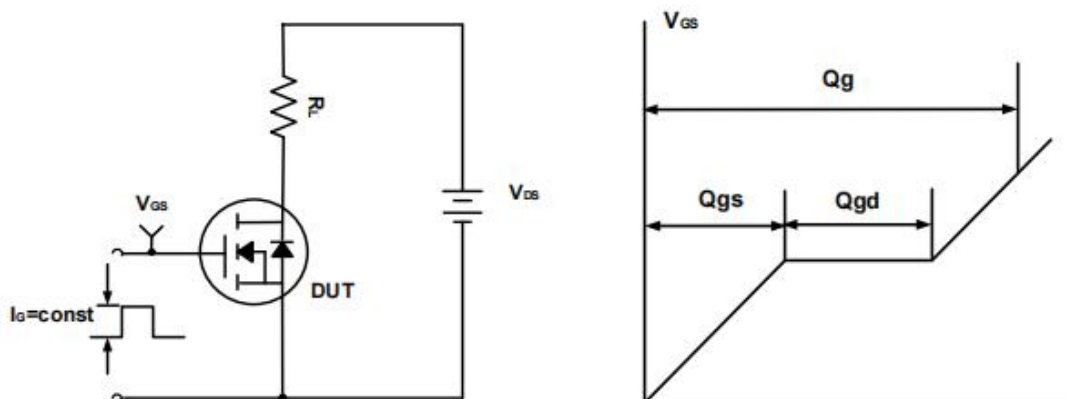


Figure A. Gate Charge Test Circuit & Waveforms

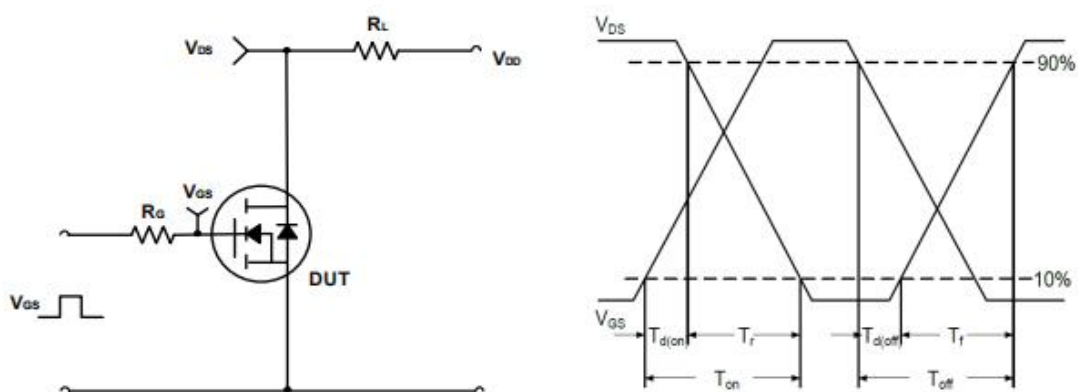


Figure B. Switching Test Circuit & Waveforms

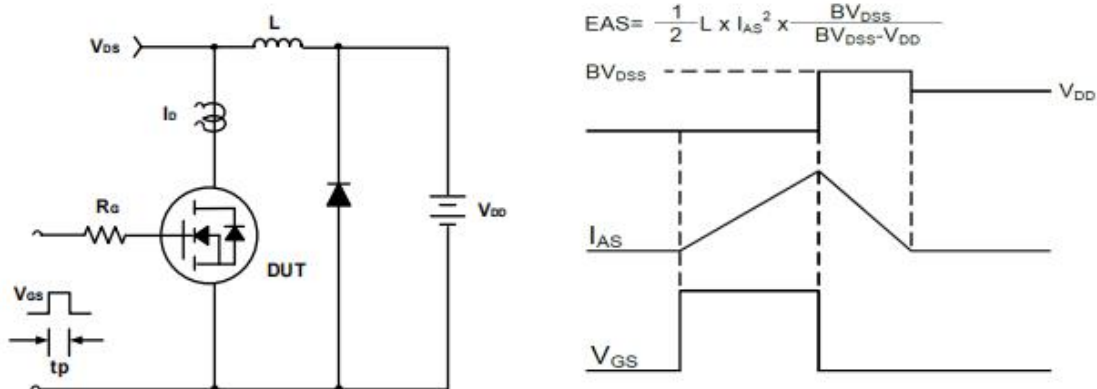
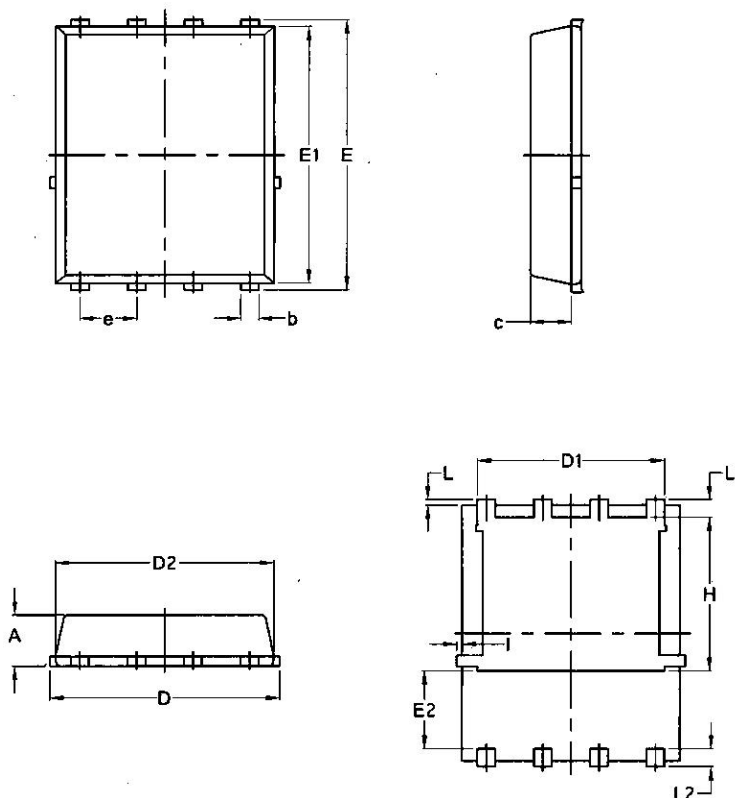


Figure C. Unclamped Inductive Switching Circuit & Waveforms



Package Dimensions PDFN5x6-8L



Symbol	Common			
	mm		Inch	
	Min	Max	Min	Max
A	1.03	1.17	0.0406	0.0461
b	0.34	0.48	0.0134	0.0189
c	0.824	0.0970	0.0324	0.082
D	4.80	5.40	0.1890	0.2126
D1	4.11	4.31	0.1618	0.1697
D2	4.80	5.00	0.1890	0.1969
E	5.95	6.15	0.2343	0.2421
E1	5.65	5.85	0.2224	0.2303
E2	1.60	/	0.0630	/
e	1.27 BSC		0.05 BSC	
L	0.05	0.25	0.0020	0.0098
L1	0.38	0.50	0.0150	0.0197
L2	0.38	0.50	0.0150	0.0197
H	3.30	3.50	0.1299	0.1378
I	/	0.18	/	0.0070



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