

Features

- Drives both High-side and Low-side N-channel MOSFET with Independent Inputs
- 3.5-A Peak Output Source and Sink Current Capability
- Max Bootstrap Supply Voltage up to 120 V
- Wide Supply Rail from 7 V to 20 V
- 6.5-V Typical under Voltage Lockout
- Input Interlock
- Enable and Disable Features
- Integrated Bootstrap Diode
- TTL/CMOS Compatible Input, -10-V to 20-V Input Capability
- 27-ns Propagation Delay Times
- 2-ns Delay Matching
- 8.7-ns Rise Time and 5.9-ns Fall Time with 1800-pF Load
- 15-ns Input Deglitching Time
- 20-ns Minimum Pulse Width
- Supply Rail Under-Voltage Lockout (UVLO)
- Operation from -40°C to 150°C
- Available in SOP8 and DFN3X3-10 Packages

Applications

- Power Supplies for Telecom, Datacom, and Datacenters
- Half-bridge and Full-bridge Converters
- Push-pull Converters
- High-voltage Synchronous-Buck Converters
- 48-V Fan Driver

Description

The TPM27282 MOSFET drivers are pin-to-pin compatible with industrial-standard 100-V half-bridge drivers. They are designed to control two N-channel MOSFETs in half-bridge or synchronous buck configurations. They have high peak currents at 3.5 A for both pull-up and pull-down, and low output resistance at 1 Ω . This helps to drive bigger MOSFETs with less switching loss. They can handle -10V DC input directly, which is stronger and lets them connect to gate-drive transformers without external diodes. The drivers work with any supply voltage up to 20 V. The device has an independent enable pin and an interlock feature.

Both high-side and low-side driver stages have a 6.5-V or 5.8-V under-voltage lockout that forces outputs low if the supply voltage drops below a set threshold. An integrated bootstrap diode eliminates the need for an external diode in many setups, saving space and reducing costs. The TPM27282 comes in with DFN3X3-10 suitable for high-density designs.

Typical Application Circuit

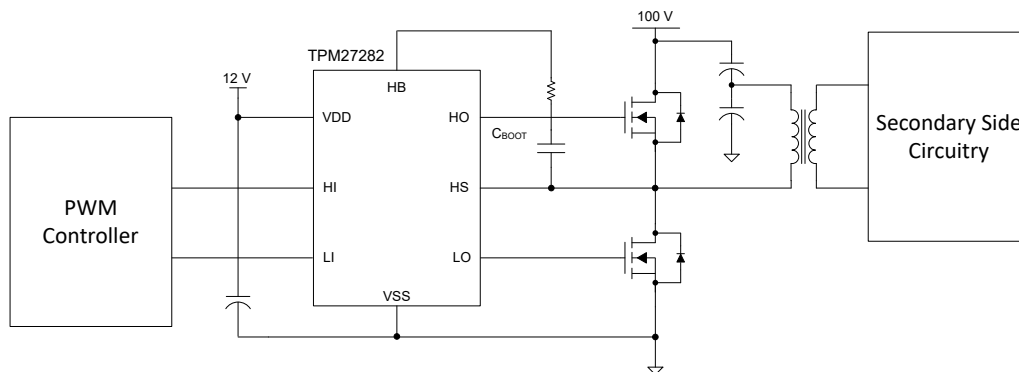


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Revision History

Date	Revision	Notes
2025-05-22	Rev.A.0	Initial release.
2025-02-09	Rev.A.1	<ul style="list-style-type: none">• Updated the application diagram.• Updated the Bootstrap Diode description in the Feature Description. The actual product remains unchanged. Added the DFN4X4-8 package.

Pin Configuration and Functions

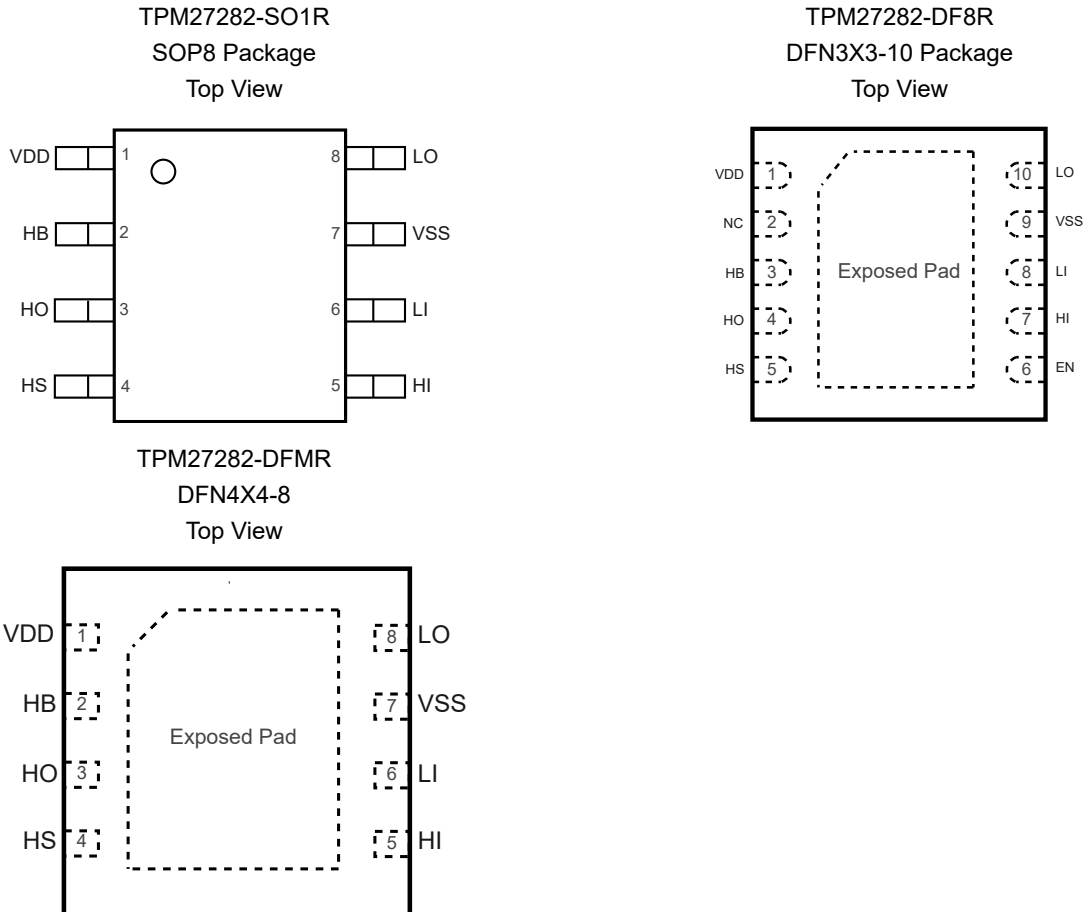


Table 1. Pin Functions

Pin No.			Name	I/O	Description
SOP8	DFN4X4-8	DFN3X3-10			
1	1	1	VDD	P	The low-side gate driver in the TPM27282 requires a positive supply, which should be decoupled to the VSS with a typical capacitor value of 1 μ F to ensure stable operation. If an external boot diode is used, its anode should be connected to this pin.
-	-	2	NC	P	Not connected
2	2	3	HB	P	The high-side bootstrap supply in the TPM27282 includes an integrated bootstrap diode with an external bootstrap capacitor. Attach the positive terminal of this capacitor to the HB pin, with a typical recommendation of 0.1 μ F for the HB bypass capacitor, mainly determined by characteristics of the high-side MOSFET. When an external bootstrap diode is used, connect its cathode to this pin. 3PEAK recommends using an external bootstrap in the case of high input voltage or high switching frequency.

120-V Supply, 3.5-A Peak, High-frequency HS and LS Gate Driver

Pin No.			Name	I/O	Description
SOP8	DFN4X4-8	DFN3X3-10			
3	3	4	HO	O	The high-side output of the TPM27282 should be connected directly to the gate of the high-side power MOSFET or to one terminal of an external gate resistor if used.
4	4	5	HS	P	The high-side source connection on the TPM27282 should be connected to the source of the high-side power MOSFET. The negative side of the bootstrap capacitor should be attached to this pin.
-	-	6	EN		Device enable input with internal pull-down. Active high, when the pin is high, the device is enabled; when the pin is low or floating, the device is disabled. 3PEAK recommends adding a 1-nF capacitor to noisy systems.
5	5	7	HI	I	High-side driver logic input, TTL compatible. Floating logic low.
6	6	8	LI	I	Low-side driver logic input, TTL compatible. Floating logic low.
7	7	9	VSS	GND	Supply ground.
8	8	10	LO	O	Low-side driver output. The low-side output of the TPM27282 should be connected directly to the gate of the low-side power MOSFET or to one terminal of an external gate resistor if used.
n/a	n/a	Exposed Pad	EP	G	Exposed Pad. Recommend connecting to GND.

Specifications

Absolute Maximum Ratings

Over operating free-air temperature unless otherwise noted ⁽¹⁾

Parameter		Min	Max	Unit
VDD	Supply Voltage	-0.3	20	V
EN, HI, LI	Input Voltages	-10	20	V
LO (DC)	Output Voltage	-0.3	(V _{DD}) + 0.3	V
LO (Pulse < 100 ns) ⁽³⁾	Output Voltage	-2	(V _{DD}) + 0.3	V
HB	Bootstrap Voltage	-0.3	120	V
HB - HS	High-side Voltage	-0.3	26	V
HO (DC)	Output Voltage	(V _{HS}) - 0.3	(V _{HB}) + 0.3	V
HO (Pulse < 100 ns) ⁽³⁾	Output Voltage	(V _{HS}) - 2	(V _{HB}) + 0.3	V
HS (DC)	High-side MOSFET Source Voltage	-8	120	V
HS (Pulse < 300 ns) ⁽³⁾	High-side MOSFET Source Voltage	-12	120	V
HS (Pulse < 100 ns) ⁽³⁾	High-side MOSFET Source Voltage	-18	120	V
T _J	Maximum Operating Junction Temperature ⁽²⁾	-40	150	°C
T _{STG}	Storage Temperature Range	-65	150	°C

(1) Stresses beyond those listed under Absolute Maximum Rating may cause device permanent damage. The device is not guaranteed to function outside of its Recommended Operation Conditions.

(2) The IC includes over-temperature protection to protect the device during overload conditions. Junction temperature will exceed 150°C when over-temperature protection is active. Continuous operation above the specified maximum operating junction temperature will reduce lifetime.

(3) Values are verified by characterization and are not production-tested.

ESD, Electrostatic Discharge Protection

Symbol	Parameter	Condition	Min	Max	Unit
V _{ESD}	Human Body Model ESD (HBM)	ANSI/ESDA/JEDEC JS-001 ⁽¹⁾	-2	+2	kV
	Charged Device Model ESD (CDM)	ANSI/ESDA/JEDEC JS-002 ⁽²⁾	-1	+1	kV

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.

(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

120-V Supply, 3.5-A Peak, High-frequency HS and LS Gate Driver**Recommended Operating Conditions**

Over-operating the free-air temperature range unless otherwise noted

Parameter		Min	Typ	Max	Unit
V _{DD}	Supply Voltage Range	7	12	16	V
V _{EN,HI,LI}	Driver Input Voltage Range	-10		V _{DD} + 0.3	V
V _{HS}	Voltage on HS (DC)	-8		100	V
	Voltage on HS (pulse width < 100 ns)	-12		110	
V _{LO}	Voltage on LO	0		V _{DD} + 0.3	V
V _{HO}	Voltage on HO	V _{HS}		V _{HB} + 0.3	V
V _{SR}	Slew Rate on HS			50	V/ns
V _{HB}	Voltage on HB	V _{HS} +5.5, V _{DD} -1		V _{HS} +16, 115	V
I _{BST}	Transient Internal Bootstrap Diode Current			2	A
T _J	Operating Junction Temperature	-40		150	°C

Thermal Information

Parameter	R _{θJA}	R _{θJC}	Unit
DFN3X3-10	39.86	43.35	°C/W
SOP8	105	51	°C/W

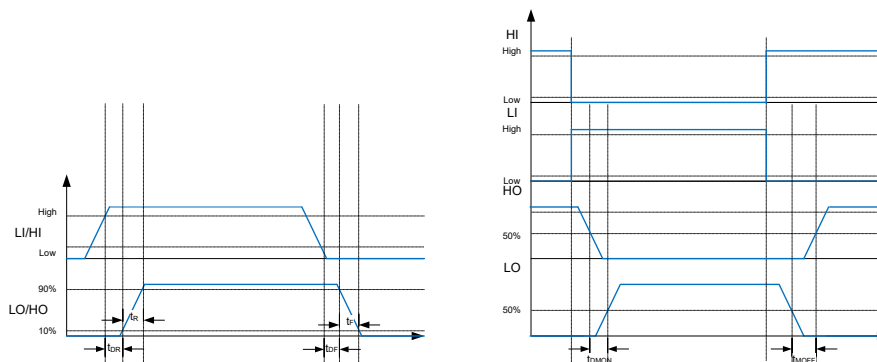
120-V Supply, 3.5-A Peak, High-frequency HS and LS Gate Driver
Electrical Characteristics

All test conditions: $V_{DD} = 12\text{ V}$, $T_J = -40^\circ\text{C} \sim 150^\circ\text{C}$, typical values are tested under 25°C , unless otherwise noted.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
Supply Currents						
I_{DD}	VDD Quiescent Current	$V_{HI} = V_{LI} = 0$	200	334	500	μA
I_{DDO}	VDD Operating Current	$f_{SW} = 500\text{ kHz}$, $C_{Load} = 0\text{ nF}$	1.5	2.46	4.5	mA
I_{HB}	HB Quiescent Current	$V_{HI} = V_{LI} = 0$	90	138	410	μA
I_{HBO}	HB Operating Current	$f_{SW} = 500\text{ kHz}$, $C_{Load} = 0\text{ nF}$	1.6	2.75	3.8	mA
I_{HBS}	HB to VSS Quiescent Current	$V_{HS} = V_{HB} = 110\text{ V}$			1	μA
I_{HBSO}	HB to VSS Operating Current	$f_{SW} = 500\text{ kHz}$, $C_{Load} = 0\text{ nF}$	0.05	0.51	0.95	mA
Inputs						
$V_{HI, LI, R}$	Input Logic High Threshold		1.8	2.1	2.4	V
$V_{HI, LI, F}$	Input Logic Low Threshold		0.8	1.14	1.5	V
$V_{HI, LI, Hys}$	Hysteresis			0.96		V
$V_{EN, R}$	EN Logic High Threshold		1.4	1.71	2	V
$V_{EN, F}$	EN Logic Low Threshold		1.1	1.29	1.45	V
$V_{EN, Hys}$	Hysteresis			0.27		V
R_{PD}	Input Pull Down Resistance		180	250	320	k Ω
Undervoltage Protection (UVLO)						
V_{DDR}	VDD Rising Threshold		6.1	6.55	6.85	V
V_{DDF}	VDD Falling Threshold		5.7	6.15	6.5	V
V_{DDHYS}	VDD Threshold Hysteresis			0.33		V
V_{HBR}	HB Rising Threshold		4.36	4.68	4.93	V
V_{HBF}	HB Falling Threshold		3.95	4.3	4.6	V
V_{HBHYS}	HB Threshold Hysteresis			0.38		V
LO Gate Driver						
V_{LOH}	Output High Voltage	$I_{OUT} = -100\text{ mA}$, $V_{LOH} = V_{DD} - V_{LO}$	50	108	220	mV
V_{LOL}	Output Low Voltage	$I_{OUT} = 100\text{ mA}$	18	36	70	mV
I_{LOSRC}	Output Source Peak Current	$C_{Load} = 10\text{ nF}$, $V_{LO} = 0\text{ V}$		3.5		A
I_{LOSINK}	Output Sink Peak Current	$C_{Load} = 10\text{ nF}$, $V_{LO} = 12\text{ V}$		6.5		A
R_{LOH}	Output Pull High Resistance	$I_{OUT} = -100\text{ mA}$	0.5	1	2.2	Ω
R_{LOL}	Output Pull Low Resistance	$I_{OUT} = 100\text{ mA}$	0.18	0.4	0.7	Ω
HO Gate Driver						
V_{HOH}	Output High Voltage	$I_{OUT} = -100\text{ mA}$, $V_{HOH} = V_{HB} - V_{HO}$	50	104	220	mV
V_{HOL}	Output Low Voltage	$I_{OUT} = 100\text{ mA}$	20	41	75	mV
I_{HOSRC}	Output Source Peak Current	$C_{Load} = 10\text{ nF}$, $V_{HO} = 0\text{ V}$		3.5		A
I_{HOSINK}	Output Sink Peak Current	$C_{Load} = 10\text{ nF}$, $V_{HO} = 12\text{ V}$		6.5		A

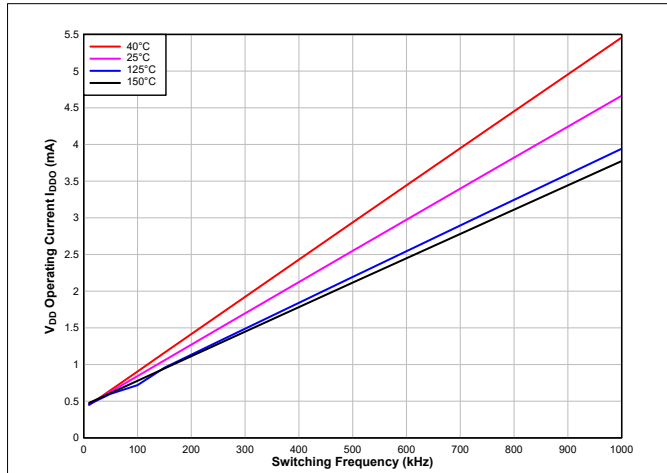
120-V Supply, 3.5-A Peak, High-frequency HS and LS Gate Driver

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
R _{HOH}	Output Pull High Resistance	I _{OUT} = -100 mA	0.5	1	2.2	Ω
R _{HOL}	Output Pull Low Resistance	I _{OUT} = 100 mA	0.2	0.4	0.75	Ω
Bootstrap Diode						
V _{FL}	Low Current Forward Voltage	I _{VDD} - HB = 100 μA	0.8	1.266	2.1	V
V _{FH}	High Current Forward Voltage	I _{VDD} - HB = 100 mA	1.4	1.899	2.8	V
R _D	Dynamic Resistance			3.998	10	Ω
Output Rise and Fall Time						
T _{DLFF}	VLI Falling to VLO Falling	C _{Load} = 10 pF		27.6		ns
T _{DHFF}	VHI Falling to VHO Falling	C _{Load} = 10 pF		29.4		ns
T _{DLRR}	VLI Rising to VLO Rising	C _{Load} = 10 pF		29.2		ns
T _{DHRR}	VHI Rising to VHO Rising	C _{Load} = 10 pF		29.4		ns
T _R	LO, HO Rise Time	C _{Load} = 1.8 nF		10.94		ns
T _F	LO, HO Fall Time	C _{Load} = 1.8 nF		5.63		ns
Delay Matching						
T _{MON}	HO OFF to LO ON			2		ns
T _{MOFF}	LO OFF to HO ON			2		ns
Miscellaneous						
T _{MIN_ON}	Minimum Input Pulse Width			9		ns
T _{IN_Deg glitch}	Input Deglitch Time			15		ns


Figure 1. Timing Diagram

Typical Performance Characteristics

Unless otherwise specified $V_{DD} = V_{HB} = 12\text{ V}$, $V_{HS} = V_{SS} = 0\text{ V}$, No load on outputs



$C_L = 0\text{ F}$, $V_{DD} = V_{HB} = 12\text{ V}$

Figure 2. I_{DD} Operating Current vs. Frequency

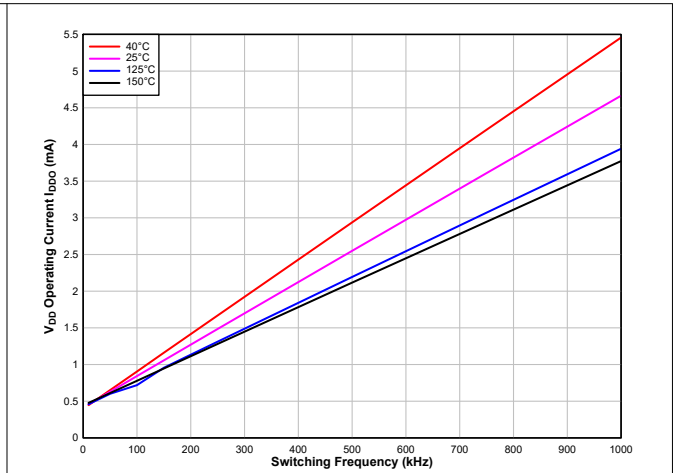


Figure 3. Boot Voltage Operating Current vs. Frequency

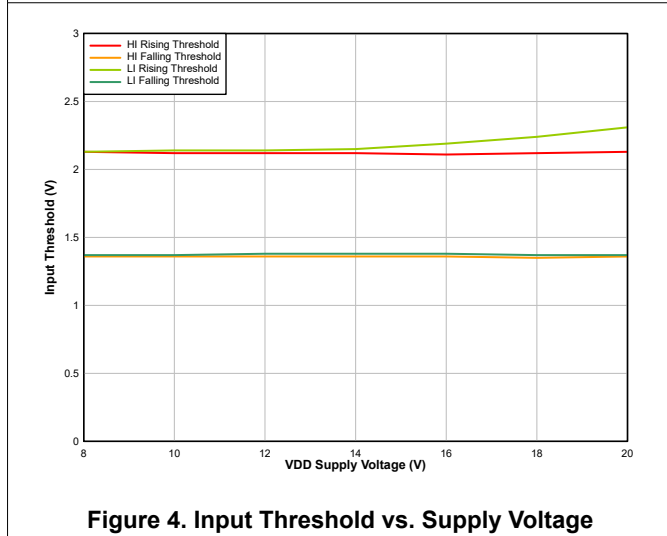


Figure 4. Input Threshold vs. Supply Voltage

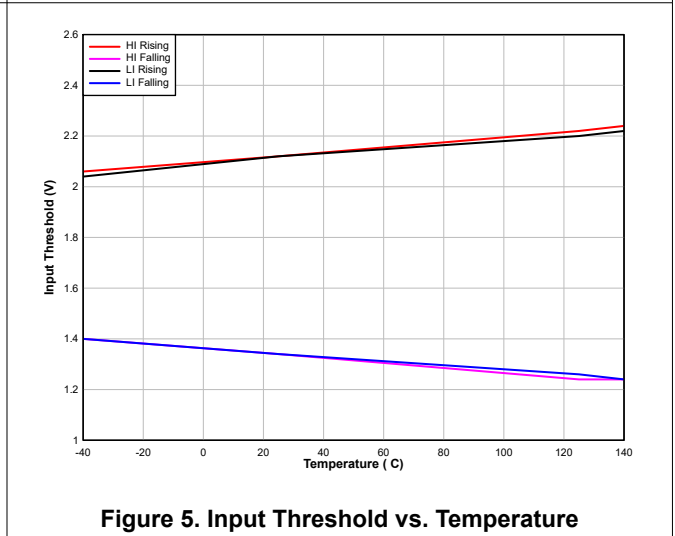


Figure 5. Input Threshold vs. Temperature

120-V Supply, 3.5-A Peak, High-frequency HS and LS Gate Driver

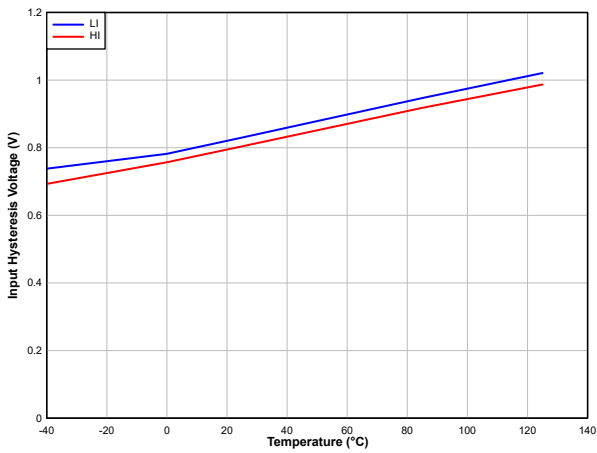


Figure 6. Input Hysteresis vs. Temperature

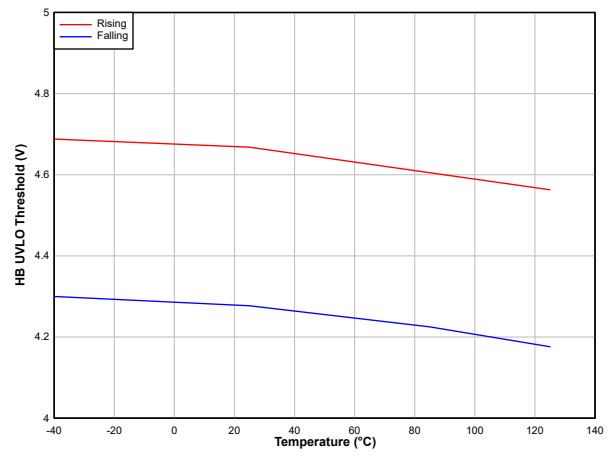
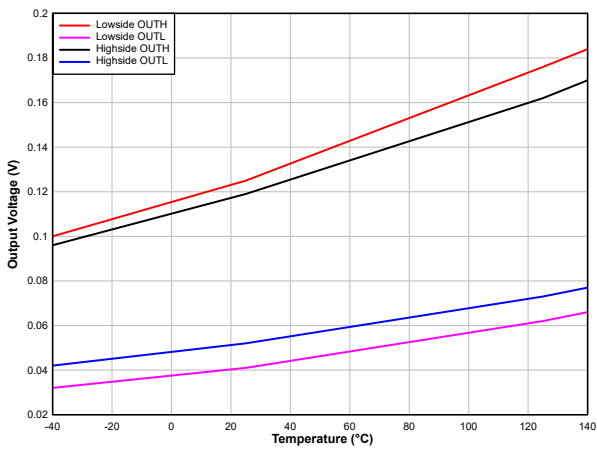


Figure 7. Input Resistance vs. Temperature



$I_{OUT} = 100 \text{ mA}$

Figure 8. Output Voltage vs. Temperature

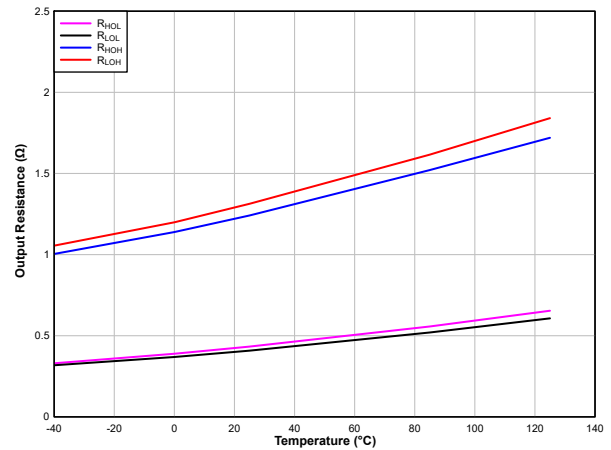


Figure 9. Driver Output Resistance vs. Temperature

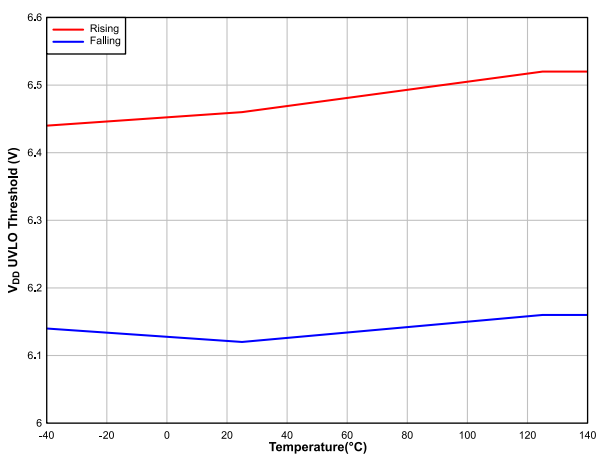


Figure 10. VDD UVLO Threshold vs. Temperature

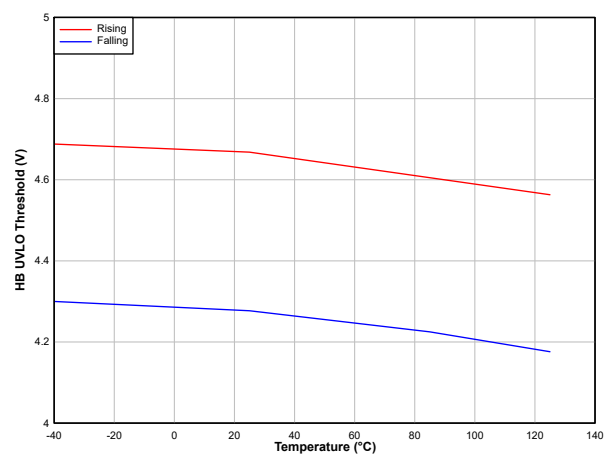


Figure 11. HB UVLO Threshold vs. Temperature

120-V Supply, 3.5-A Peak, High-frequency HS and LS Gate Driver

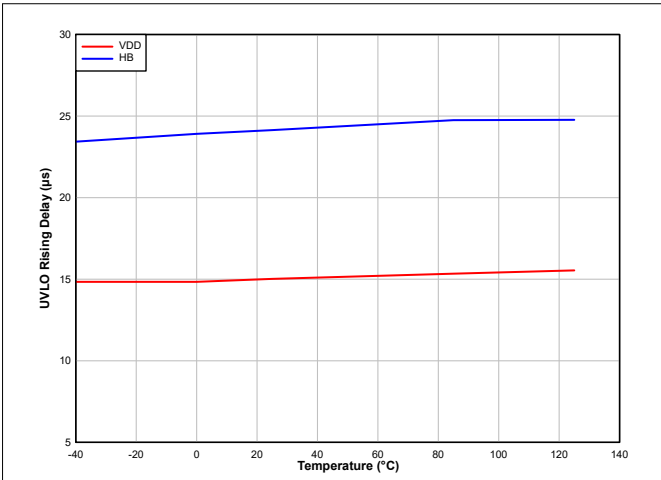


Figure 12. UVLO Rising Delay vs. Temperature

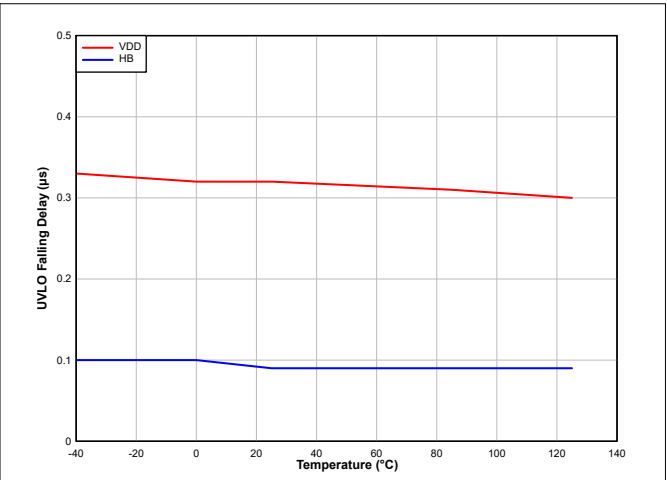


Figure 13. UVLO Falling Delay vs. Temperature

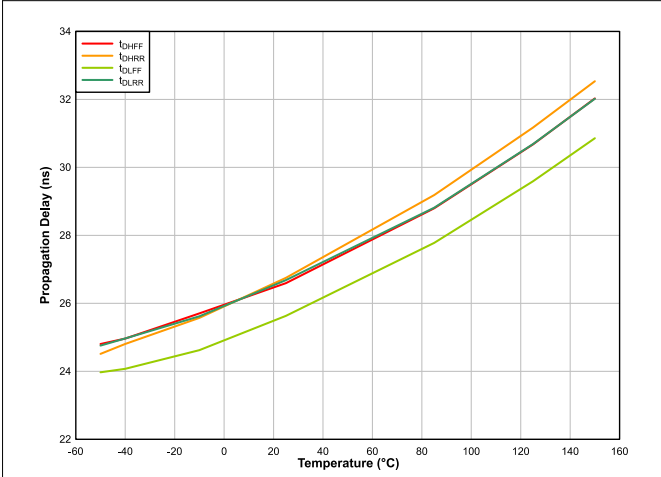


Figure 14. Propagation Delays vs. Temperature

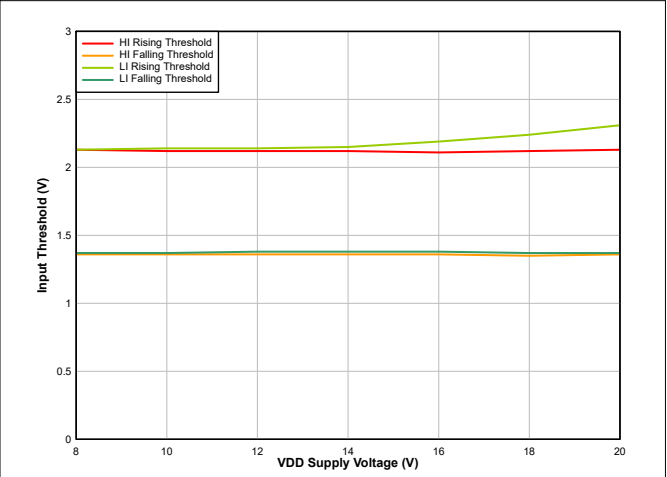


Figure 15. Propagation Delay vs. Supply Voltage

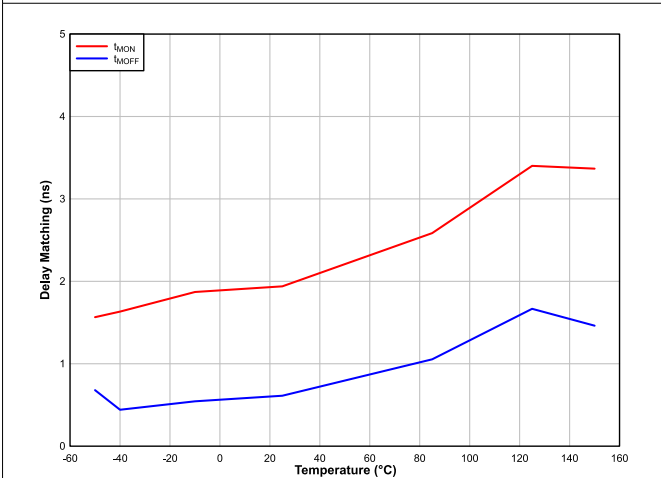


Figure 16. Delay Matching vs. Temperature

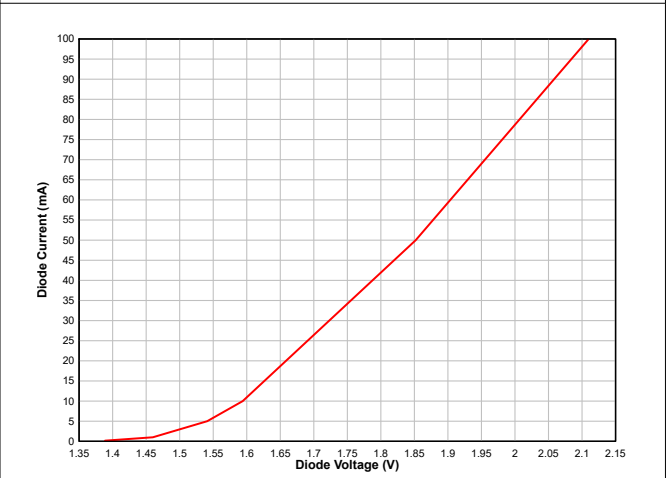


Figure 17. Diode Current vs. Diode Voltage

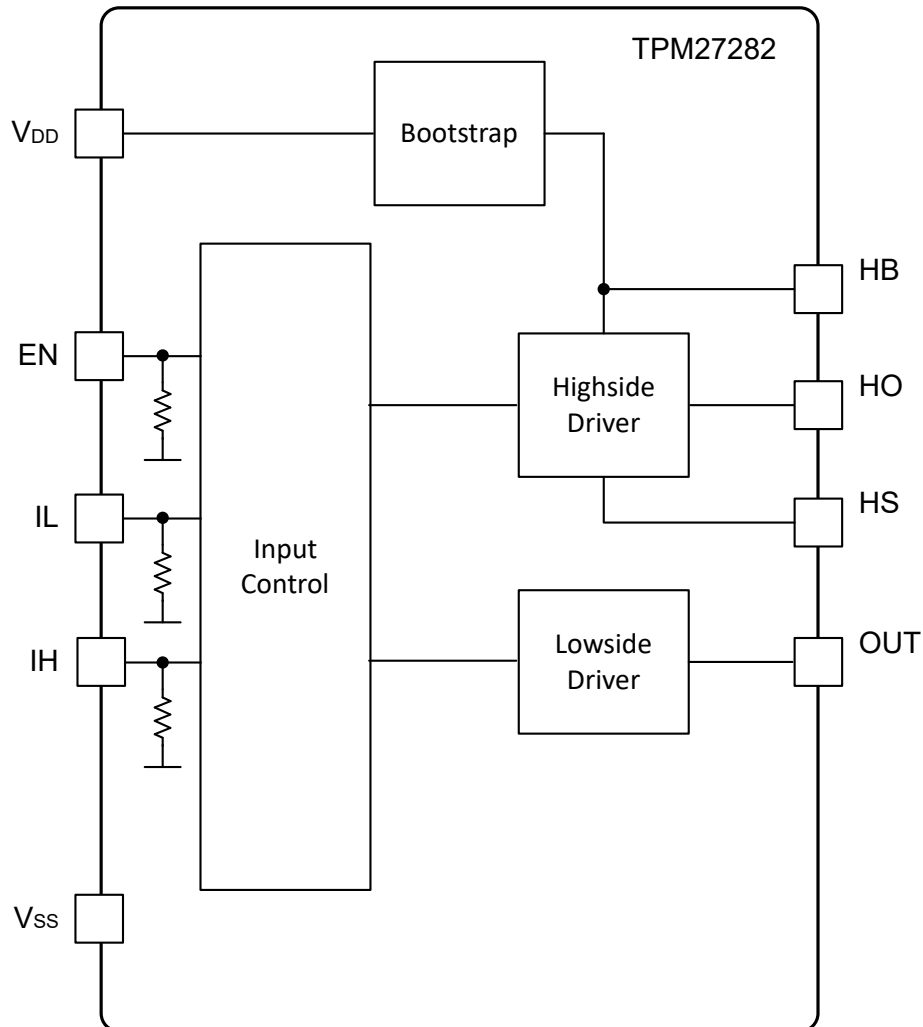
Detailed Description

Overview

The TPM27282 is a high-side and low-side MOSFET driver, featuring enable features, independent inputs for each side, providing ultimate flexibility in controlling application signals. It includes an integrated boot diode for the high-side driver's bias supply and is compatible with TTL logic inputs. The high-side driver operates in reference to the switch node (HS), typically connected to the high-side MOSFET's source and the low-side MOSFET's drain. The low-side driver is grounded at VSS. Key functions include input stages, under-voltage lockout (UVLO) protection, level shifting, the integrated boot diode, and output driver stages. It provides an input interlock feature.

Table 2. The TPM27282 Device Logic

EN	HI	LI	HO	LO
H	L	L	L	L
	L	H	L	H
	H	L	H	L
	H	H	L	L
	Floating	L	L	L
	Floating	H	L	H
	L	Floating	L	L
	H	Floating	H	L
L	X	X	L	L
Floating	X	X	L	L

Functional Block Diagram

Figure 18. Functional Block Diagram
Feature Description
Under Voltage Lockout (UVLO)

The gate driver incorporates Under-Voltage Lockout (UVLO) protection for the bias supplies of both the high-side and low-side drivers, ensuring that operation ceases when voltages fall below critical thresholds. The VDD UVLO safeguards the entire system by disabling both drivers if VDD is below 5.8 V, with a re-enabling threshold at 6.8 V, while the VHB UVLO specifically targets the high-side driver, engaging if the VHB to VHS differential is below 4.9 V and re-enabling at 7 V. These features provide a reliable and stable operation with hysteresis to prevent oscillation around the threshold points.

Input Stage

The TPM27282 features input stages that facilitate PWM signal interfacing with specific characteristics. It is designed with a pseudo-CMOS input structure offering significant hysteresis and compatibility with various PWM controllers. The TPM27282

120-V Supply, 3.5-A Peak, High-frequency HS and LS Gate Driver

has a pull-down resistance of 250 k Ω with capacitance of approximately 2 pF on inputs. It provides a more standard logic level input with a rising threshold at 2.4 V and a falling threshold at 0.8 V

The TPM27282 input stage could withstand negative voltage as low as -10V to improve system robustness.

The TPM27282 input stage has interlock logic to prevent cross-conduction. However, there is no deadtime built-in within the interlock feature.

Bootstrap Diode

The TPM27282 drivers include an integrated boot diode for generating the high-side bias voltage. This diode has its anode connected to VDD and its cathode connected to VHB. The VHB capacitor, which is linked to both the HB and HS pins, is recharged during each switching cycle when the HS pin goes to ground. The boot diode is designed to offer fast recovery, low resistance, and a voltage rating margin, ensuring efficient and dependable performance.

3PEAK recommends using an external Schottky diode in parallel with the internal diode in the case of high input voltage or high switching frequency for robust system operation. 3PEAK recommends connecting a 5- Ω resistor in series with VHB capacitor to limit charging current when using the internal diode.

Output Stages

The output stages of the driver serve as the link to the power MOSFETs in the power train. They are designed for high efficiency, with characteristics such as high slew rate, minimal resistance, and the ability to handle high peak currents, ensuring the power MOSFETs switch effectively. The low-side output stage operates with a reference from VDD to VSS, while the high-side output stage is referenced between VHB and VHS.

Application and Implementation

Note

Information in the following application sections is not part of the 3PEAK's component specification and 3PEAK does not warrant its accuracy or completeness. 3PEAK's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

Application Information

Driver Power Dissipation

The power dissipation of the gate driver consists of two parts: quiescent power P_{DC} and switching Power P_G .

The DC component of power loss in a driver is given by

$$P_{DC} = I_Q \times V_{DD} \quad (1)$$

where I_Q represents the quiescent current of the driver. This current is used to power all the internal circuits.

The power P_G is lost in the resistive components of the circuit during the MOSFET/IGBT switching transitions. Approximately half of this power is expended while the load capacitor charges on turn-on, and the other half is lost as the load capacitor discharges on turn-off. Without the use of an external gate resistor between the driver and the MOSFET/IGBT, the entire P_G is dissipated within the driver package itself. However, by incorporating external gate-drive resistors, the power dissipation is distributed between the internal resistance of the driver and the external gate resistors, effectively sharing the thermal load.

$$P_G = Q_g \times V_{DD} \times f_{SW} \quad (2)$$

where

- Q_g is the gate charge of the power device
- f_{SW} is the switching frequency
- V_{DD} is the supply voltage

If R_G is applied between the driver and the gate of the power device to slow down the power device transition, the power dissipation of the driver is shown below:

$$P_G = \frac{1}{2} \times Q_g \times V_{DD} \times f_{SW} \times \left(\frac{R_{OL}}{R_{OL} + R_G} + \frac{R_{OH}}{R_{OH} + R_G} \right) \quad (3)$$

where

- R_{OH} is the equivalent pull-up resistance of TPM27282
- R_{OL} is the pull-down resistance of TPM27282
- R_G is the gate resistance between the driver output and the gate of the power device

Typical Application

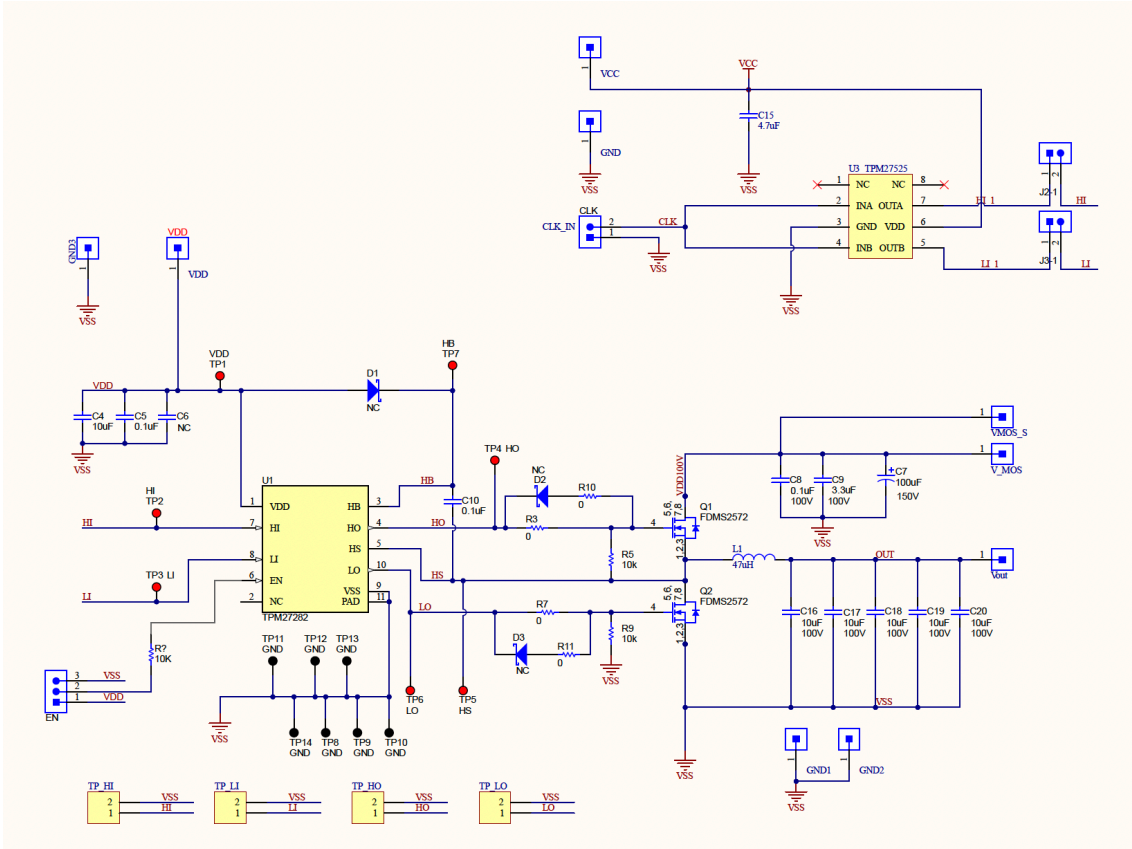


Figure 19. Typical Application

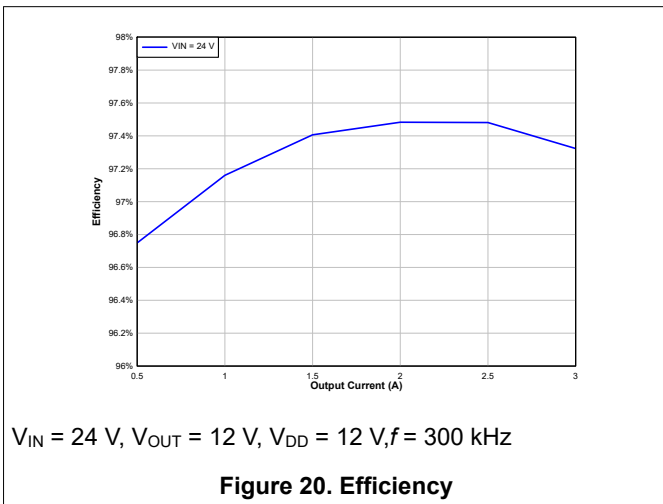


Figure 20. Efficiency

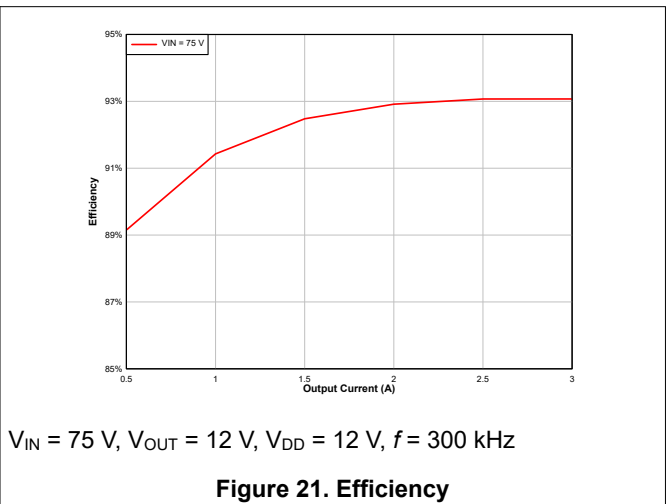


Figure 21. Efficiency

Layout

Layout Guideline

- For the voltage mode input driver, a low ESR and ESL capacitor should be placed close to VCC and VEE pins, and make the loop from VCC to VEE small.
- For the current mode input driver, a low ESR and ESL capacitor should be placed close to Cathode and Anode pins.
- To ensure isolation performance between the primary and secondary sides, avoid placing any PCB traces or copper below the driver device. A PCB cutout or groove is recommended to increase creepage distance.
- To enhance thermal performance, PCB copper connected with VCC and VEE is recommended to be enlarged.
- Using a Kelvin source to decouple the power loop and driver loop.

Layout Example

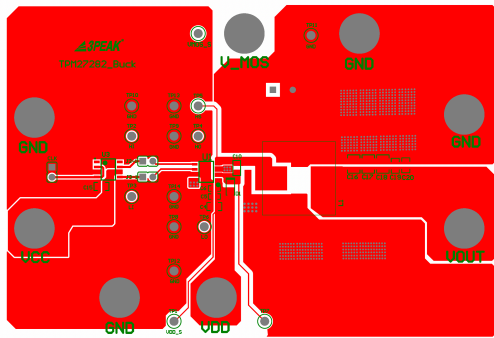


Figure 22. Top Layer

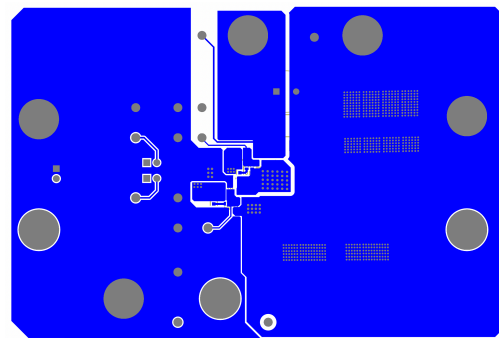


Figure 23. Bottom Layer

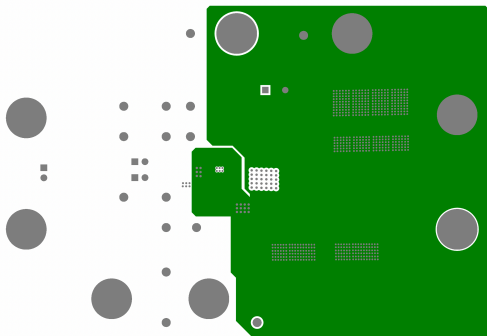


Figure 24. M1 Layer

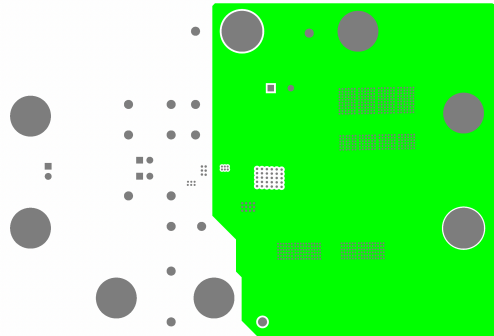
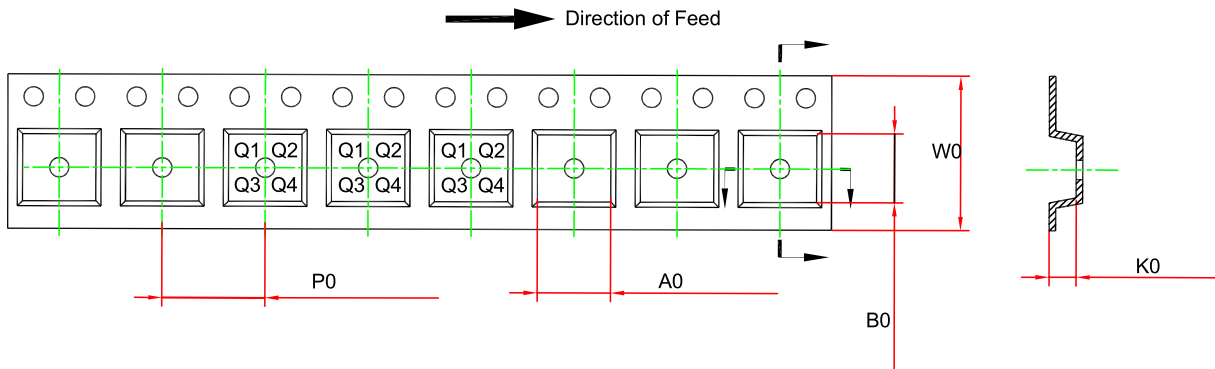
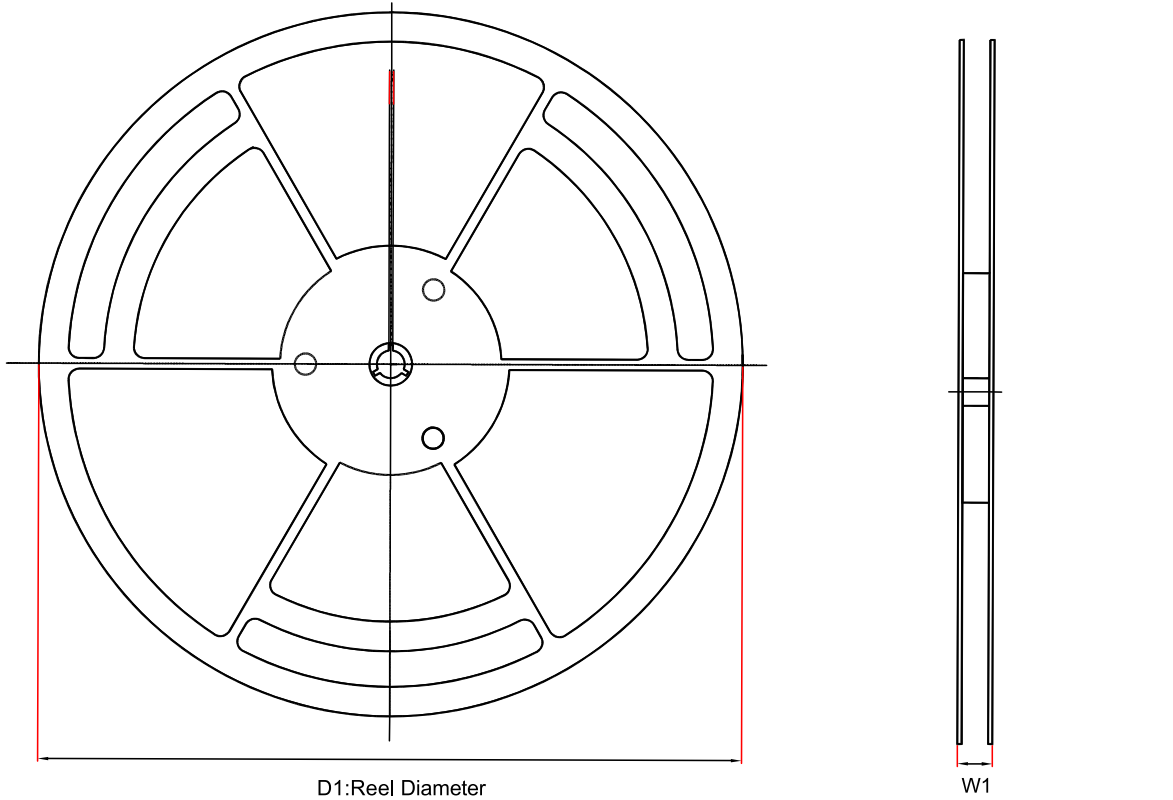


Figure 25. M2 Layer

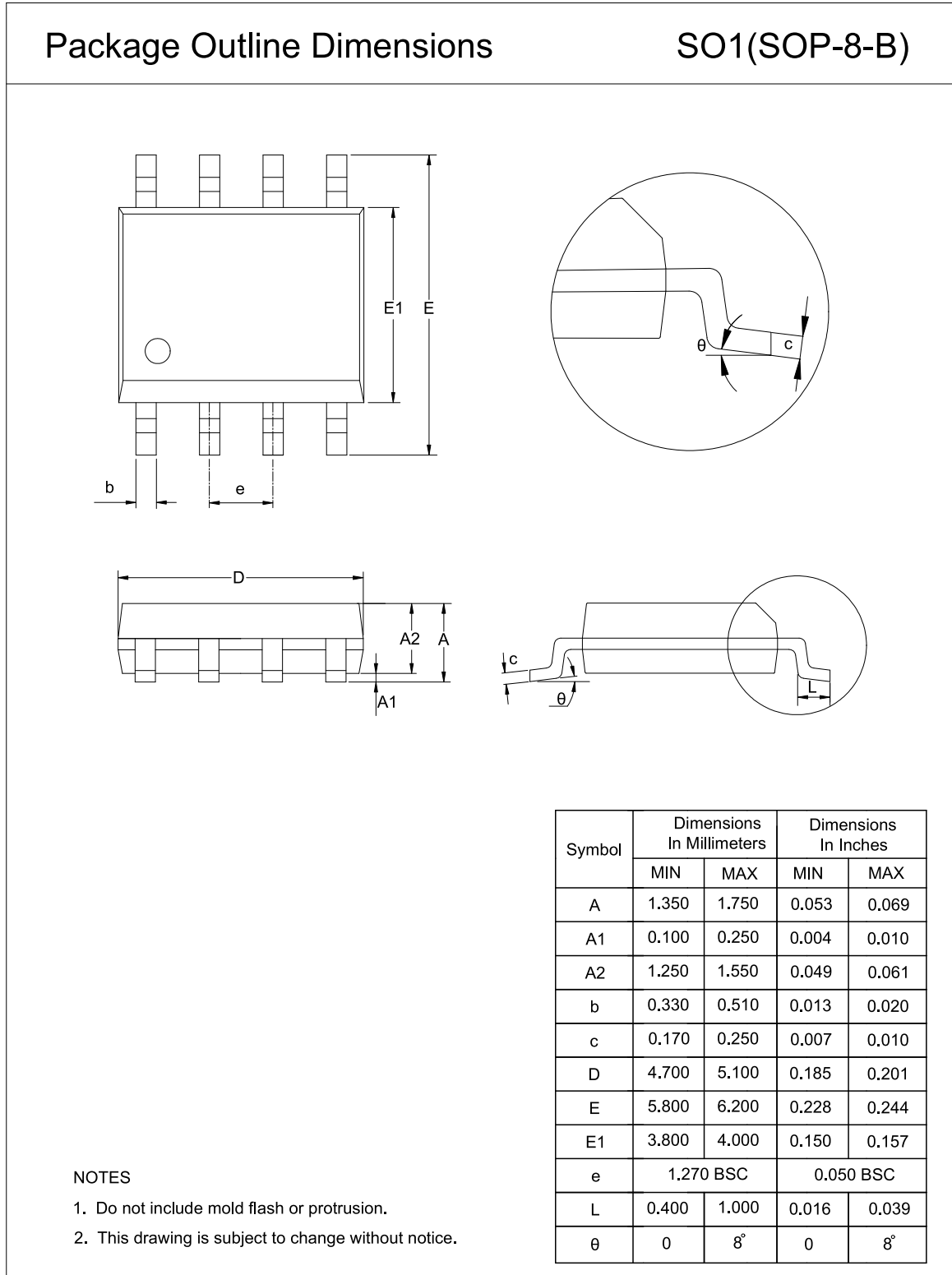
Tape and Reel Information

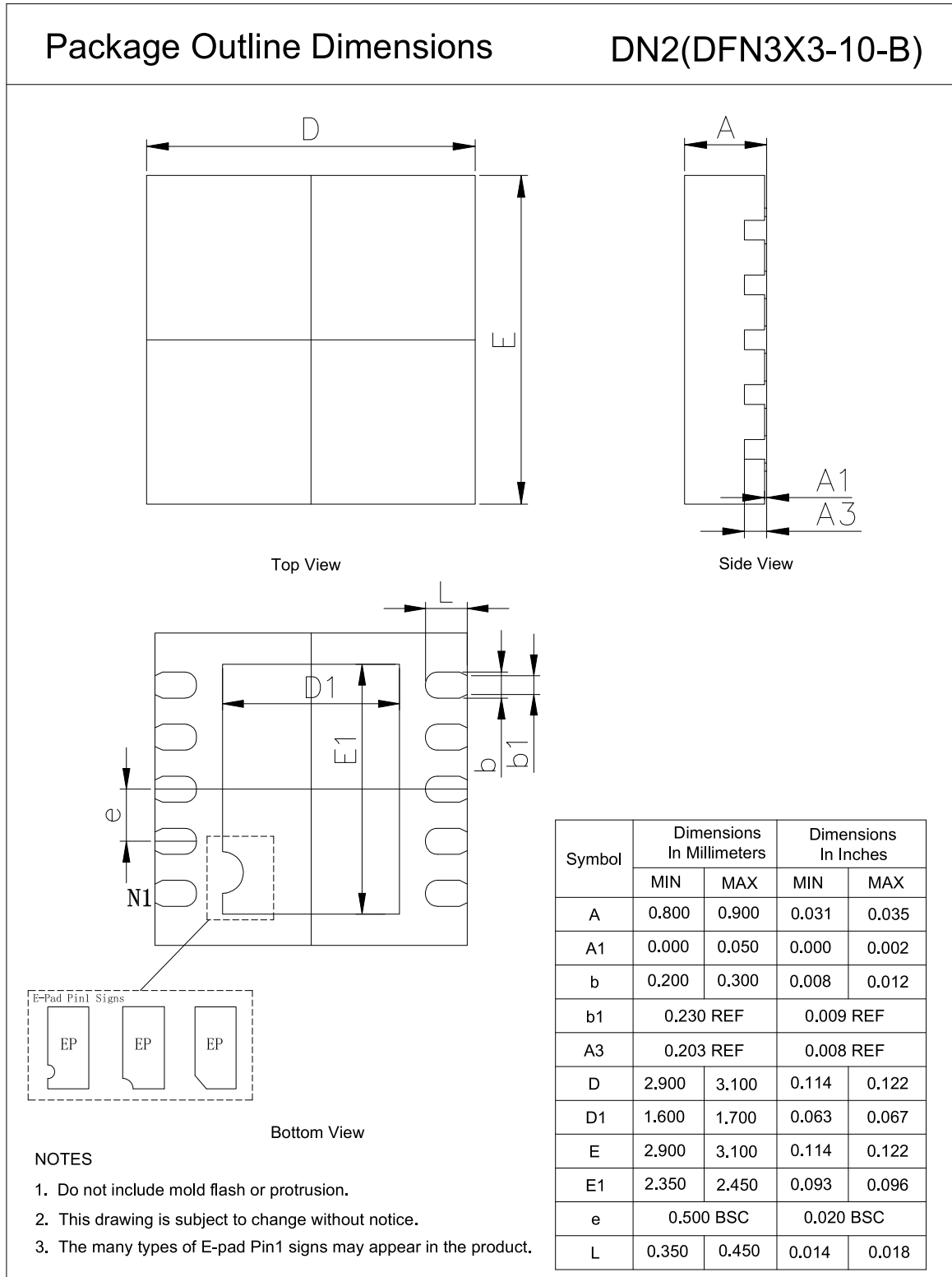


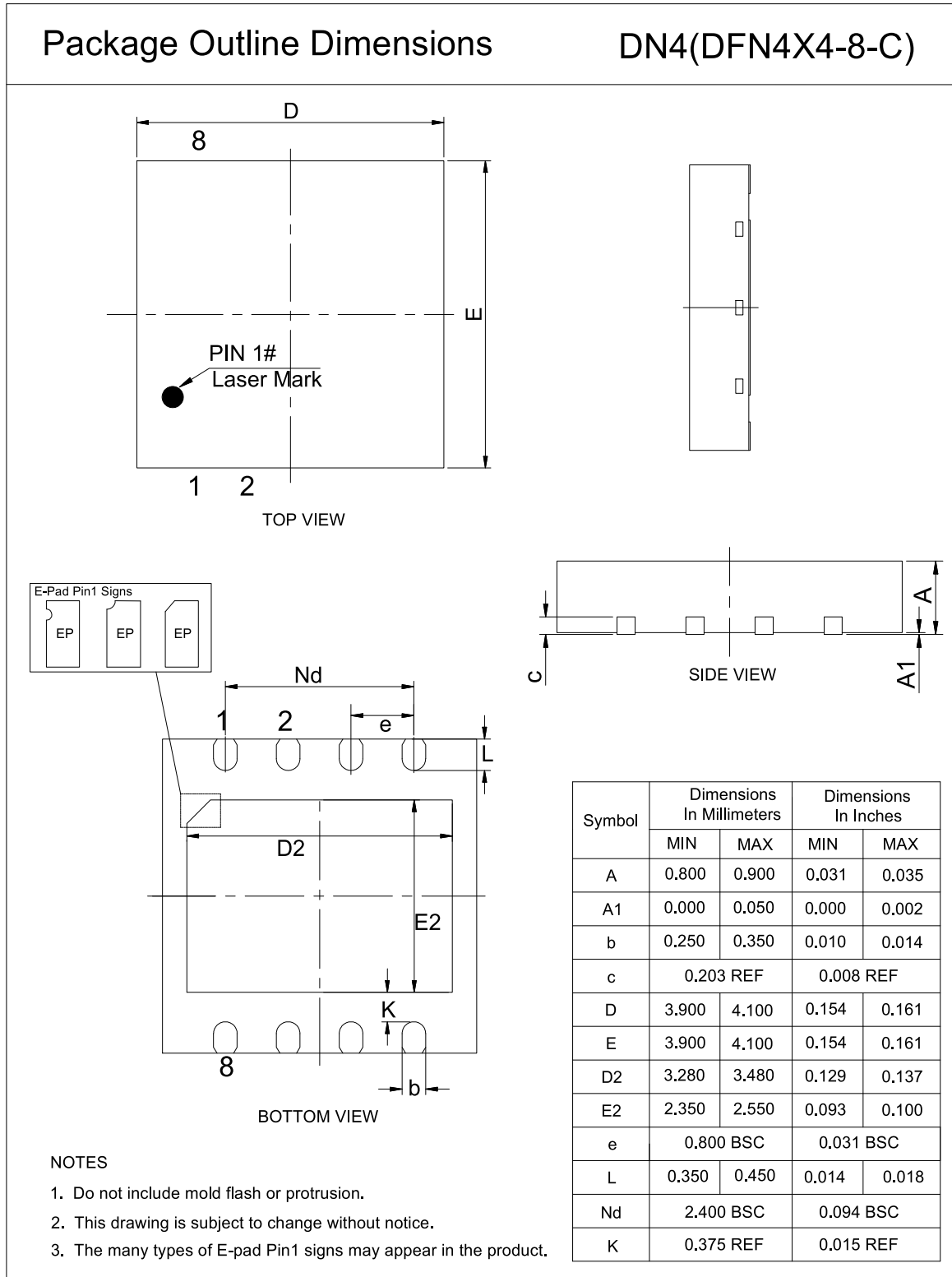
Order Number	Package	D1 (mm)	W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P0 (mm)	W0 (mm)	Pin1 Quadrant
TPM27282-SO1R	SOP8	330	17.6	6.5	5.4	2	8	12	Q1
TPM27282-DF8R	DFN3X3-10	330	17.6	3.3	3.3	1.1	8	12	Q2
TPM27282-DFMR	DFN4X4-8	330	17.6	4.3	4.3	1.1	8	12	Q2

Package Outline Dimensions

SOP8



DFN3X3-10


DFN4X4-8


Order Information

Order Number	Operating Temperature Range	Package	Marking Information	MSL	Transport Media, Quantity	Eco Plan
TPM27282-DF8R	-40 to 125°C	DFN3X3-10	27282	MSL1	Tape and Reel,4000	Green
TPM27282-SO1R ⁽¹⁾	-40 to 125°C	SOP8	27282	MSL1	Tape and Reel,4000	Green
TPM27282-DFMR ⁽¹⁾	-40 to 125°C	DFN4X4-8	27282	MSL3	Tape and Reel,3000	Green

(1) Contact 3PEAK representatives for more information.

Green: 3PEAK defines "Green" to mean RoHS compatible and free of halogen substances.

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