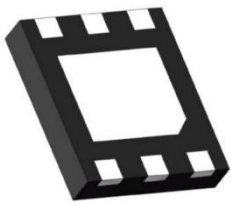
Description

Innotion's YP801241T is a 12-watt, pre-matched gallium nitride (GaN) high electron mobility transistor (HEMT) designed specifically with high efficiency, high gain and wide bandwidth capabilities with frequency up to 8500MHz. The transistor is supplied in a plastic DFN-6L 4mm*4.5mm package.



Typical Performance (T_c=25℃) of Demonstration Amplifier

Tabel 1. Test data 7-8GHz

Bias: VDD=28V，VGS=-2.7V, IDQ=60mA

Freq(GHz)	Pout(dBm)	Gpsat(dB)	EFF(%)
7	42.2	10	51.4
7.2	42.1	10	53.8
7.4	42.1	10	54.3
7.6	41.8	10	54.2
7.8	41.4	10	52.9
8	41.1	10	52

Features

- High Efficiency and Linear Gain Operation
- Negative Gate Voltage and Bias Sequencing Required
- Excellent Thermal Stability and Excellent Ruggedness
- Metal Based Package Sealed with Ceramic-Epoxy Lid

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Table2. Maximum Ratings

Rating	Symbol	Value	Unit
Drain-Source Voltage	V_{DSS}	+120	Vdc
Gate-Source Voltage	V_{GS}	-8 to 0	Vdc
Operating Voltage	V_{DD}	20~32	Vdc
Storage Temperature Range	T_{stg}	-55 to +150	℃
Case Operating Temperature	T_C	+150	℃
Operating Junction Temperature	T_J	+225	℃
Maxium Forward Current	I_{gmax}	2.4	mA

Table3. Electrical Characteristics

Characteristics	Symbol	Min.	Typ.	Max.	Unit	Conditions
DC Characteristics						
Gate Threshold Voltage	$V_{GS(th)}$		-2.8		V	V_{DS}=28V, I_D=2.4mA
Gate Quiescent Voltage	$V_{GS(Q)}$		-2.7		V	V_{DS}=28V, I_{DS}=60mA
Drain-Source Breakdown Voltage	V_{BR}		90		V	V_{GS}=-10V,I_{DS}=2.4mA

Table4. DC BIAS SEQUENCING

DC BIAS SEQUENCING	
Turn On GaN Device	Turn Off GaN Device
1. RF Power Off 2. Set VGS=-5V(Negative Voltage to Pinch Off) 3. Turn on VDD Voltage 4. Slowly Increase VGS Until Bias Current IDQ is Set 5. Turn on RF Power	1. Turn off RF Power 2. Turn off VDD Voltage 3. After VDD is Discharged, Set VGS=-5V 4. Turn off VGS Voltage

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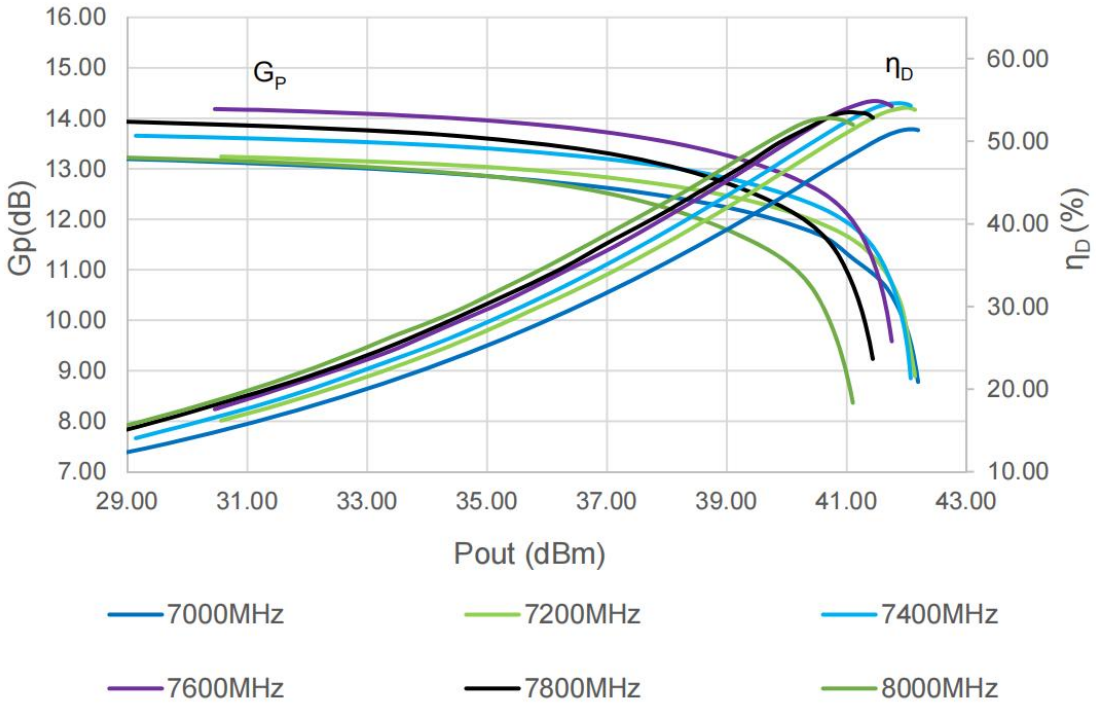
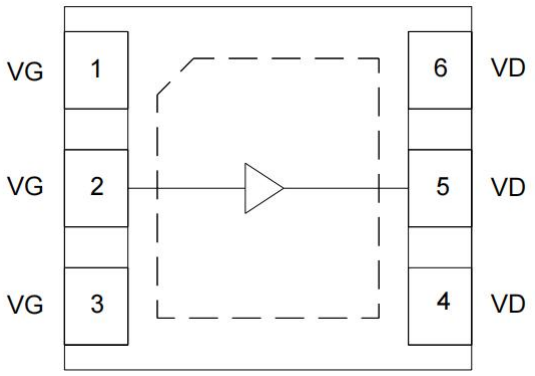
Test Result

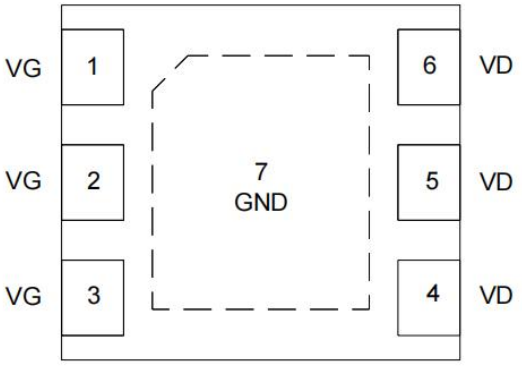
Bias: V_{DS}=28V, I_{DQ}=60mA, CW



Pin Definitions



Function Block Diagram



Pin Definitions

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PCB Layout

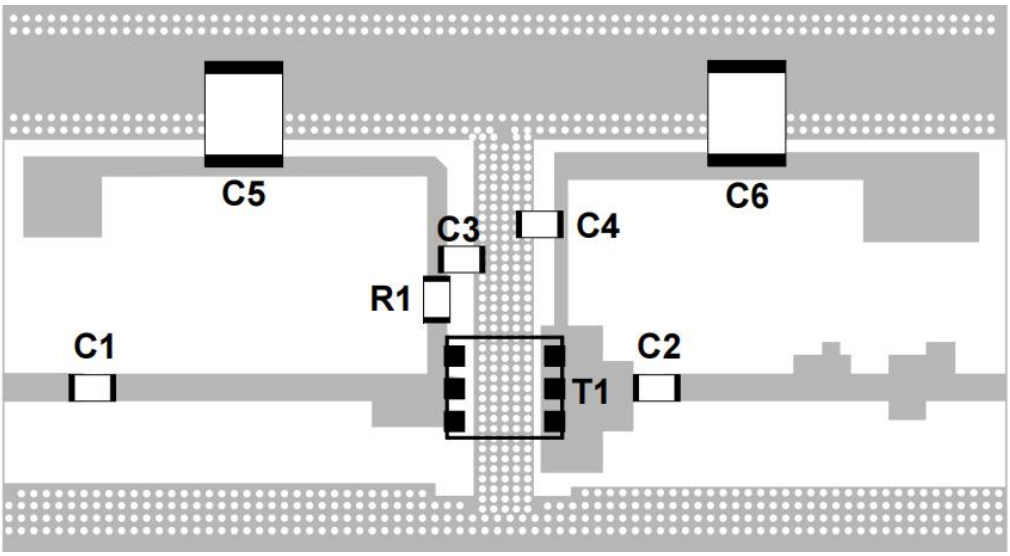


Figure.1 7-8G reference design

BOM List

S/N	Type	Designator	Part NO.	Value
1	Cap	C1,C2,C3	ATC600F1R2JT250XT	1.2pF
2	Cap	C4	ATC600S1R0JT250XT	1pF
3	Cap	C5,C6	GRM31CZ72A225KE	2.2uF
4	Res	R1	RC0805FR_0710RL	10Ω
5	Transistor	T1	YP801241T	
6	PCB	/	RO4350B	20mil

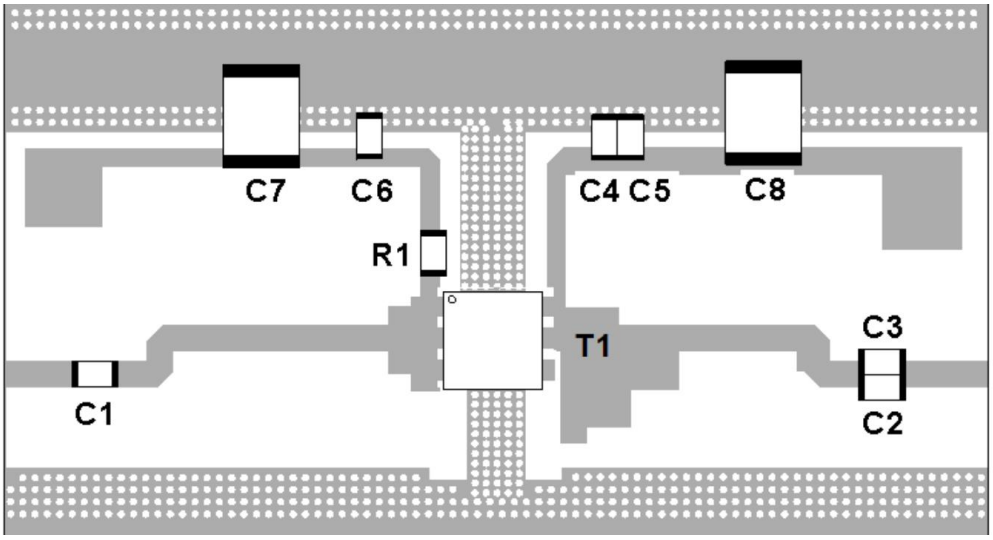


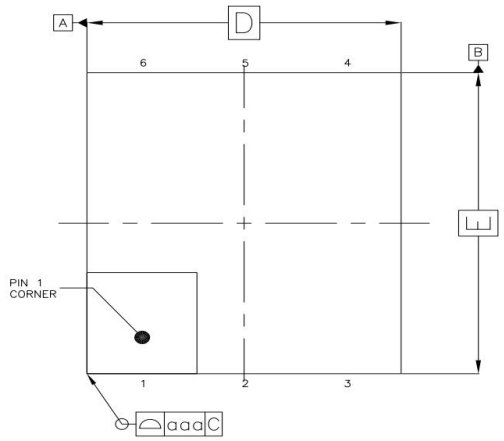
Figure.2 5-6G reference design

BOM List

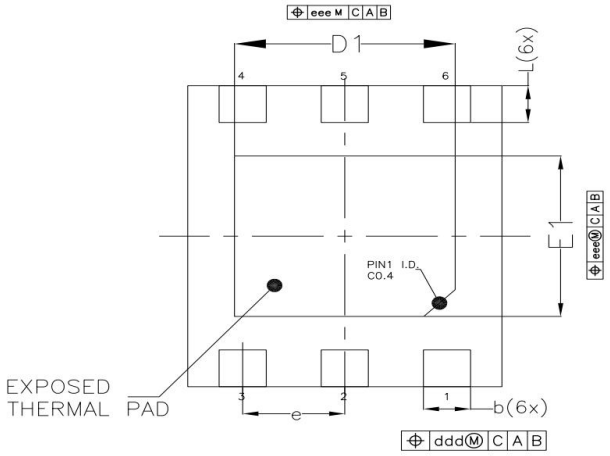
S/N	Type	Designator	Part NO.	Value
1	Cap	C1,C2,C3	ATC600F3R3JT250XT	3.3 pF
2	Cap	C4,C5,C6	ATC600S2R7JT250XT	2.7 pF
3	Cap	C7,C8	GRM31CZ72A225KE	2.2 UF
4	Res	R1	RC0805FR_0710RL	10Ω
5	Transistor	T1	YP801241T	
6	PCB	/	RO4350B	20mil

Packaging Diagram

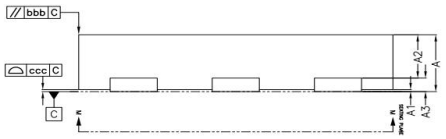
(DFN-6L, 4mm*4.5mm, Units: millimeters)



TOP VIEW



BOTTOM VIEW
VIEW M—M



SIDE VIEW

Description		S/N	mm		
			min.	Typical	max.
TOTAL THICKNESS		A	0.78	0.85	0.93
STAND OFF		A1	0.00	-----	0.05
MOLD THICKNESS		A2	0.60	0.65	0.70
L/F THICKNESS		A3	0.203 REF		
BODY SIZE	D	D	3.95	4.00	4.05
	E	E	4.45	4.50	4.55
LEAD PITCH		e	1.30 BSC		
LEAD WIDTH		b	0.55	0.60	0.65
LEAD LENGTH		L	0.50	0.55	0.60
EP SIZE		D1	2.76	2.81	2.86
		E1	2.35	2.40	2.45
Tolerance of form and position					
PACKAGE EDGE TOLERANCE		aaa	0.1		
MOLD FLATNESS		bbb	0.1		
LEAD COPLANARITY		ccc	0.08		
LEAD POSITION OFFSET		ddd	0.1		
EXPOSED PAD OFFSET		eee	0.1		