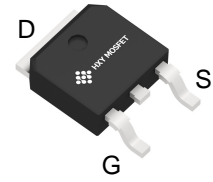




## Description

The 60N02 uses advanced trench technology to provide excellent  $R_{DS(ON)}$ , low gate charge and operation with gate voltages as low as 4.5V. This device is suitable for use as a Battery protection or in other Switching application.



TO-252-2L

## General Features

$V_{DS} = 20V$   $I_D = 60A$

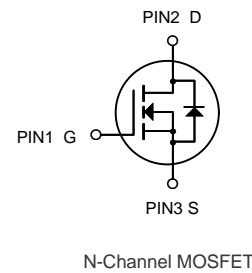
$R_{DS(ON)} < 6m\Omega @ V_{GS}=4.5V$

## Application

Battery protection

Load switch

Uninterruptible power supply



## Ordering Information

Product ID	Pack	Brand	Qty(PCS)
60N02	TO-252-2L	HXY MOSFET	2500

## Absolute Maximum Ratings ( $T_c=25^\circ C$ unless otherwise noted)

Symbol	Parameter	Limit	Unit
$V_{DS}$	Drain-Source Voltage	20	V
$V_{GS}$	Gate-Source Voltage	$\pm 12$	V
$I_D$	Drain Current-Continuous	60	A
$I_D(100^\circ C)$	Drain Current-Continuous( $T_c=100^\circ C$ )	42	A
$I_{DM}$	Pulsed Drain Current	210	A
$P_D$	Maximum Power Dissipation	60	W
	Derating factor	0.48	W/ $^\circ C$
$E_{AS}$	Single pulse avalanche energy (Note 5)	200	mJ
$T_J, T_{STG}$	Operating Junction and Storage Temperature Range	-55 To 150	$^\circ C$
$R_{\theta JC}$	Thermal Resistance, Junction-to-Case (Note 2)	2.1	$^\circ C/W$



**Electrical Characteristics (T<sub>c</sub>=25°C unless otherwise noted)**

Parameter	Symbol	Condition	Min	Typ	Max	Unit
Drain-Source Breakdown Voltage	BV <sub>DSS</sub>	V <sub>GS</sub> =0V I <sub>D</sub> =250μA	20	-	-	V
Zero Gate Voltage Drain Current	I <sub>DSS</sub>	V <sub>DS</sub> =20V, V <sub>GS</sub> =0V	-	-	1	μA
Gate-Body Leakage Current	I <sub>GSS</sub>	V <sub>GS</sub> =±12V, V <sub>DS</sub> =0V	-	-	±100	nA
Gate Threshold Voltage	V <sub>GS(th)</sub>	V <sub>DS</sub> =V <sub>GS</sub> , I <sub>D</sub> =250μA	0.5	0.75	1.0	V
Drain-Source On-State Resistance	R <sub>DS(on)</sub>	V <sub>GS</sub> =4.5V, I <sub>D</sub> =20 A	-	4.5	6	mΩ
		V <sub>GS</sub> =2.5V, I <sub>D</sub> =15A	-	5.3	8.2	mΩ
Forward Transconductance	g <sub>FS</sub>	V <sub>DS</sub> =10V, I <sub>D</sub> =20A	15	-	-	S
Input Capacitance	C <sub>iss</sub>	V <sub>DS</sub> =10V, V <sub>GS</sub> =0V, F=1.0MHz	-	2000	-	PF
Output Capacitance	C <sub>oss</sub>		-	500	-	PF
Reverse Transfer Capacitance	C <sub>rss</sub>		-	200	-	PF
Turn-on Delay Time	t <sub>d(on)</sub>	V <sub>DD</sub> =10V, I <sub>D</sub> =2A, R <sub>L</sub> =1Ω V <sub>GS</sub> =4.5V, R <sub>G</sub> =3Ω	-	6.4	-	nS
Turn-on Rise Time	t <sub>r</sub>		-	17.2	-	nS
Turn-Off Delay Time	t <sub>d(off)</sub>		-	29.6	-	nS
Turn-Off Fall Time	t <sub>f</sub>		-	16.8	-	nS
Total Gate Charge	Q <sub>g</sub>	V <sub>DS</sub> =10V, I <sub>D</sub> =20A, V <sub>GS</sub> =10V	-	27	-	nC
Gate-Source Charge	Q <sub>gs</sub>		-	6.5	-	nC
Gate-Drain Charge	Q <sub>gd</sub>		-	6.4	-	nC
Diode Forward Voltage <sup>(Note 3)</sup>	V <sub>SD</sub>	V <sub>GS</sub> =0V, I <sub>S</sub> =10A	-	-	1.2	V
Diode Forward Current <sup>(Note 2)</sup>	I <sub>S</sub>		-	-	60	A
Reverse Recovery Time	t <sub>rr</sub>	T <sub>J</sub> = 25°C, I <sub>F</sub> = 20A di/dt = 100A/μs <sup>(Note3)</sup>	-	25	-	nS
Reverse Recovery Charge	Q <sub>rr</sub>		-	24	-	nC
Forward Turn-On Time	t <sub>on</sub>	Intrinsic turn-on time is negligible (turn-on is dominated by LS+LD)				

**Notes:**

1. Repetitive Rating: Pulse width limited by maximum junction temperature.
2. Surface Mounted on FR4 Board, t ≤ 10 sec.
3. Pulse Test: Pulse Width ≤ 300μs, Duty Cycle ≤ 2%.
4. Guaranteed by design, not subject to production
5. E<sub>AS</sub> condition : T<sub>J</sub>=25°C, V<sub>DD</sub>=10V, V<sub>G</sub>=10V, L=0.5mH, R<sub>G</sub>=25Ω.



Typical Electrical and Thermal Characteristics (Curves)

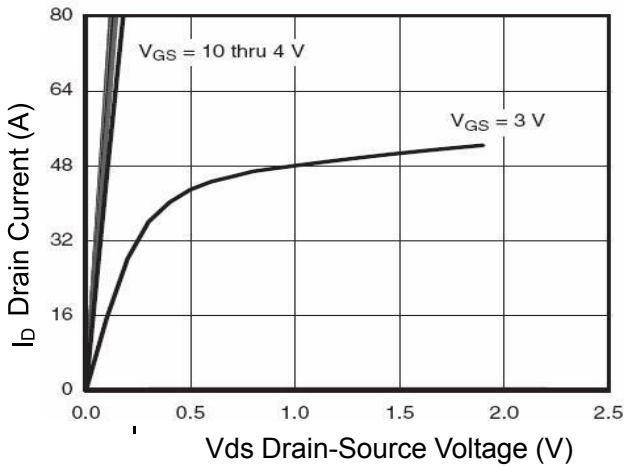


Figure 1 Output Characteristics

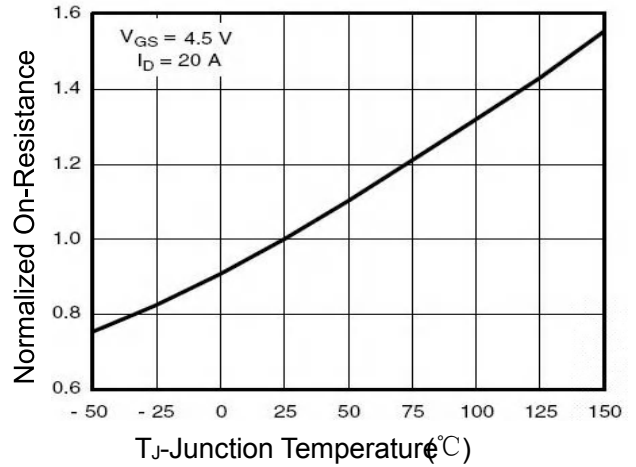


Figure 4  $R_{dson}$ -Junction Temperature

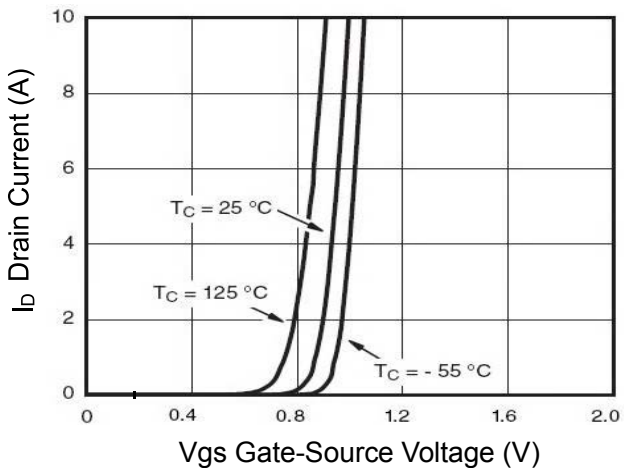


Figure 2 Transfer Characteristics

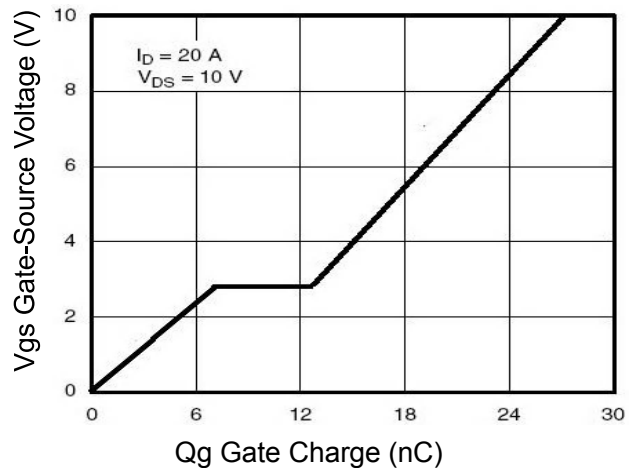


Figure 5 Gate Charge

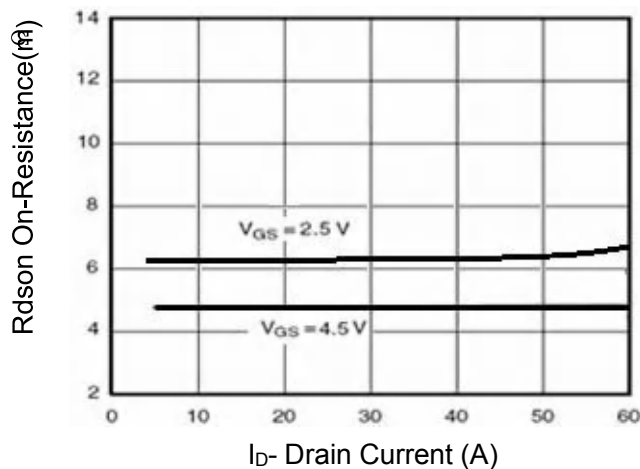


Figure 3  $R_{dson}$ - Drain Current

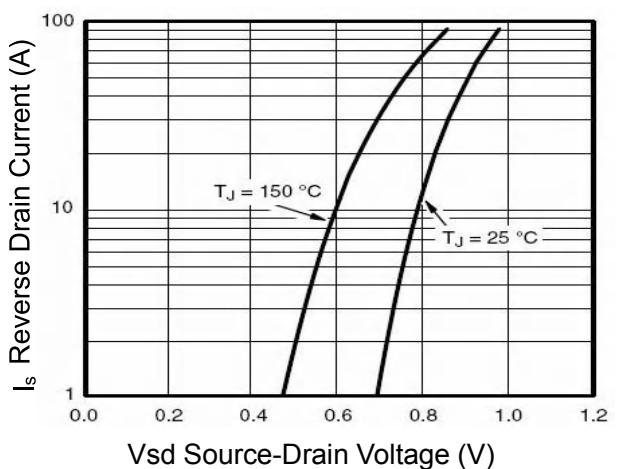
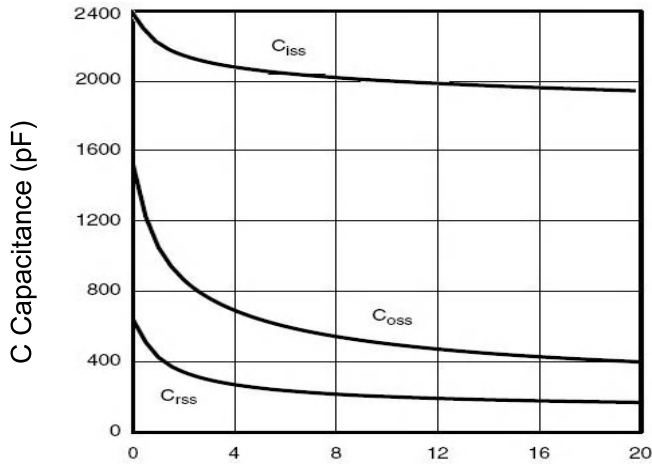
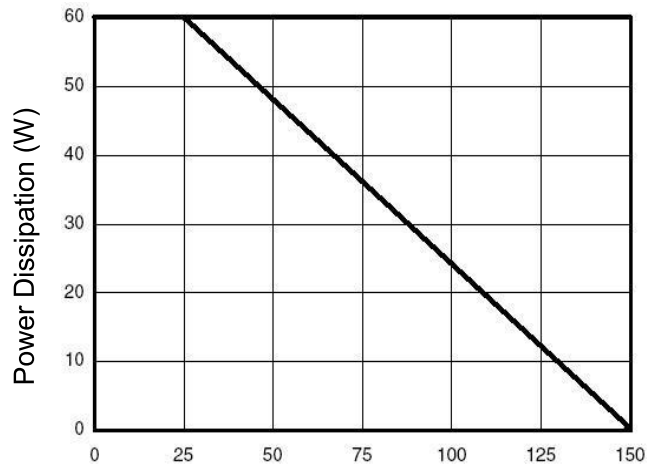


Figure 6 Source- Drain Diode Forward



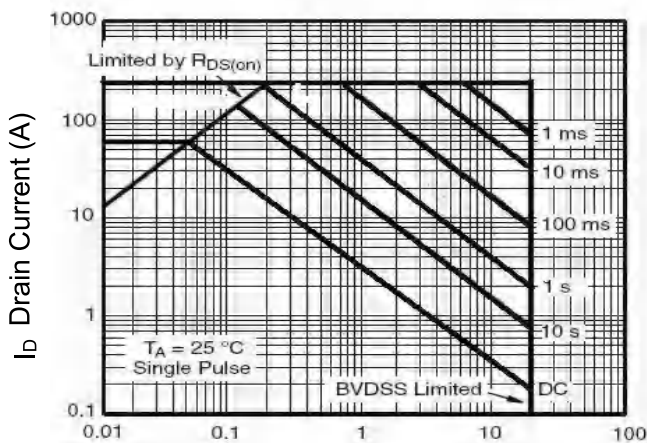
Vds Drain-Source Voltage (V)

Figure 7 Capacitance vs Vds



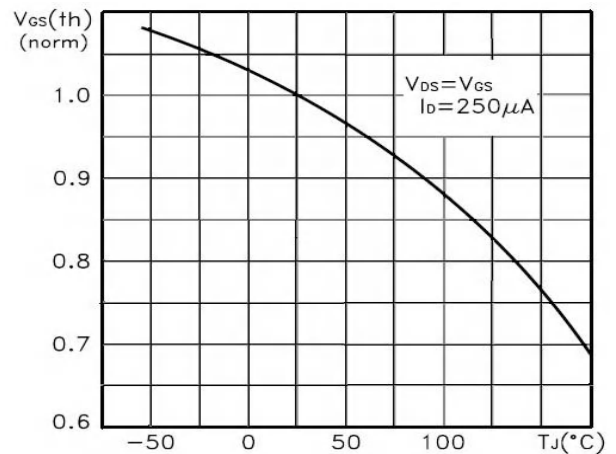
TJ-Junction Temperature (°C)

Figure 9 Power De-rating



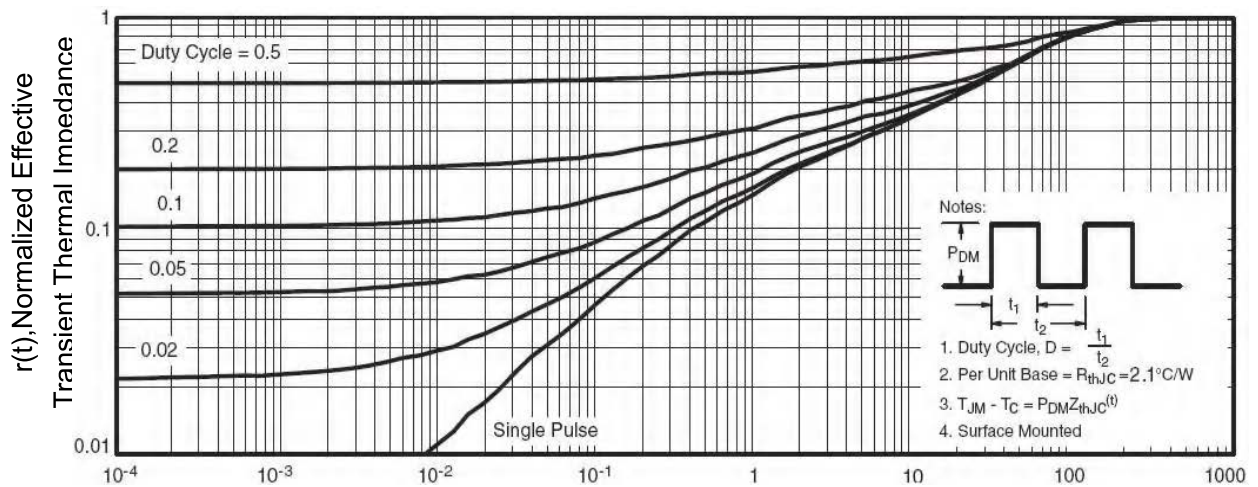
Vds Drain-Source Voltage (V)

Figure 8 Safe Operation Area



TJ-Junction Temperature(°C)

Figure 10 VGS(th) vs Junction Temperature



Square Wave Pluse Duration(sec)

Figure 11 Normalized Maximum Transient Thermal Impedance





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