



Description

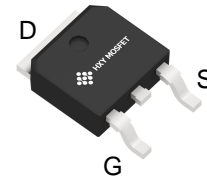
The HXY2N65D can be used in various power switching circuit for system miniaturization and higher efficiency. The package form is TO-252-2L, which accords with the RoHS standard.

General Features

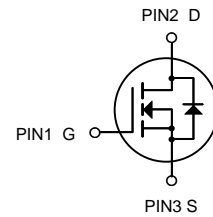
$V_{DS} = 650V, I_D = 2A$
 $R_{DS(ON)} < 5\Omega @ V_{GS} = 10V$

Application

- Power switch circuit of adaptor and charger.



TO-252-2L
(DPAK)



N-Channel MOSFET

Ordering Information

Product ID	Pack	Brand	Qty(PCS)
HXY2N65D	TO-252-2L(DPAK)	HXY MOSFET	2500

Absolute Maximum Ratings @T_j = 25°C(unless otherwise specified)

Symbol	Parameter	Rating	Units
V _{DS}	Drain-Source Voltage	650	V
V _{GS}	Gate-Source Voltage	±30	V
I _D @T _C =25°C	Drain Current, V _{GS} @ 10V	2	A
I _D @T _C =100°C	Drain Current, V _{GS} @ 10V	1.3	A
I _{DM}	Pulsed Drain Current	8	A
P _D @T _C =25°C	Total Power Dissipation	35	W
E _{AS}	Single Pulse Avalanche Energy	50	mJ
T _{STG}	Storage Temperature Range	-45 to 125	°C
T _J	Operating Junction Temperature Range	-45 to 125	°C



Electrical Characteristics (T_c= 25°C unless otherwise specified):

Symbol	Parameter	Test Conditions	Rating			Units
			Min.	Typ.	Max.	
V _{DSS}	Drain to Source Breakdown Voltage	V _{GS} =0V, I _D =250μA	650	--	--	V
ΔBV _{DSS} /ΔT _J	Bvdss Temperature Coefficient	I _D =250uA, Reference 25°C	--	0.7	--	V/°C
I _{DSS}	Drain to Source Leakage Current	V _{DS} =650V, V _{GS} = 0V, T _a = 25°C	--	--	1	μA
		V _{DS} =520V, V _{GS} = 0V, T _a = 125°C	--	--	100	μA
I _{GSS(F)}	Gate to Source Forward Leakage	V _{GS} =+30V	--	--	100	nA
I _{GSS(R)}	Gate to Source Reverse Leakage	V _{GS} =-30V	--	--	-100	nA
R _{DS(ON)}	Drain-to-Source On-Resistance	V _{GS} =10V, I _D =1A	--	4.2	5	Ω
V _{GS(TH)}	Gate Threshold Voltage	V _{DS} = V _{GS} , I _D = 250μA	2.0	--	4.0	V
g _{fs}	Forward Transconductance	V _{DS} =15V, I _D =1A	--	1.8	--	S
C _{iss}	Input Capacitance	V _{GS} = 0V V _{DS} = 25V f = 1.0MHz	--	335	--	pF
C _{oss}	Output Capacitance		--	33	--	
C _{rss}	Reverse Transfer Capacitance		--	3	--	
t _{d(ON)}	Turn-on Delay Time		--	11	--	
t _r	Rise Time	I _D =2A V _{DD} = 325V R _G =10Ω	--	13	--	ns
t _{d(OFF)}	Turn-Off Delay Time		--	29	--	
t _f	Fall Time		--	12	--	
Q _g	Total Gate Charge	I _D =2A V _{DD} =520V V _{GS} = 10V	--	9.5	--	nC
Q _{gs}	Gate to Source Charge		--	1.5	--	
Q _{gd}	Gate to Drain ("Miller")Charge		--	4.9	--	
I _S	Continuous Source Current (Body Diode)		--	--	2	A
I _{SM}	Maximum Pulsed Current (Body Diode)		--	--	8	A
V _{SD}	Diode Forward Voltage	I _S =2.0A, V _{GS} =0V	--	--	1.5	V
t _{rr}	Reverse Recovery Time	I _S =2.0A, T _J = 25°C di _f /dt=100A/us, V _{GS} =0V	--	187	--	ns
Q _{rr}	Reverse Recovery Charge		--	610	--	nC
I _{RRM}	Reverse Recovery Current		--	6.6	--	A

Symbol	Parameter	Max.	Units
R _{θJC}	Junction-to-Case	3.57	°C/W
R _{θJA}	Junction-to-Ambient	100	°C/W

a¹: Repetitive rating; pulse width limited by maximum junction temperature

a²: L=10mH, I_D=3.1A, Start T_J=25°C

a³: I_{SD} =2A, di/dt ≤100A/us, V_{DD} ≤BV_{DS}, Start T_J=25°C



Characteristics Curve:

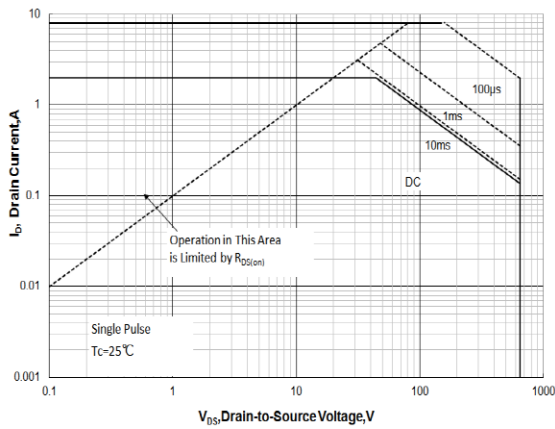


Figure 1 Maximum Forward Bias Safe Operating Area

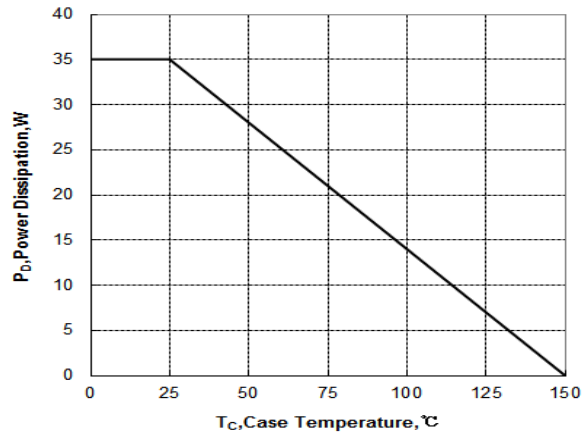


Figure 2 Maximum Power dissipation vs Case Temperature

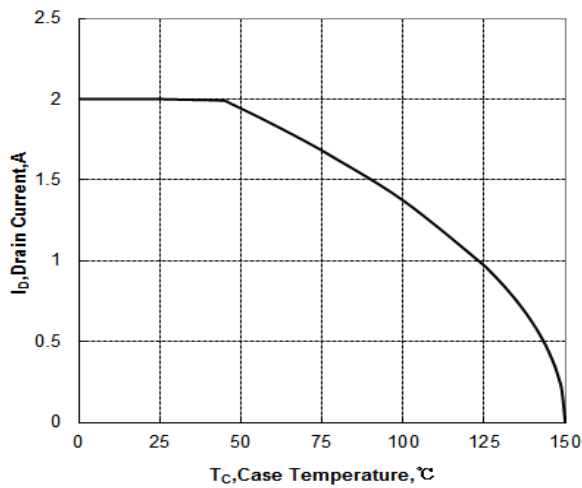


Figure 3. Maximum Continuous Drain Current vs Case Temperature

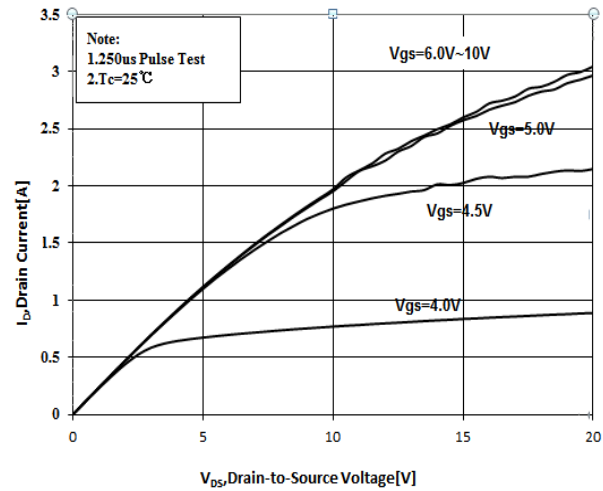


Figure 4. Typical Output Characteristics

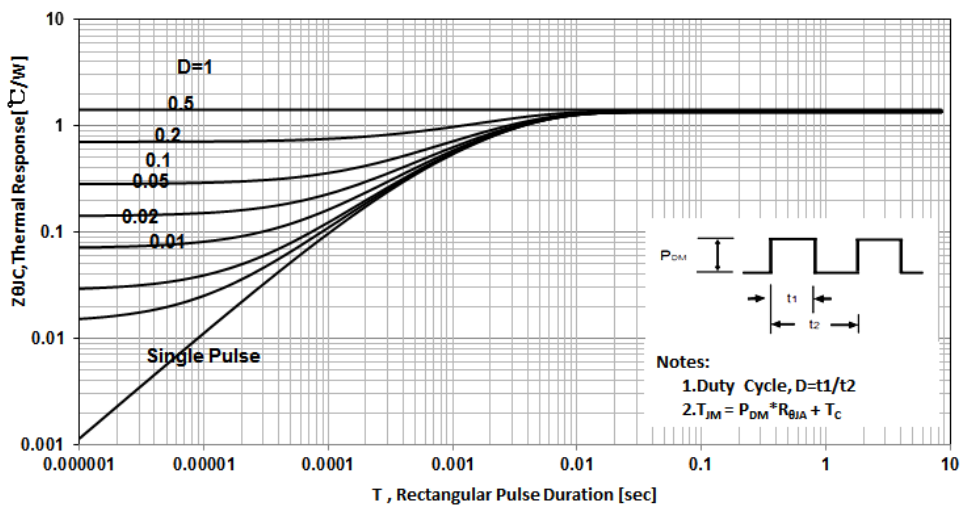


Figure 5. Maximum Effective Thermal Impedance , Junction to Case

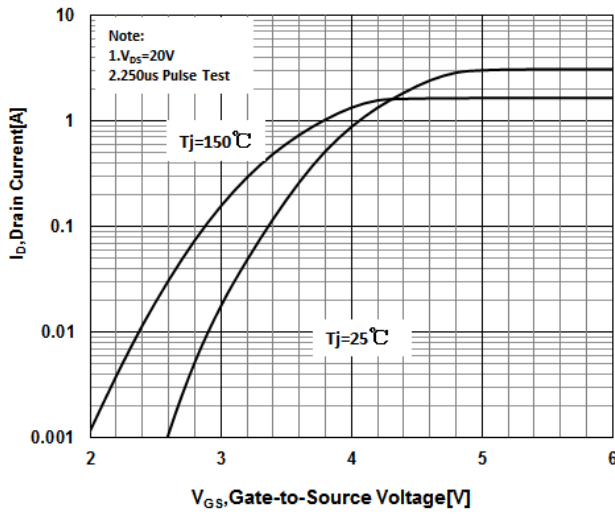


Figure 6. Typical Transfer Characteristics

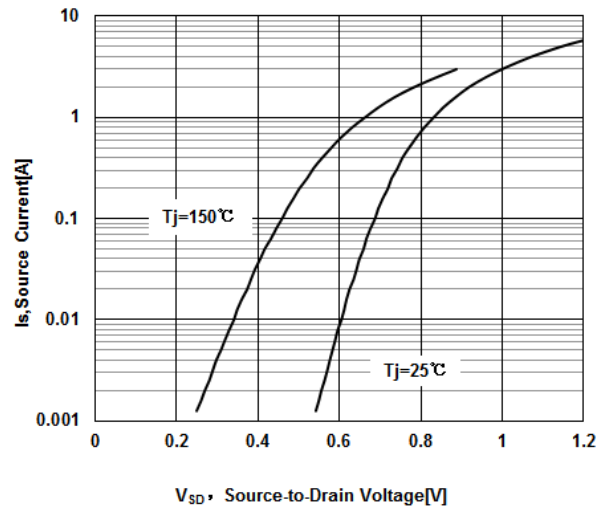


Figure 7. Typical Body Diode Transfer Characteristics

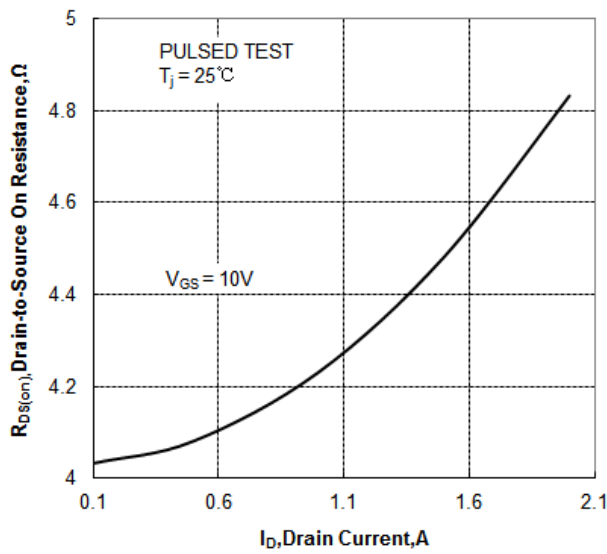


Figure 8. Typical Drain to Source ON Resistance vs Drain Current

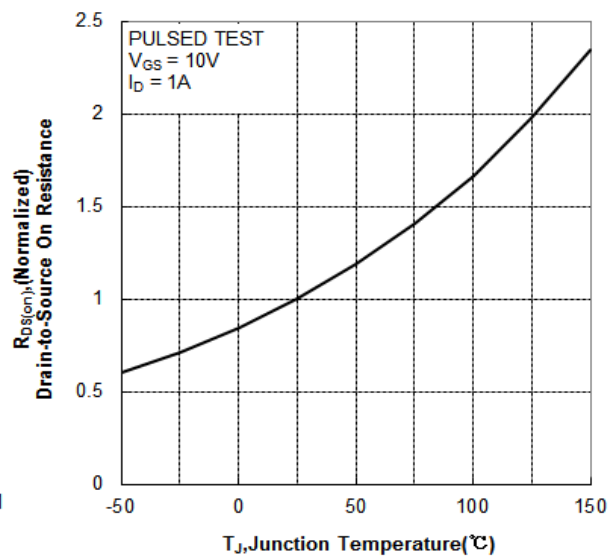


Figure 9. Typical Drain to Source on Resistance vs Junction Temperature

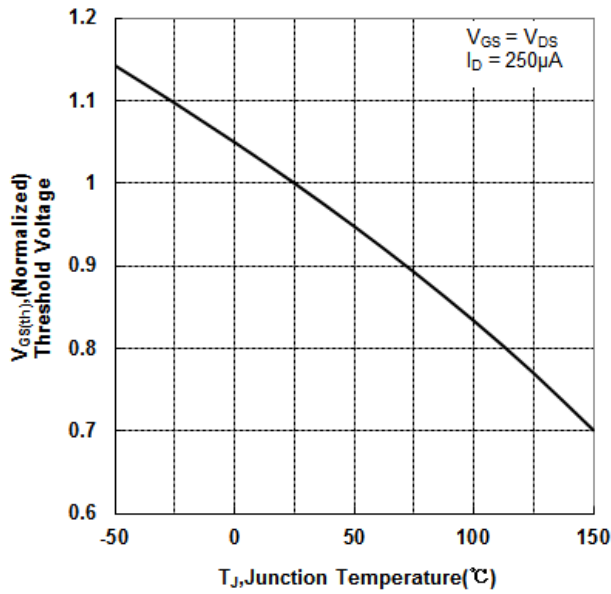


Figure 10. Typical Theshold Voltage vs Junction Temperature

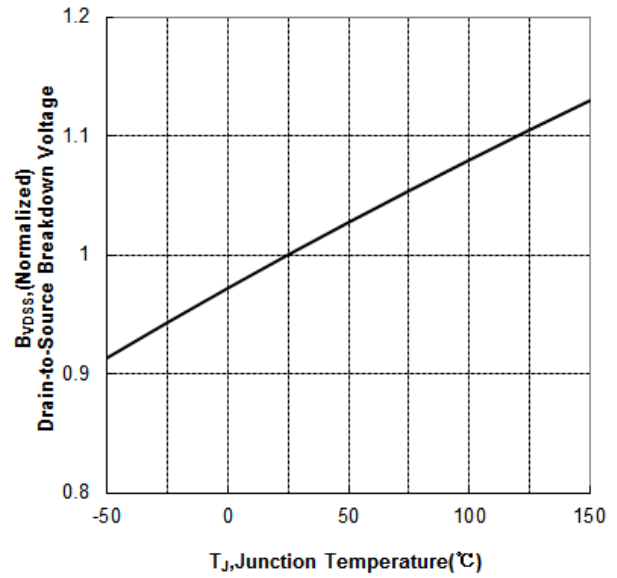


Figure 11. Typical Breakdown Voltage vs Junction Temperature

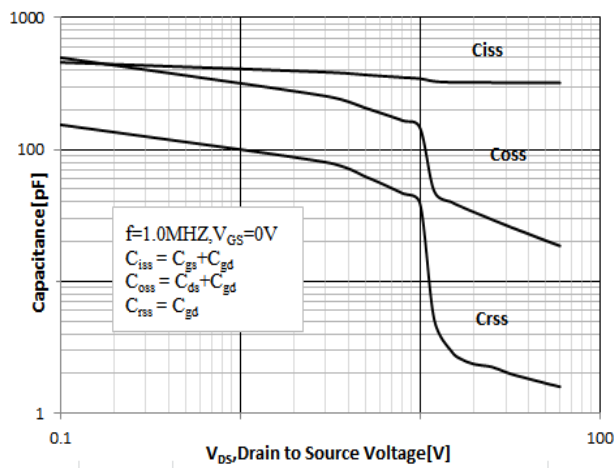


Figure 12 Typical Capacitance vs Drain to Source Voltage

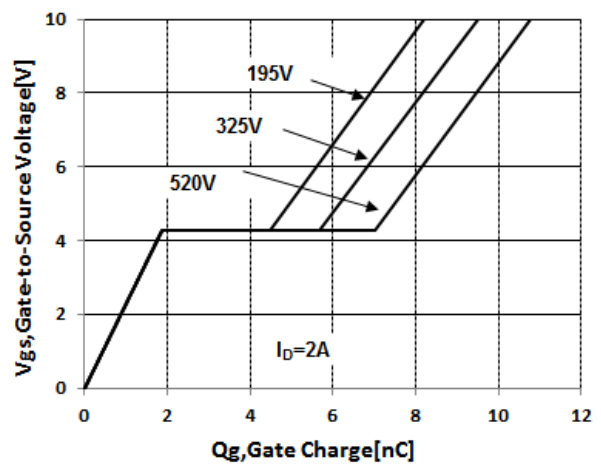


Figure 13 Typical Gate Charge vs Gate to Source Voltage



Test Circuit and Waveform

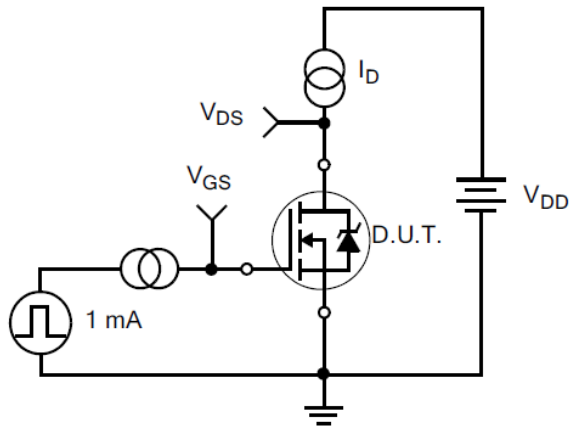


Figure 14. Gate Charge Test Circuit

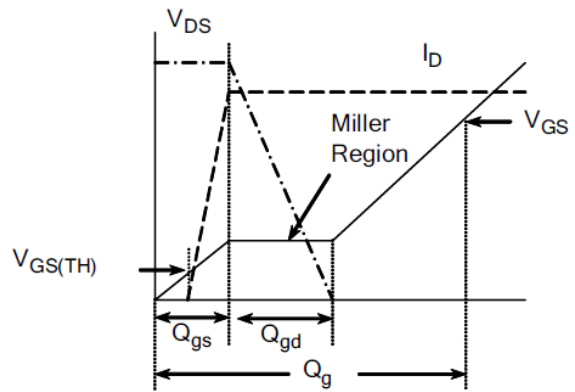


Figure 15. Gate Charge Waveforms

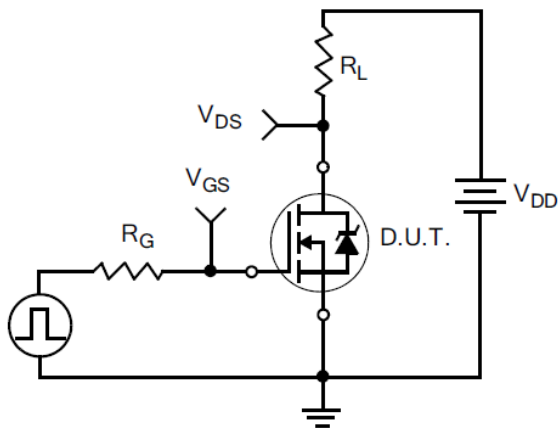


Figure 16. Resistive Switching Test Circuit

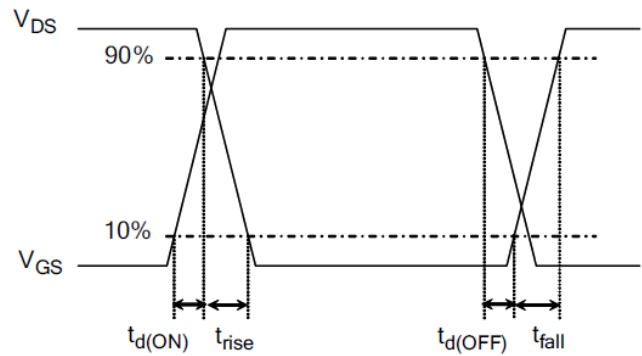


Figure 17. Resistive Switching Waveforms

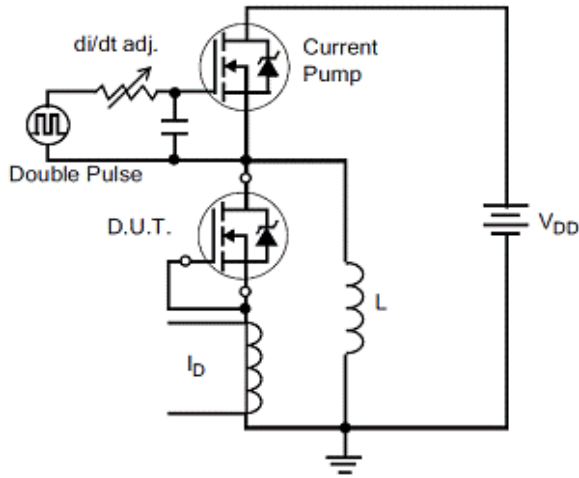


Figure 18. Diode Reverse Recovery Test Circuit

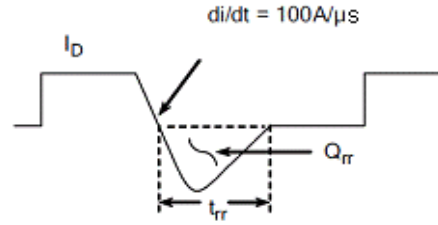


Figure 19. Diode Reverse Recovery Waveform

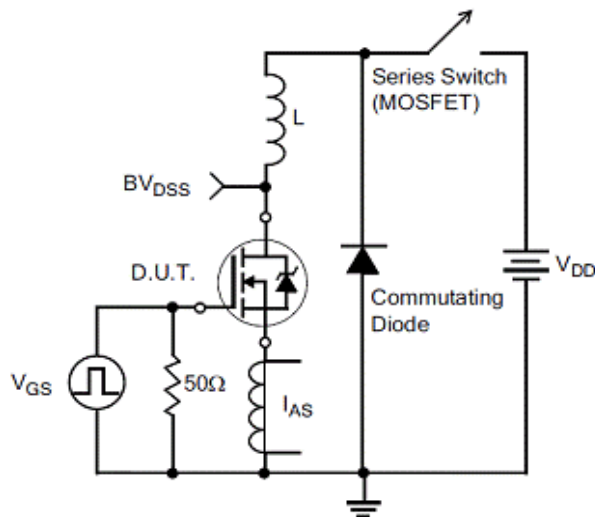


Figure20.Unclamped Inductive Switching Test Circuit

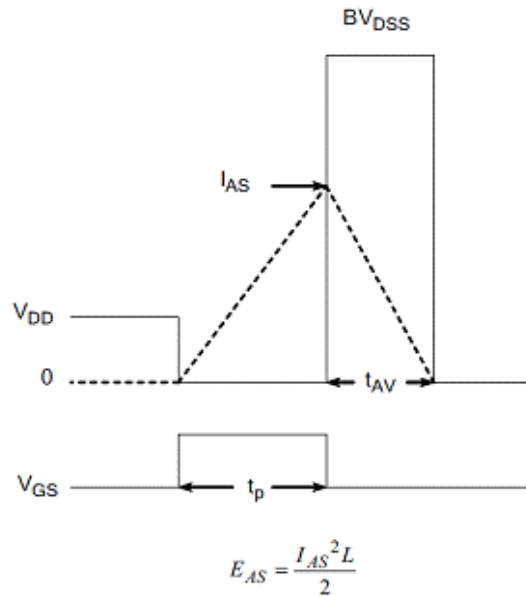


Figure21.Unclamped Inductive Switching Waveform



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