



Description

The SI4559ADY uses advanced trench technology to provide excellent $R_{DS(ON)}$, low gate charge and operation with gate voltages as low as 4.5V. This device is suitable for use as a Battery protection or in other Switching application.

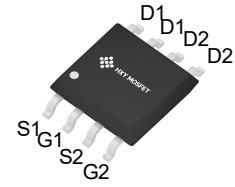
General Features

$V_{DS} = 60V$ $I_D = 6A$

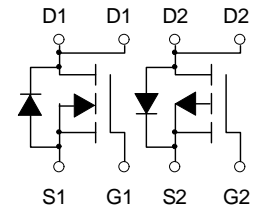
$R_{DS(ON)} < 48m\Omega @ V_{GS}=10V$

$V_{DS} = -60V$ $I_D = -5A$

$R_{DS(ON)} < 85 m\Omega @ V_{GS}=-10V$



SOP-8
(SOIC-8)



N-Channel and P-Channel

Application

Wireless charging

Boost driver

Brushless motor

Ordering Information

Product ID	Pack	Brand	Qty(PCS)
SI4559ADY	SOP-8(SOIC-8)	HXY MOSFET	3000

Absolute Maximum Ratings ($T_C=25^\circ C$ unless otherwise noted)

Symbol	Parameter	Rating		Units
		N-Channel	P-Channel	
VDS	Drain-Source Voltage	60	-60	V
VGS	Gate-Source Voltage	± 20	± 20	V
$I_D @ T_A=25^\circ C$	Continuous Drain Current, $V_{GS} @ 10V^1$	6.0	-5.0	A
$I_D @ T_A=70^\circ C$	Continuous Drain Current, $V_{GS} @ 10V^1$	4.0	-3.5	A
IDM	Pulsed Drain Current ²	11	-8.5	A
EAS	Single Pulse Avalanche Energy ³	22.5	35.3	mJ
IAS	Avalanche Current	22.6	-26.6	A
$P_D @ T_A=25^\circ C$	Total Power Dissipation ⁴	2.5	2.5	W
TSTG	Storage Temperature Range	-55 to 150	-55 to 150	$^\circ C$
T_J	Operating Junction Temperature Range	-55 to 150	-55 to 150	$^\circ C$
$R_{\theta JA}$	Thermal Resistance Junction-Ambient ¹	85		$^\circ C/W$
$R_{\theta JC}$	Thermal Resistance Junction-Case ¹	62.5		$^\circ C/W$



N-Channel Electrical Characteristics ($T_J=25^\circ\text{C}$, unless otherwise noted)

Symbol	Parameter	Test Condition	Min.	Typ.	Max.	Units
Off Characteristic						
$V_{(BR)DSS}$	Drain-Source Breakdown Voltage	$V_{GS}=0V, I_D=250\mu A$	60	-	-	V
I_{DSS}	Zero Gate Voltage Drain Current	$V_{DS}=60V, V_{GS}=0V,$	-	-	1.0	μA
I_{GSS}	Gate to Body Leakage Current	$V_{DS}=0V, V_{GS}=\pm 20V$	-	-	± 100	nA
On Characteristics						
$V_{GS(th)}$	Gate Threshold Voltage	$V_{DS}=V_{GS}, I_D=250\mu A$	1.0	1.6	2.5	V
$R_{DS(on)}$	Static Drain-Source on-Resistance <small>note3</small>	$V_{GS}=10V, I_D=5A$	-	40	48	m Ω
		$V_{GS}=4.5V, I_D=3A$	-	48	60	
Dynamic Characteristics						
C_{iss}	Input Capacitance	$V_{DS}=25V, V_{GS}=0V,$ $f=1.0MHz$	-	1148	-	pF
C_{oss}	Output Capacitance		-	58.5	-	pF
C_{rss}	Reverse Transfer Capacitance		-	49.4	-	pF
Q_g	Total Gate Charge	$V_{DS}=30V, I_D=2.5A,$ $V_{GS}=10V$	-	20.3	-	nC
Q_{gs}	Gate-Source Charge		-	3.7	-	nC
Q_{gd}	Gate-Drain("Miller") Charge		-	5.3	-	nC
Switching Characteristics						
$t_{d(on)}$	Turn-on Delay Time	$V_{DS}=30V, I_D=5A,$ $R_G=1.8\Omega, V_{GS}=10V$	-	7.6	-	ns
t_r	Turn-on Rise Time		-	20	-	ns
$t_{d(off)}$	Turn-off Delay Time		-	15	-	ns
t_f	Turn-off Fall Time		-	24	-	ns
Drain-Source Diode Characteristics and Maximum Ratings						
I_S	Maximum Continuous Drain to Source Diode Forward Current		-	-	6	A
I_{SM}	Maximum Pulsed Drain to Source Diode Forward Current		-	-	20	A
V_{SD}	Drain to Source Diode Forward Voltage	$V_{GS}=0V, I_S=5A$	-	-	1.2	V
t_{rr}	Body Diode Reverse Recovery Time	$I_F=5A, di/dt=100A/\mu s$	-	29	-	ns
Q_{rr}	Body Diode Reverse Recovery Charge		-	43	-	nC

Notes:1. Repetitive Rating: Pulse Width Limited by Maximum Junction Temperature

2. EAS condition : $T_J=25^\circ\text{C}, V_{DD}=30V, V_G=10V, L=0.5mH, R_g=25\Omega, I_{AS}=8.7A$

3. Pulse Test: Pulse Width $\leq 300\mu s$, Duty Cycle $\leq 0.5\%$



P-Channel Electrical Characteristics ($T_J=25^\circ\text{C}$, unless otherwise noted)

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
BV_{DSS}	Drain-Source Breakdown Voltage	$V_{GS}=0V, I_D=-250\mu A$	-60	---	---	V
$R_{DS(ON)}$	Static Drain-Source On-Resistance ²	$V_{GS}=-10V, I_D=-3.5A$	---	70	100	m Ω
		$V_{GS}=-4.5V, I_D=-3.1A$	---	100	115	
$V_{GS(th)}$	Gate Threshold Voltage	$V_{GS}=V_{DS}, I_D=-250\mu A$	-1.0	---	-2.5	V
I_{DSS}	Drain-Source Leakage Current	$V_{DS}=-48V, V_{GS}=0V, T_J=25^\circ\text{C}$	---	---	1	μA
		$V_{DS}=-48V, V_{GS}=0V, T_J=55^\circ\text{C}$	---	---	5	
I_{GSS}	Gate-Source Leakage Current	$V_{GS}=\pm 20V, V_{DS}=0V$	---	---	± 100	nA
g_{fs}	Forward Transconductance	$V_{DS}=-5V, I_D=-3A$	---	8.5	---	S
Q_g	Total Gate Charge (-4.5V)	$V_{DS}=-48V, V_{GS}=-4.5V, I_D=-3A$	---	12.1	---	nC
Q_{gs}	Gate-Source Charge		---	2.2	---	
Q_{gd}	Gate-Drain Charge		---	6.3	---	
$T_{d(on)}$	Turn-On Delay Time	$V_{DD}=-15V, V_{GS}=-10V, R_G=3.3\Omega, I_D=-1A$	---	9.2	---	ns
T_r	Rise Time		---	20.1	---	
$T_{d(off)}$	Turn-Off Delay Time		---	46.7	---	
T_f	Fall Time		---	9.4	---	
C_{iss}	Input Capacitance	$V_{DS}=-15V, V_{GS}=0V, f=1\text{MHz}$	---	1137	---	pF
C_{oss}	Output Capacitance		---	76	---	
C_{rss}	Reverse Transfer Capacitance		---	50	---	
I_S	Continuous Source Current ^{1,5}	$V_G=V_D=0V, \text{ Force Current}$	---	---	-6.0	A
V_{SD}	Diode Forward Voltage ²	$V_{GS}=0V, I_S=-1A, T_J=25^\circ\text{C}$	---	---	-1.2	V

Note :

- 1.The data tested by surface mounted on a 1 inch² FR-4 board with 20Z copper.
- 2.The data tested by pulsed , pulse width $\leq 300\mu s$, duty cycle $\leq 2\%$
- 3.The EAS data shows Max. rating . The test condition is $V_{DD}=-25V, V_{GS}=-10V, L=0.1mH, I_{AS}=-24A$
- 4.The power dissipation is limited by 150 $^\circ\text{C}$ junction temperature
- 5.The data is theoretically the same as I_D and I_{DM} , in real applications , should be limited by total power dissipation.



N-Channel Typical Characteristics

Figure 1: Output Characteristics

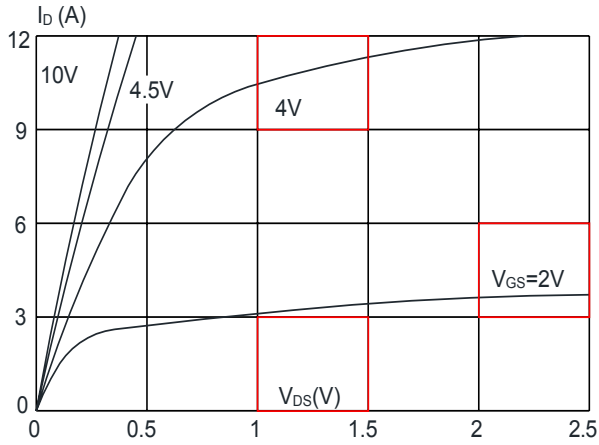


Figure 2: Typical Transfer Characteristics

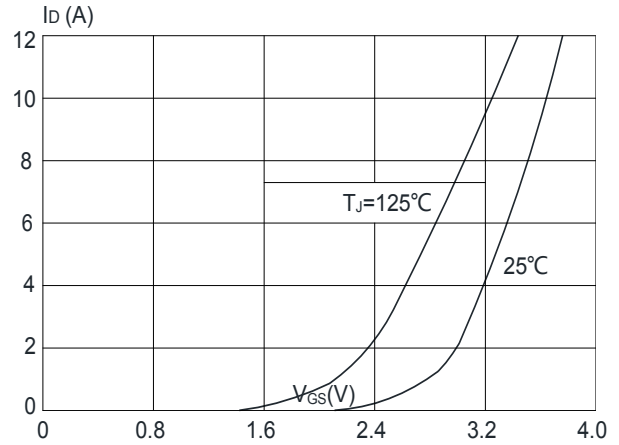


Figure 3: On-resistance vs. Drain Current

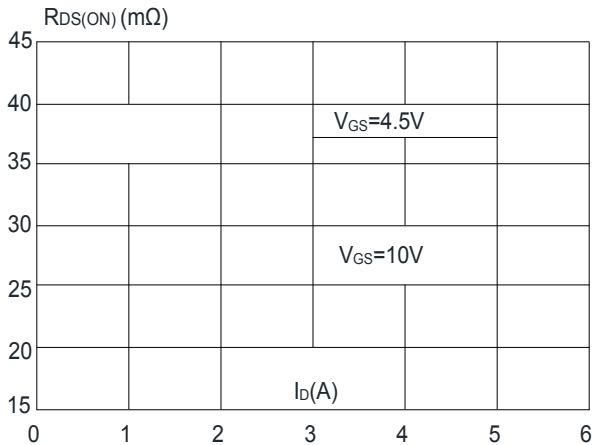


Figure 4: Body Diode Characteristics

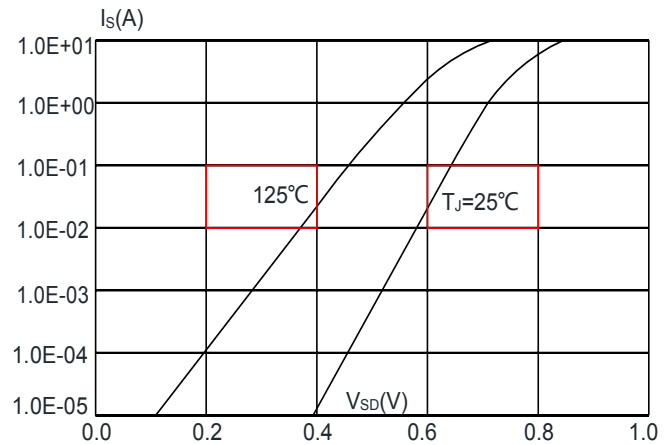


Figure 5: Gate Charge Characteristics

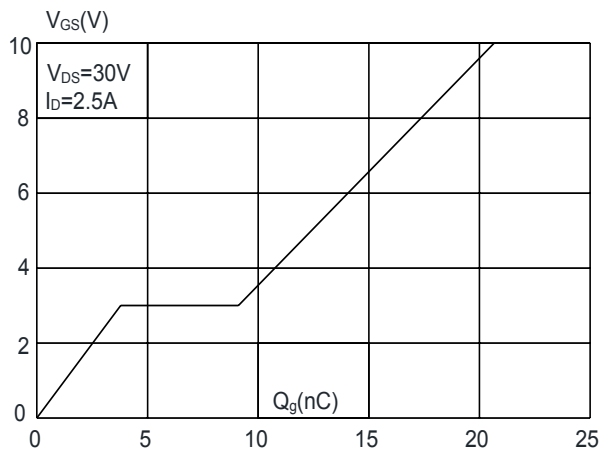


Figure 6: Capacitance Characteristics

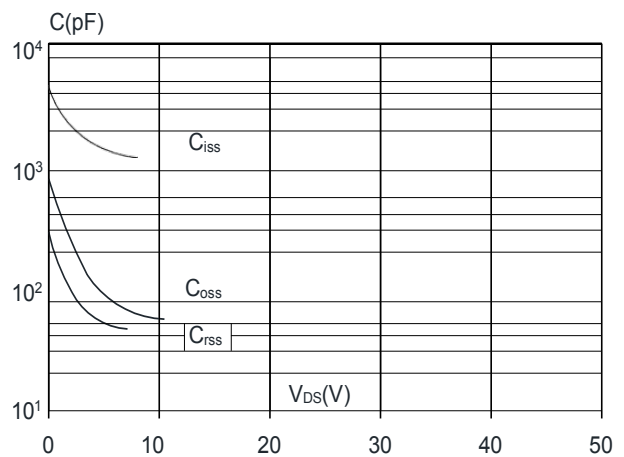




Figure 7: Normalized Breakdown Voltage vs. Junction Temperature

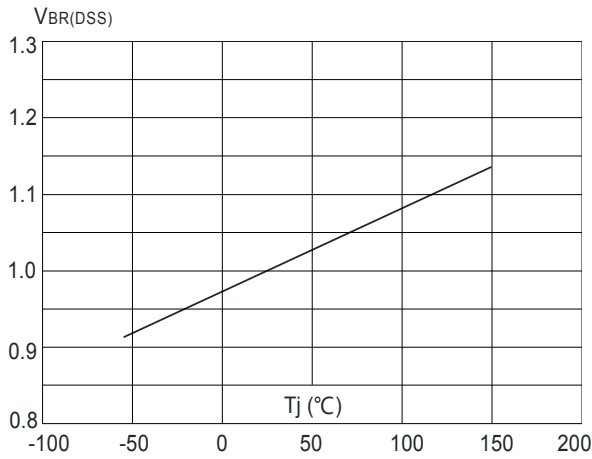


Figure 8: Normalized on Resistance vs. Junction Temperature

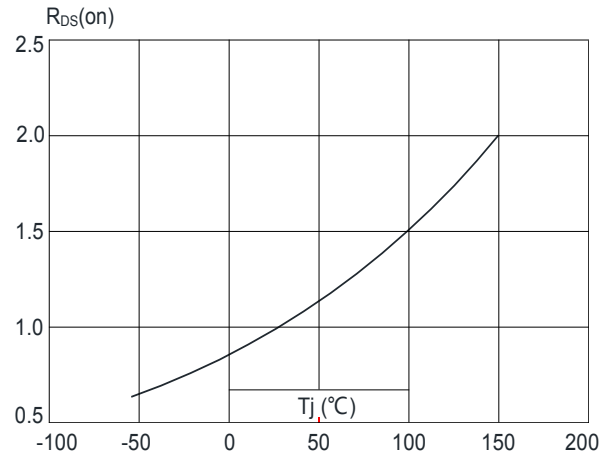


Figure 9: Maximum Safe Operating Area

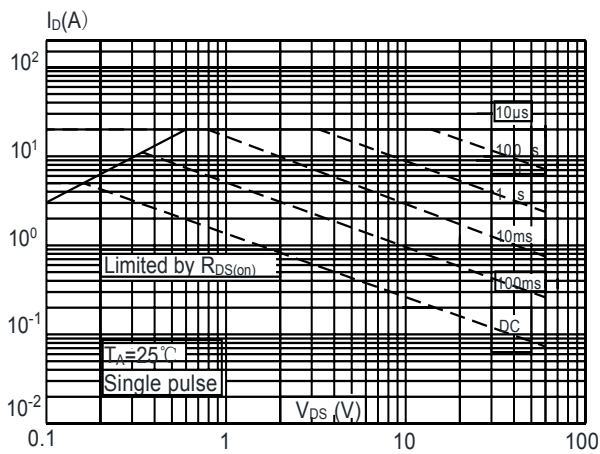


Figure 10: Maximum Continuous Drain Current vs. Ambient Temperature

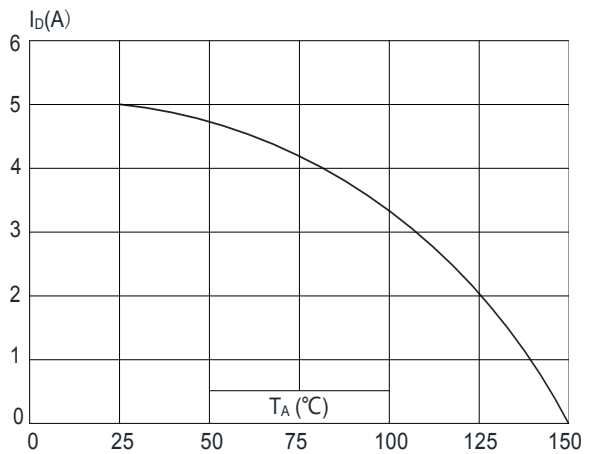
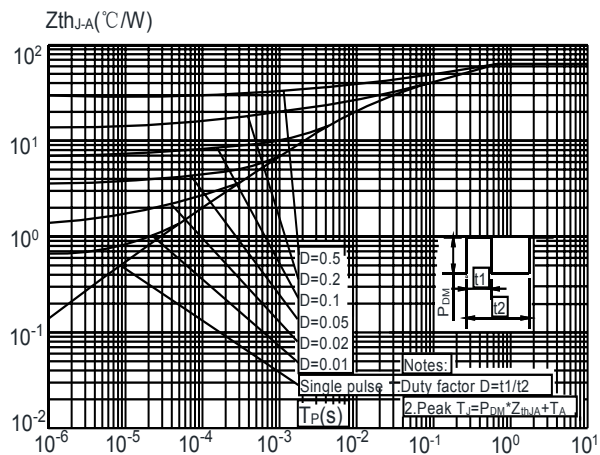


Figure.11: Maximum Effective Transient Thermal Impedance, Junction-to-Ambient





P-Channel Typical Characteristics

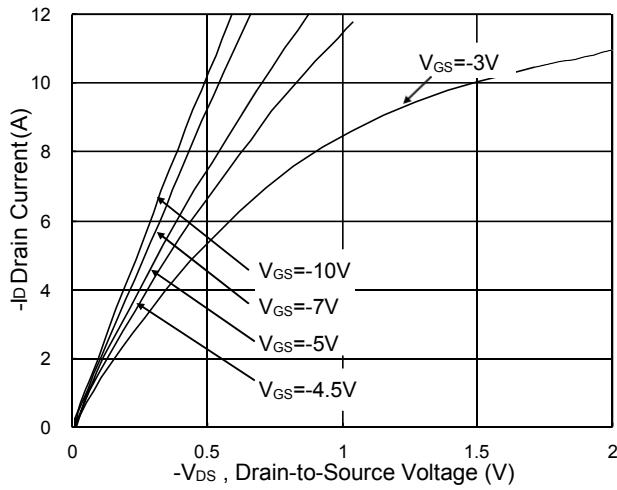


Fig.1 Typical Output Characteristics

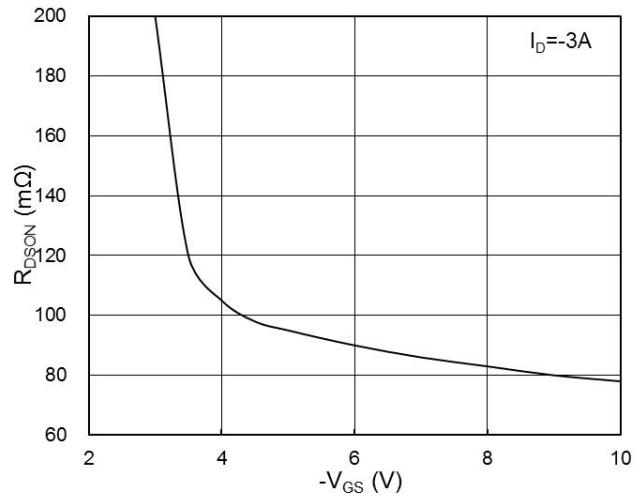


Fig.2 On-Resistance vs. G-S Voltage

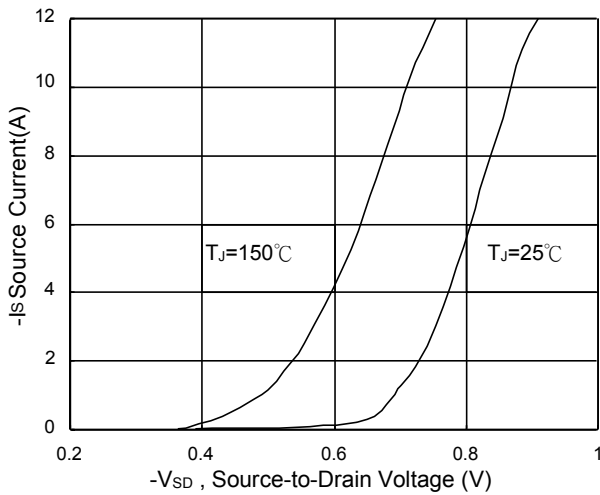


Fig.3 Source Drain Forward Characteristics

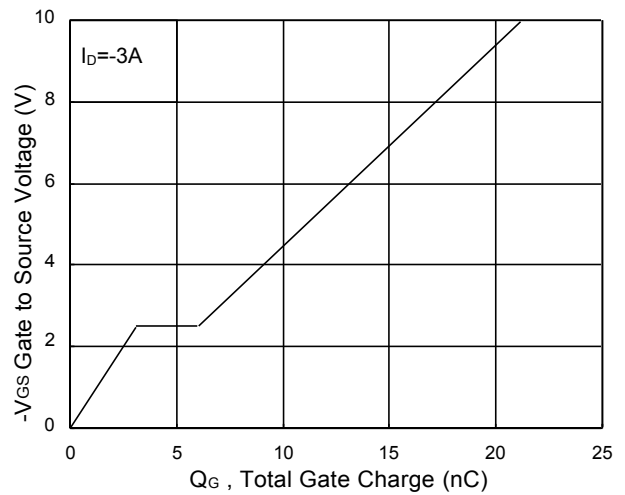


Fig.4 Gate-Charge Characteristics

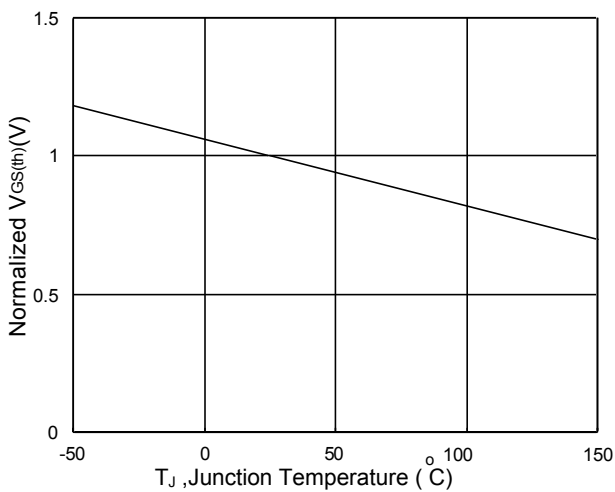


Fig.5 Normalized V_{GS(th)} vs. T_J

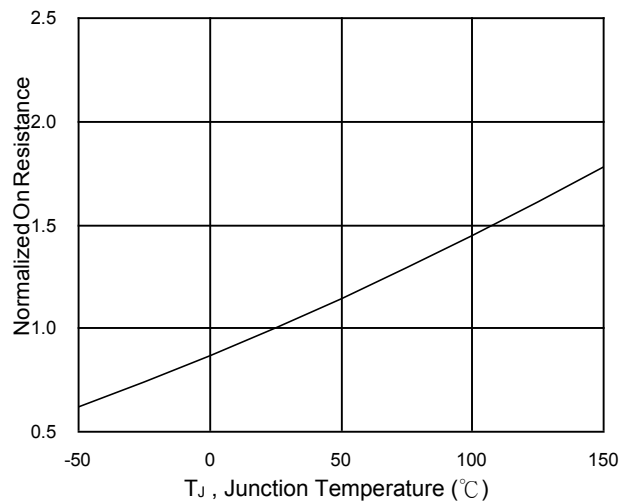


Fig.6 Normalized R_{DS(on)} vs. T_J

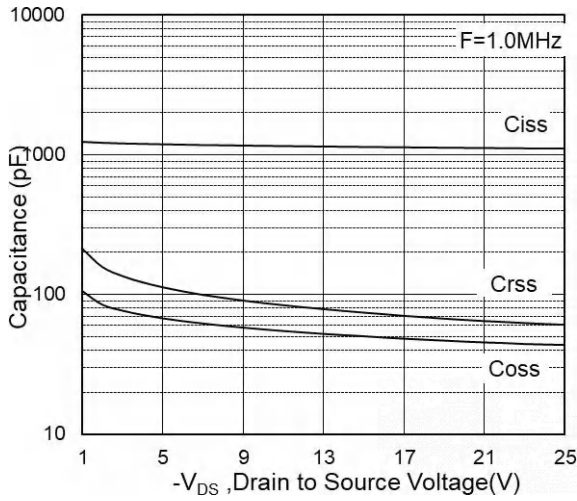


Fig.7 Capacitance

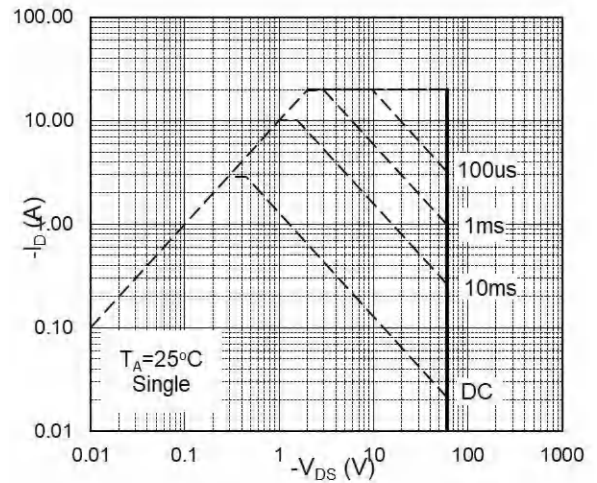


Fig.8 Safe Operating Area

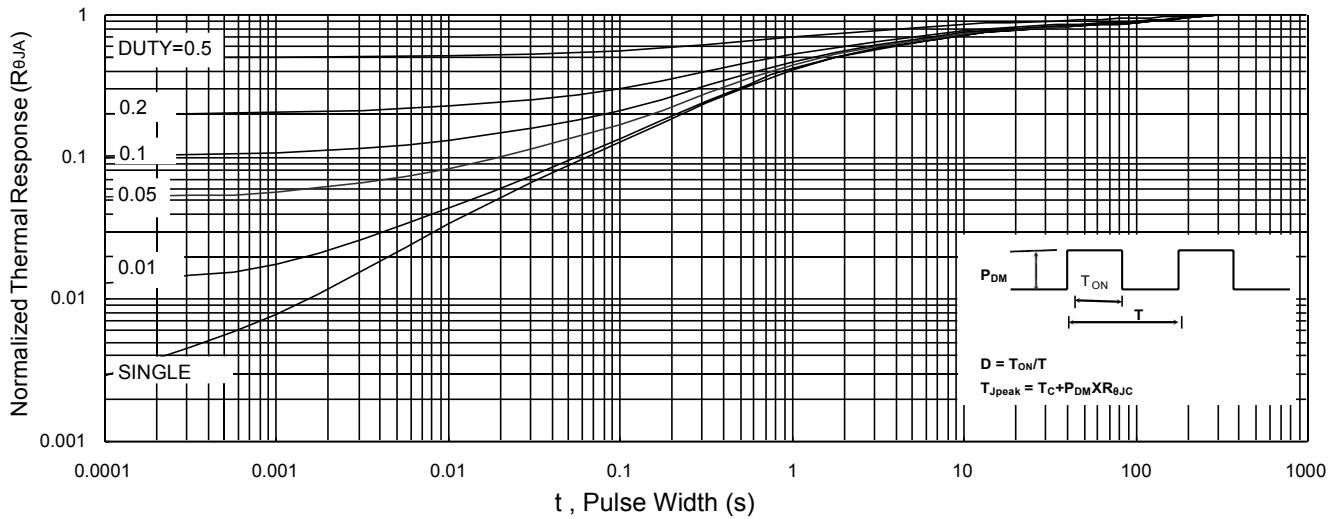


Fig.9 Normalized Maximum Transient Thermal Impedance

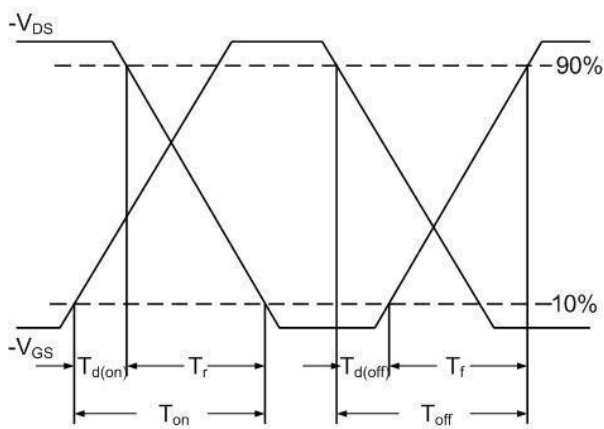


Fig.10 Switching Time Waveform

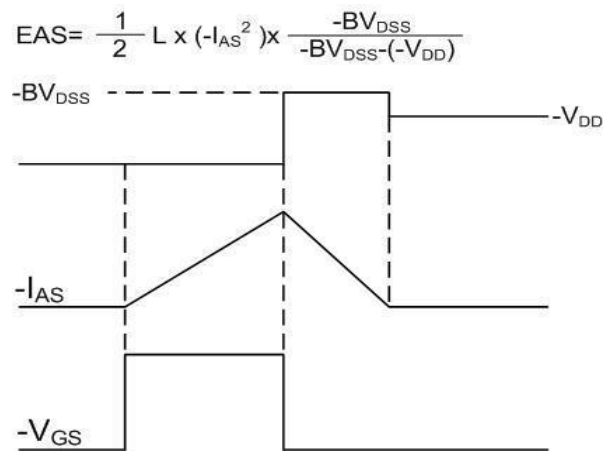
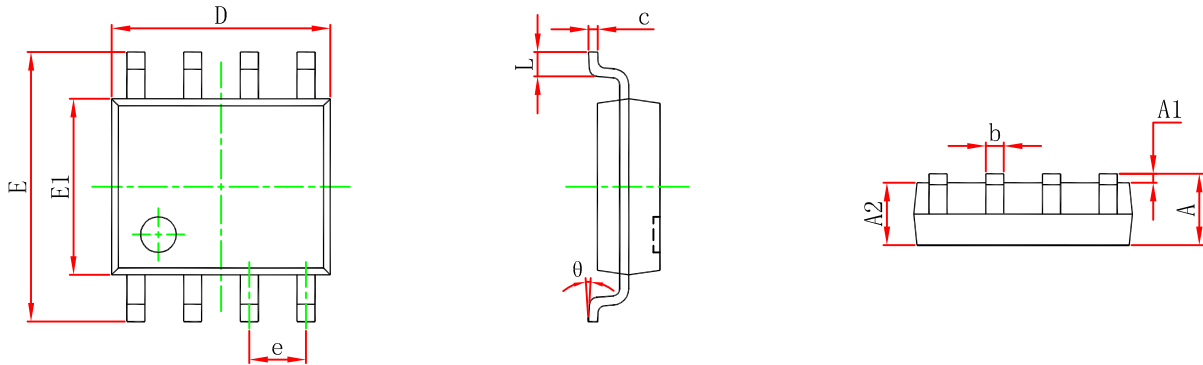


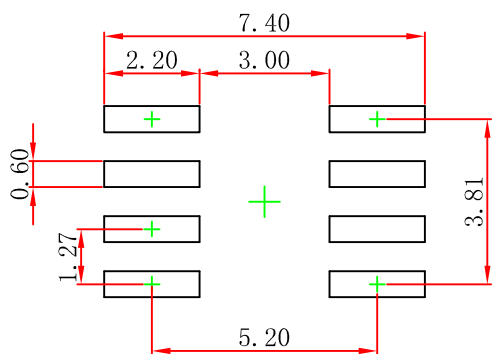
Fig.11 Unclamped Inductive Waveform



SOP-8(SOIC-8) Package Outline Dimensions



Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min	Max	Min	Max
A	1.350	1.750	0.053	0.069
A1	0.100	0.250	0.004	0.010
A2	1.350	1.550	0.053	0.061
b	0.330	0.510	0.013	0.020
c	0.170	0.250	0.007	0.010
D	4.800	5.000	0.189	0.197
e	1.270 (BSC)		0.050 (BSC)	
E	5.800	6.200	0.228	0.244
E1	3.800	4.000	0.150	0.157
L	0.400	1.270	0.016	0.050
θ	0°	8°	0°	8°



- Note:
1. Controlling dimension: in millimeters.
 2. General tolerance: $\pm 0.05\text{mm}$.
 3. The pad layout is for reference purposes only.



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