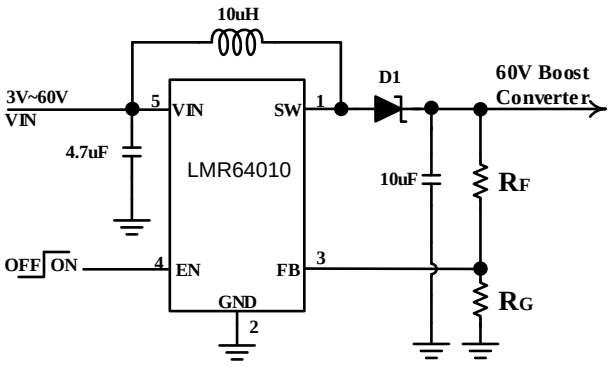
High-Efficiency Asynchronous Boost/Buck-Boost Converter with 60V/1.2MHz Switching and 2A Peak Current

Features

- All ports feature ±2000V (HBM) ESD protection
- Wide input/output voltage range: 3.0V–60V
- Built-in 350mΩ high-side MOSFET
- Up to 90% boost efficiency
- Cycle-by-cycle peak current limit protection
- SKIP mode for ultra-high light-load efficiency
- Available in compact SOT23-5 and thermally enhanced ESOP8 packages
- Built-in soft-start circuit to prevent inrush current
- Thermal shutdown protection
- Input undervoltage protection (UVLO)
- Internal loop compensation reduces solution size, cost, and design complexity
- Junction temperature range: -40°C to +125°C



Note:

- **EN must not float.** The chip starts when EN voltage exceeds 0.6V and shuts down when below 0.3V.
- **EN is a low-voltage pin.** Use a voltage divider from VIN for proper operation.

Applications

- Battery-powered devices
- Industrial distributed power systems

SOT23-5

Ordering Information

Part Number	Package	Top Mark
LMR64010XMFX	SOT23-5	6302
LMR64010XMF	ESOP8	R64010

Absolute Maximum Ratings†

Table 3.1:

Parameter	Range
Pin-to-GND voltage (VIN, SW)	-0.3V~60V
Pin-to-GND voltage (FB, EN)	-0.3V~6V
Switch current limit	2A
Storage temperature	-65℃ to 150℃
Operating temperature	-40℃ to 125℃
Operating temperature	±2KV
ESD rating (CDM)	±500V

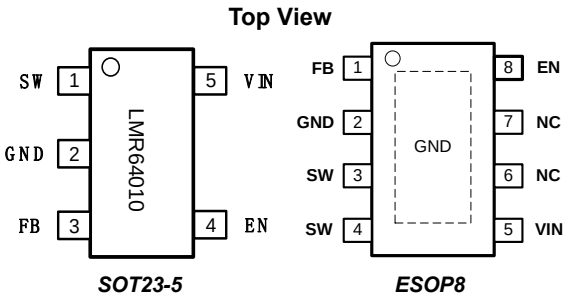
† Note: Exceeding these limits may cause permanent damage. These are stress ratings only; prolonged operation under these conditions may affect reliability.

ESD Warning

ESD-Sensitive Device.

Charged devices and boards may discharge unnoticed. Despite built-in protection circuits, high-energy ESD events may damage the device. Proper ESD precautions must be taken to avoid degradation or failure.

Pin arrangement



Packaging and Pin Arrangement

Table 3.2: Pin Descriptions

Pin number		Name	*Description*
SOT23	ESOP8		
1	3,4	SW	Internal power switch node. Connect to external inductor and Schottky diode.
2	2	GND	Ground.
3	1	FB	Feedback input. Connect to external resistors to set output voltage.
4	8	EN	Enable pin. Drive high (>0.6V) to enable, low (<0.3V) to disable.
5	5	VIN	Power input. Bypass with ≥4.7μF ceramic capacitor near VIN and GND.
-	6,7	NC	No connection. Leave floating.

Electrical Characteristics

Unless otherwise noted, specifications apply at TJ = -40°C to +125°C. Typical values are at TJ = 25°C.

Table 4: Electrical Specifications

Parameter		Test Conditions	Min	Typ	Max	Unit
Input Characteristics						
V_{IN}	Input voltage range		3.0		60	V
V_{UVLO}	UVLO threshold	Rising		3.0		V
		Falling		2.6		V
I_Q	IQ (quiescent)	No load，No Switch,VIN=12V		180		μA
I_S	ISD (shutdown)	EN=0, VIN=12V		10		μA
Switching Characteristics						
$R_{DS(ON)}$	Power switch RDS(ON)	TJ= 25℃	330	350	410	mΩ
f_{SW}	Switching frequency (PWM mode)	PWM Operation	1.05	1.2	1.35	MHZ
f_{SW_FB}	Soft-start frequency (VIN=12V, EN=1)	VIN=12V，EN=1		$1/4\,F_{sw}$		MHZ
D_{MAX}	Maximum duty cycle			90		%
$I_{LIMIT.SW(Peak)}$	SW peak current limit	VIN=5V	1.5	1.7	2.1	A
V_{FB}	FB feedback voltage		1.195	1.2	1.205	V
$I_{FB.BIAS}$	FB bias current			50		nA
$I_{SW.LKG}$	SW leakage current				4	μA
Enable (3V≤VIN≤60V)						
V_{EN_H}	EN rising threshold	EN=0 ⤴ EN=1		0.5		V
V_{EN_L}	EN falling threshold	EN=1 ⤵ EN=0		0.4		V
I_{EN}	EN input current	V_{EN}=5V	5		10	μA
Thermal Protection						
T_{OTP-R}	OTP threshold (rising)	TJ Rising		150		℃
T_{OTP-F}	OTP release (falling)	TJ Falling		120		℃
Thermal Resistance (1)						
θ_{JA}	Junction-to-ambient	0 LFPM Air Flow		210		℃/W
θ_{JB}	Junction-to-board			38.4		℃/W
θ_{JCtop}	Junction-to-case top			122		℃/W
Ψ_{JB}	Thermal characterization parameter			37.5		℃/W

(1) Combined with simulation data, provided for reference only.

Functional Block Diagram

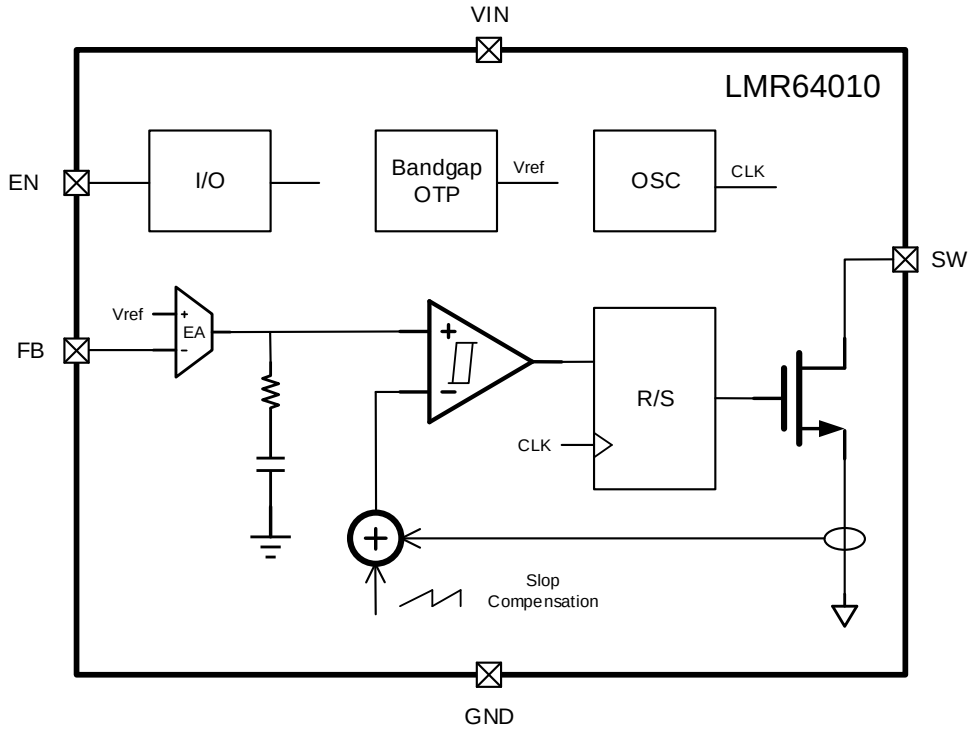


Figure 4: Internal Functional Block Diagram

Application Circuits

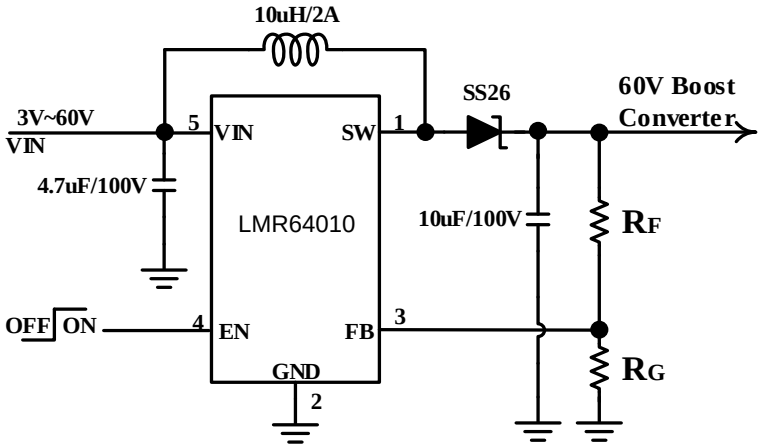


Figure 5.a: Boost Converter Typical Application

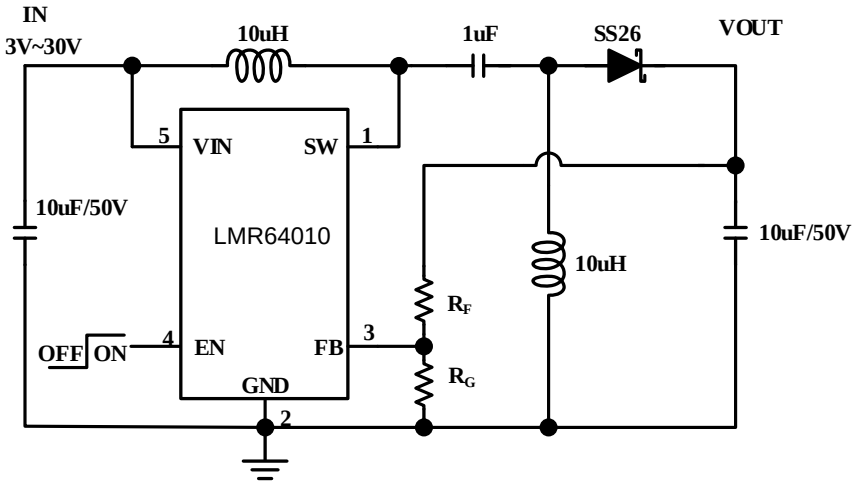


Figure 5.b: Buck-Boost Converter Typical Application

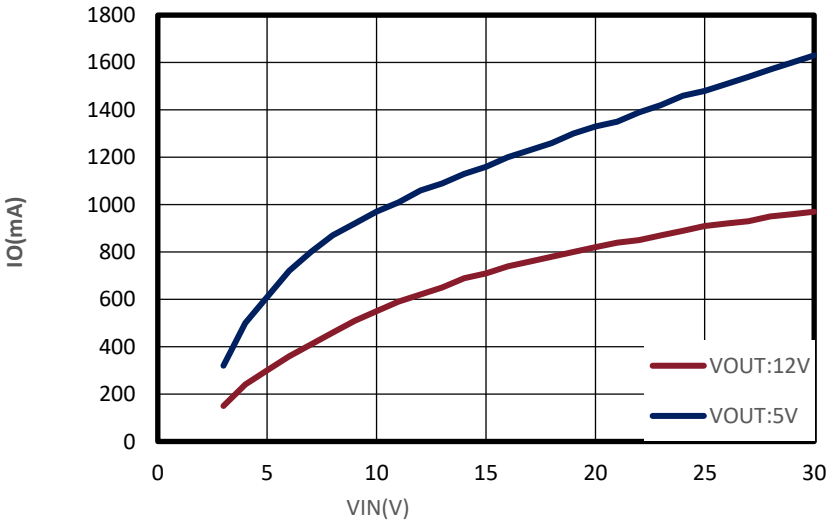


Figure 5.c: Load Current vs. Input Voltage

Application Information:High Efficiency Asynchronous Boost Converter

Summary

LMR64010 is an asynchronous boost converter chip that integrates power switches, with a wide input voltage range of 3V to 60V. It integrates soft start to minimize the need for external surge suppression components, making it an ideal choice for wide input power range boost converters.
The output current can be adjusted through an external resistor Equipped with an integrated 350m Ω power switch, it can provide a peak current capability of at least 2A, and has excellent load and line transient response. Equipped with SKIP control mode, it combines low static current with high switching frequency to achieve high efficiency over a wide range of load currents.
Additional features include: soft start, hot shutdown, UVLO undervoltage lock, and cycle by cycle current limit protection.

Setting Output Voltage

The output current of LMR64010 can be adjusted by an external resistor voltage divider to regulate the magnitude of the output voltage. The recommended output resistance values are shown in the table below.
The voltage divider network consists of RG and RF, **please ensure that RG is less than or equal to 30K**.
The converter regulates the output voltage by keeping the voltage on the FB pin equal to the internal reference voltage VREF.
Once RG is selected, the RF value can be chosen based on VFB, with a typical VFB value of 1.2V:

$$V_{OUT} = 1.2 \times \frac{R_F + R_G}{R_G} \quad (V)$$

Table 6: Output Voltage Configurations

VOUT	RF	RG	Setting error (1)	
6V	13K	3.3K	6.09V	1.53%
9V	30K	4.7K	9.165V	1.83%
12V	33K	3.6K	12.21V	1.81%
27V	390K	18K	27.2V	0.76%
36V	240K	8.2K	36.33V	0.91%
48V	240K	6.2K	48.36V	0.75%

(1) Other voltage divider resistor pairs and high-precision resistors can also be selected to achieve higher setting accuracy

SKIP pulse skipping mode

LMR64010 has a built-in pulse circuit; When under light load, the circuit is turned on; Only switch when necessary to maintain the output voltage within the specified range. This can reduce switch losses and maintain high efficiency of the converter under light load conditions.
In pulse skipping mode, when the output voltage drops below the specified value, LMR64010 enters PWM mode and stays for several oscillator cycles to raise the output voltage to the specified range. During the waiting time between sudden pulses, the power switch is turned off and all load currents are provided by the output capacitor. Due to the periodic sudden drops and recovery of the output voltage, the ripple of the output voltage in this mode is greater than that in the PWM working mode.

Input Undervoltage Protection (UVLO)

There is an internal undervoltage lockout circuit on the VIN pin of the device. When the VIN voltage drops below the threshold of UVLO, UVLO protection will be triggered and the regulator output will be turned off. The rising threshold of the UVLO is about 3.0V. When VIN reaches this voltage and the UVLO is removed, the controller will enter the soft start process.

Maximum duty cycle DMAX

When BOOST is in the maximum duty cycle operating state, the low-end N-channel MOSFET is in the on state, minimizing the turn off time. Under maximum duty cycle operating conditions, since the input voltage is the product of the output voltage value and (1-D_MAX), when the input voltage is fixed, the duty cycle reaches its maximum and the output voltage drops below the regulation range.

Soft-Start

The soft start of LMR64010 can prevent underdamped

and overshoot of the input power supply of the converter during the startup process. When the chip starts up, the internal circuit generates a soft start voltage (SS), and the switching frequency decreases to 1/4 of the maximum switching frequency, causing the current to rise at a fixed rate. During soft start, the output voltage will track the internal node voltage ramp proportionally. When it is smaller than the internal reference (REF), SS covers REF, so the error amplifier uses SS as a reference. When SS exceeds REF, REF resumes control. Throughout the entire startup phase, the switch current limitation remains effective, which can reliably avoid situations where power is applied and short circuits occur.

When the output has a very large capacitance (such as 2200uf or even larger), the output voltage rise speed will be slower than SS, limited by the maximum switch current limit, and the time to start to the target voltage setting value will be extended.

Application Information: High Efficiency Asynchronous Boost Converter (Overview)

The role of EN

BOOST's enable input pin. Drive EN to a high level state to activate the BOOST converter; Drive EN to a low level state to turn off the BOOST converter. This pin has two independent thresholds. When the rising threshold is greater than 0.5V, the output is enabled. When the falling threshold is less than 0.4V, the regulator output is turned off and the low-power sleep mode is entered. External logic signals can be used to drive EN inputs for system sorting and protection. Due to weak internal pull-down, it is not recommended to leave this pin hanging for reliable shutdown of external pull-down resistors.

Table 7. Working status of pin EN

Pin	direction	Pin status	function
EN	input	HIGH	BOOST Output Enable
		LOW	BOOST Output off

OTP overheat protection

The thermal overload protection circuit limits the junction temperature to below 150 ℃ (typical value). Under extreme conditions (i.e. high ambient temperature and/or high power consumption), when the junction temperature starts to rise above 150 ℃, the Over Temperature Protection (OTP) is activated and the system will forcibly shut down the regulator output (if EN is enabled). When the junction temperature drops below 130 ° C, the OTP state will unlock, the regulator output will restart, and the output current will return to normal operating value.

Thermal overload protection aims to protect devices from the effects of momentary accidental overload conditions.

The guaranteed operating junction temperature range of this device is -40 ° C to 125 ° C. High junction temperature will reduce the working life; When the junction temperature remains high at 125 ° C for a long time, the lifespan of the device will be shortened. Please note that the maximum ambient temperature consistent with these specifications depends on specific operating conditions, circuit board layout, rated package thermal resistance, and other environmental factors.

The junction temperature (TJ, unit: ℃) is calculated based on the ambient temperature (TA, unit: ℃) and power consumption (PD, unit: W), using the following formula:

$$T_J = T_A + (P_D \times \theta_{JA})$$

Among them, θ JA (unit: ℃/W) is the thermal resistance of the package. The calculation method and thermal resistance model are detailed in the "High Temperature Considerations" section.

Switch current limiting protection

The regulator output has a cycle by cycle overcurrent

limitation. When SW current triggers Limit. SW (Peak), BOOST output will enter a cycle by cycle current limiting state.

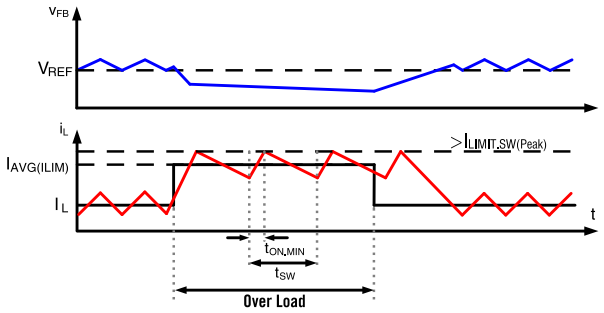


Figure 7. BOOST output overcurrent to Mtop behavior description

$I_{LIMIT.SW}$ (Peak) is related to inductance size and input voltage difference, while $I_{LIMIT.SW}$ (Peak) only
To reference the minimum value. When there is a prolonged overcurrent or short circuit, it may trigger global OTP protection.

Application information: High efficiency asynchronous boost converter (chart)

Figure 8.Electrical Characteristics vs Temperature(Unless otherwise specified, TA=25℃)

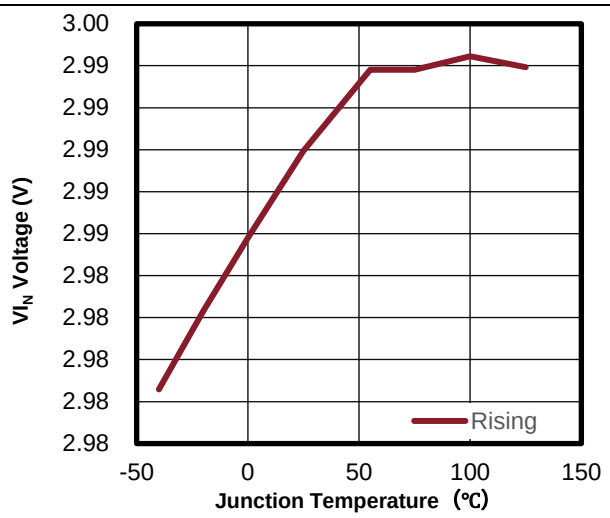


Figure 8.a UVLO Rising vs Temperature

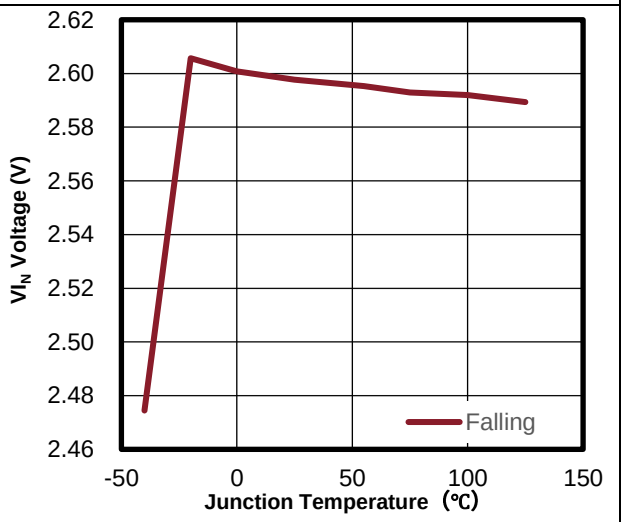


Figure 8.b UVLO Falling vs Temperature

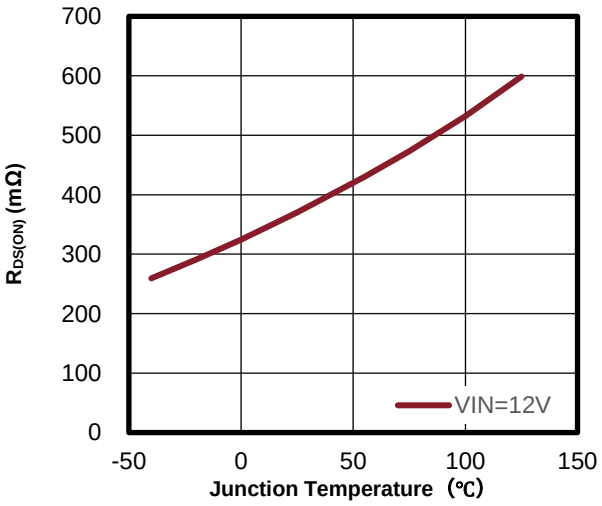


Figure 8.c $R_{DS}(ON)$ vs Temperature

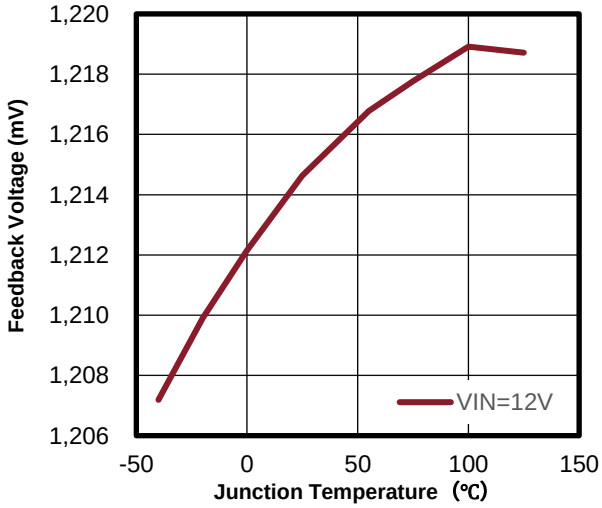


Figure 8.d FB Voltage vs Temperature

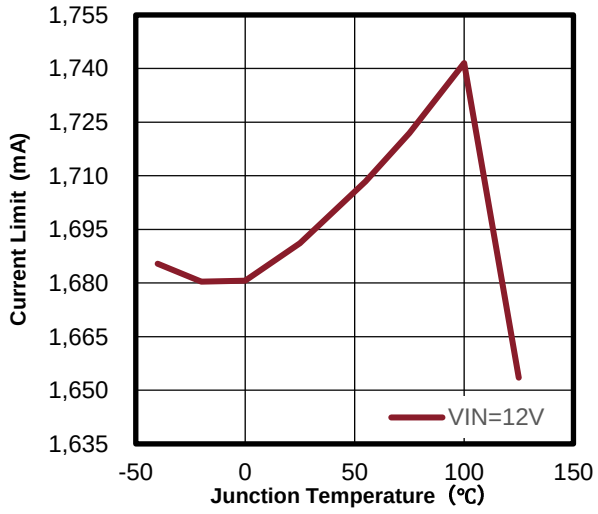


Figure 8.e Current Limit vs Temperature

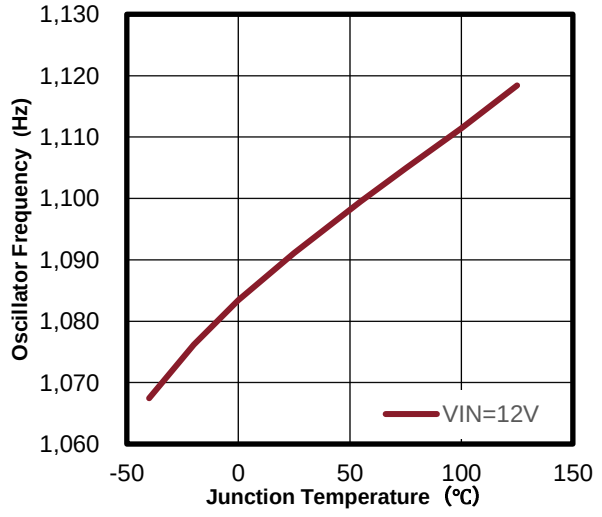


Figure 8.f f_{SW} (OSC) vs Temperature

Application information: High efficiency asynchronous boost converter (chart)

Figure 9.Efficiency vs Load Current(Unless otherwise specified, TA=25℃)

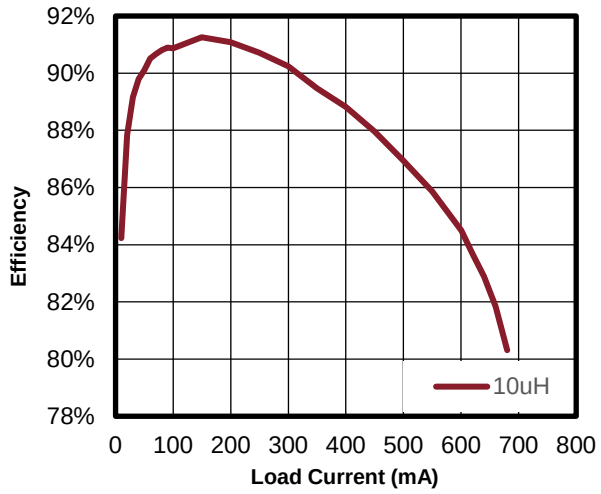


Figure 9.a V_{IN}=3.3V V_{OUT}=5V

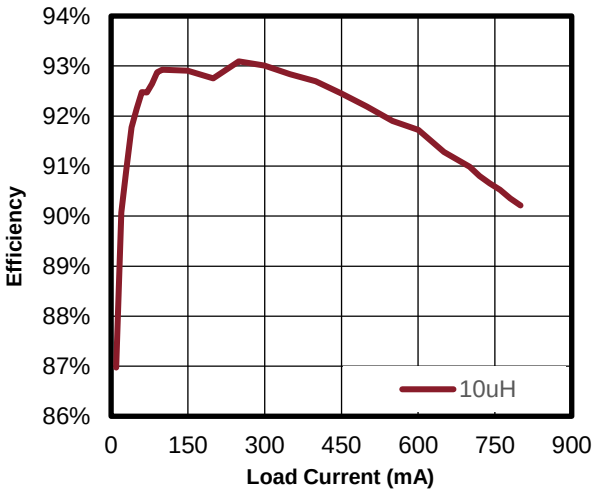


Figure 9.b V_{IN}=4.2V V_{OUT}=5V

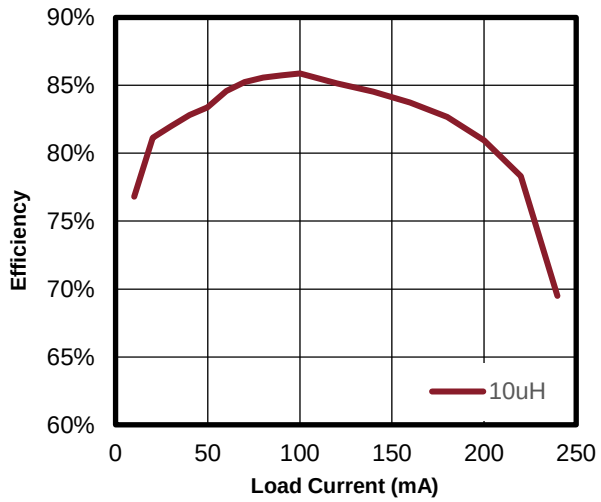


Figure 9.c V_{IN}=3.3V V_{OUT}=12V

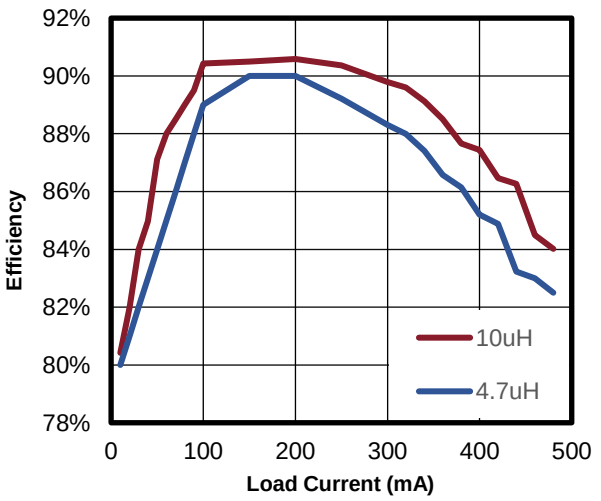


Figure 9.d V_{IN}=5V V_{OUT}=12V

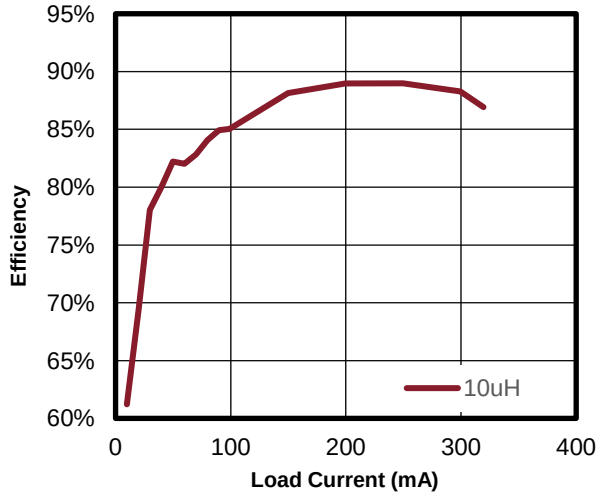


Figure 9.e V_{IN}=9V V_{OUT}=24V

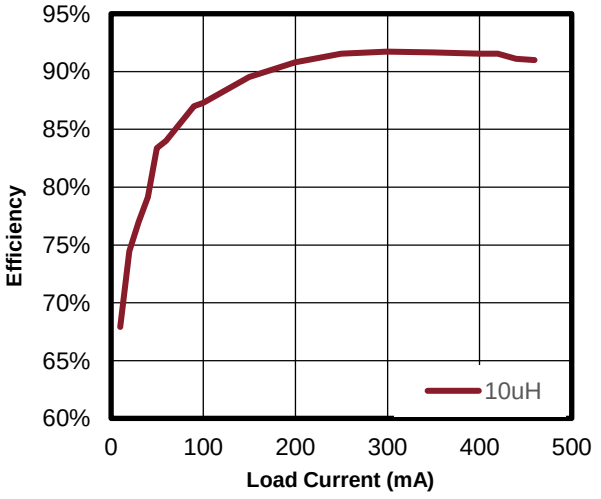


Figure 9.f V_{IN}=12V V_{OUT}=24V

Application information: High efficiency asynchronous boost converter (chart)

Figure 10. Oscilloscope waveform(Unless otherwise specified, TA=25℃)

Start-up Waveforms
NO LOAD

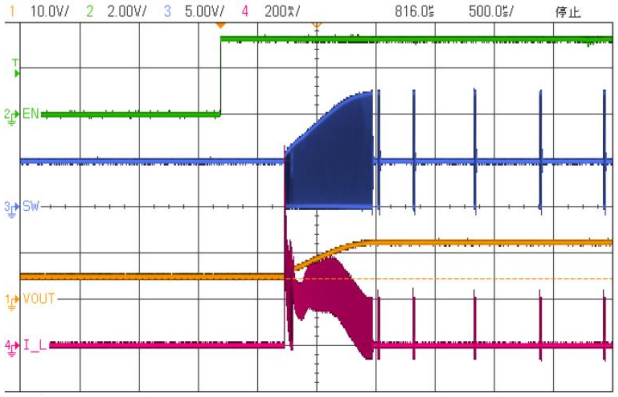


Figure 10.a 5V_{IN} to 12V_{OUT},NO LOAD
L=10uH, C_{OUT}=10uF,C_{IN}=4.7uF

Start-up Waveforms
30R LOAD

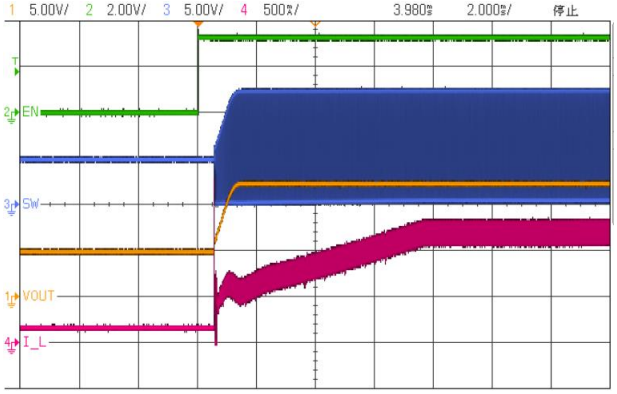


Figure 10.b 5VIN to 12VOUT, LOAD=30R
L=10uH, COUT=10uF, CIN=4.7uF

Switching Waveforms
PWM Mode

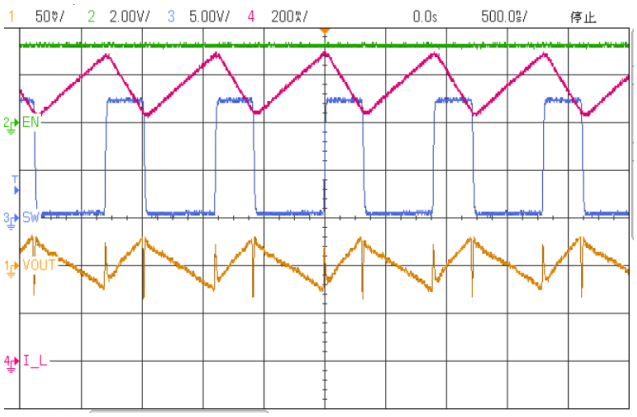


Figure 10.c V_{IN} =5V, V_{OUT}(AC)=12V, LOAD=400mA
L=10uH, C_{OUT}=10uF, C_{IN}=4.7uF

Switching Waveforms
Burst Mode Operation

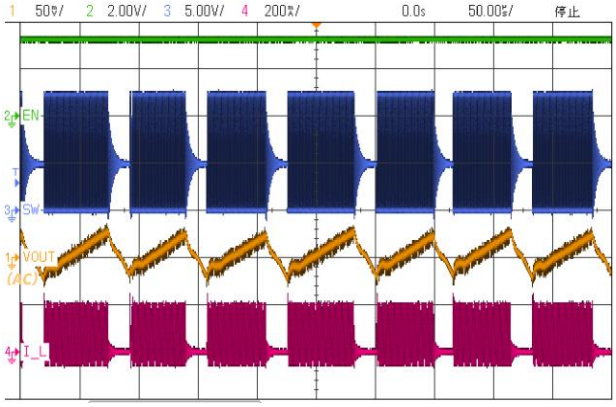


Figure 10.d V_{IN} =5V, V_{OUT}(AC)=12V, LOAD=20mA
L=10uH, C_{OUT}=10uF, C_{IN}=4.7uF

Switching Waveforms
Pulse Skip Mode

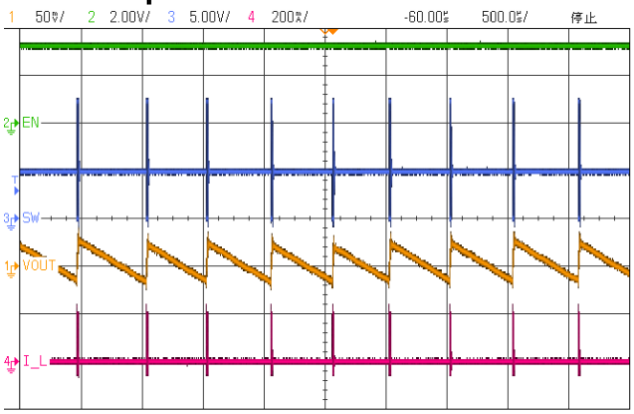


Figure 10.e V_{IN} =5V, V_{OUT}(AC)=12V,LOAD=1mA

OTP Waveforms
PWM Mode

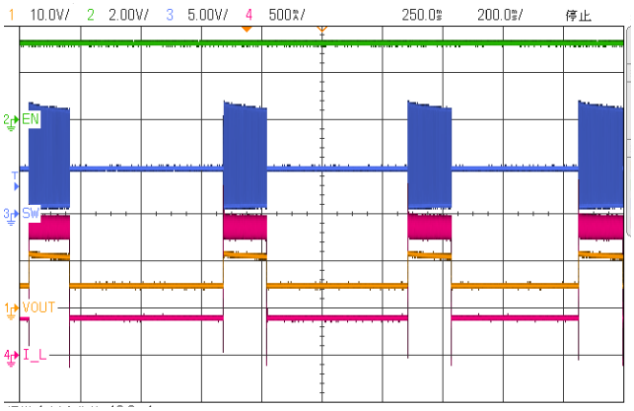


Figure 10.f V_{IN} =5V, V_{OUT}=12V,LOAD=400mA

$L=10uH, C_{OUT}=10uF, C_{IN}=4.7uF$	$L=10uH, C_{OUT}=10uF, C_{IN}=4.7uF$

Application Information: Device Selection Suggestions and Calculations

Freewheeling diode

LMR64010 requires an external freewheeling diode between the SW pin and the output. The reverse voltage rating of the selected diode must be greater than VOUTMAX, and the peak rated current of the diode must be greater than the maximum inductor current. Due to the low forward voltage drop and fast switching speed of Schottky diodes, it is recommended to use Schottky diodes for optimal efficiency.

Usually, the higher the voltage and current rating of a diode, the higher the forward voltage. If the output voltage is V_OUT, it is recommended to choose a diode with a minimum reverse voltage of 4／3 V_OUT. The rated reverse breakdown voltage of the diode must be selected appropriately and leave appropriate margin for possible ringing on the SW node.

It is generally not recommended to use so-called 'ultrafast recovery' diodes. When running in continuous mode, the reverse recovery time displayed by the "ultrafast" diode will cause a slingshot effect. The internal power switch will increase the VIN current entering the diode to restore it. Then, when the diode is finally turned off, several tens of nanoseconds later, the SW node voltage rises at an extremely high d_v／d_t, perhaps 5 to 10V/ns! Combining real-world inductors, SW nodes can easily surpass VIN tracks. This may lead to poor RFI performance, and if the overshoot is severe enough, it may damage the IC itself.

Due to the fact that the freewheeling diode transmits load current during the switch off period, the average diode current is determined by the switch duty cycle. When the output voltage is high, the diode conducts for most of the time; When VOUT approaches VIN, the diode only conducts for a small portion of the time. The worst operating condition of a diode occurs when the output terminal of the voltage regulator is short circuited to ground.

In the event of a short circuit (VOUT=0V), the diode must safely withstand the short-circuit current ISC (PK) when the duty cycle approaches 100%.

The average current on the diode under normal load conditions is the set current of the asynchronous converter, which is:

$$I_{D(AVG)} = I_{OUT} = V_{FB}/R_{Sence}\ (A)$$

The freewheeling diode in this typical design is PMEG6020ER Schottky. Its rated value is 2A average forward current and 60V reverse voltage. The typical forward voltage at 2A is 460mV.

The only reason for selecting diodes with a rated current higher than that required for normal operation is the worst-case output short circuit. In this case, the diode current increases to the current limit value. Be sure to refer to the diode data sheet used to ensure that the diode can operate normally within the thermal and electrical limits. It is recommended to choose Schottky diodes greater than or equal to 2A.

The loss of a freewheeling diode is determined by its forward conduction voltage drop and switching time, so Schottky diodes are an excellent choice due to their reduced conduction voltage and fast switching time. The diode conducts output current during the period when the internal power switch is turned off. The turn off time of the internal switch is a function of the maximum input voltage, output voltage, and switching frequency. The output current during the turn off time is multiplied by the forward voltage of the diode, which is equal to the conduction loss of the diode. At higher switching frequencies, it is necessary to consider the AC losses of diodes. The AC losses of diodes are caused by the charging and discharging of junction capacitors and reverse recovery.

If the voltage regulator operates mostly in light load current or sleep mode, consider using diodes with low leakage current and slightly higher forward voltage drop.

Application Information: CIN Selection Suggestions and Experience Considerations

Consider the type of input capacitor CIN

Caution must be exercised when selecting the type of capacitor input for the converter:

Al electrolytic capacitor

The lowest cost, but unable to obtain sufficient ripple current rating.

Ceramic capacitors

Rarely has a large capacitance, but has high ripple current and voltage ratings, making it an ideal component for input bypass.

Solid state tantalum capacitors

It is also a good choice, but it is prone to damage and accompanied by severe phenomena when encountering large surge currents during the power on process. It will short-circuit and then ignite with dazzling white light and unpleasant odor. This phenomenon only occurs on components with low daylight hours, but some OEM companies prohibit them from operating in high waves due to this

Used in applications. Although several manufacturers have developed a series of solid-state capacitors that have undergone special surge withstand tests (such as the AVX TTPS series), even these components may be damaged when the input voltage surge approaches the maximum voltage rating of the capacitor. AVX recommends reducing the voltage rating of capacitors in large wave surge applications by 2:1.

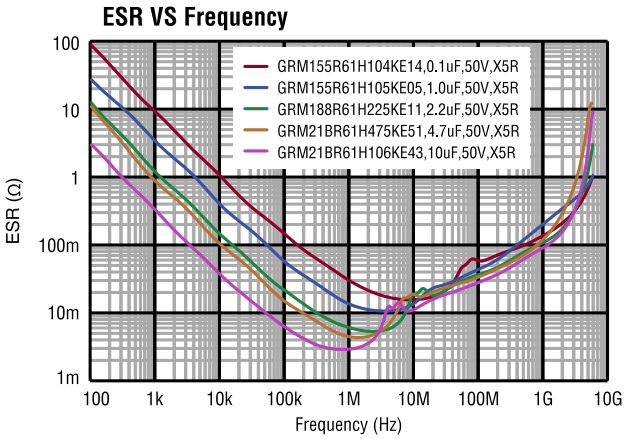
To achieve optimal performance, it is recommended to have at least one ceramic capacitor at the CIN location.

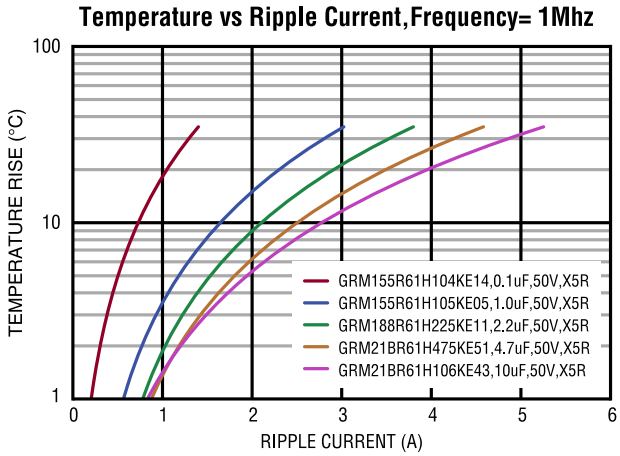
Calculation of current ripple of input bypass capacitor

The converter extracts the current from the input power supply in a pulsed manner. The average height of these pulses is equal to the load current. The rise and fall time of the current is very fast, so it is necessary to add a local bypass capacitor at both ends of the input power supply to ensure the normal operation of the voltage regulator and reduce the ripple current feedback to the input power supply. Capacitors also force the switching current to flow in a tight local loop. Minimize EMI to the greatest extent possible.

One stress that is often overlooked in power supplies is the RMS current of the input capacitor. If not understood correctly, exceeding the current will cause the capacitor to overheat and fail prematurely. Therefore, ceramic capacitors with low ESR have now become the preferred choice for bypass power levels.

The following chart is from muRata's X5R dielectric ceramic capacitor:





However, the ESR of electrolytic capacitors is often more than 10 times higher than that of ceramic capacitors: this means that it is impossible to obtain ripple current and electrolyte temperature rise that the device can operate stably. It is not feasible to use electrolytic capacitors alone.

Application Information: CIN Selection Suggestions and Experience Considerations

Using a 10uF ceramic capacitor alone is sufficient to bypass LMR64010 and handle ripple current.But the premise is that it is close enough to LMR64010 and placed directly on the traces leading from VIN (pin 5) and GND (pin 2) to achieve better performance with minimal increase in application footprint. Please refer to the layout example chapter for details.

It is recommended to use X7R or X5R capacitors to achieve optimal performance within the range of temperature and input voltage variations. The temperature and DC bias characteristics of Y5V and Z5U dielectrics are poor, and it is recommended not to use them

.

In addition, if ceramic capacitors are used alone in the power input stage, attention should be paid to their low ESR, which can easily form under damped slot circuits with long input cables or trajectories, while parallel electrolytic capacitors can suppress these high-Q circuits.

When paralleling electrolytic capacitors, you should pay attention to the ripple current in the electrolyte, as a large amount of power ripple current will eventually enter the electrolytic capacitor. When the ceramic capacitor in the combination capacitor is too small, a sufficiently high ripple voltage forms an overcurrent state in the parallel electrolytic capacitor, causing heating of the electrolytic capacitor. By plotting the Fourier series of the capacitor current, this curve can be used to calculate the electrolytic capacitor current for each harmonic (up to 10) and recombine the harmonics to calculate the total RMS current of the electrolytic capacitor. Please note that the current of ceramic capacitors is 1/4 cycle out of phase with the current of ESR, so they must be considered as vectors.

The input voltage ripple after selecting the capacitor can be estimated by the following methods:

$$\Delta V_{RIPPLE} = \frac{I_{LOAD}}{C_{IN} \times f_{SW}} \times \frac{V_{IN}}{V_{OUT}} \times \left(\frac{V_{OUT} - V_{IN}}{V_{OUT}}\right)$$

Consideration of CIN and high di/dv loop

To achieve maximum efficiency, the time for the switch to rise and fall has been made as short as possible. To prevent radiation and high-frequency resonance issues, it is necessary to arrange the layout of components connected to the switch nodes appropriately. Keep the pins of the freewheeling diode, switch, and input bypass capacitor as short as possible. B field (magnetic field) radiation can be reduced to the minimum amplitude. Minimize the length and area of all wires connected to the switch pin and BST pin as much as possible, which can also reduce electric field radiation. There must be a ground plane underneath the switch circuit to prevent coupling between layers. It is extremely important to keep the pin length on this path as short as possible to ensure clean switching operation and low amplitude EMI. This path includes a switching freewheeling diode and an input capacitor, and is the only path that contains nanosecond rise and fall times. If you search for this path on the PCB layout, you will find that it is already too short to be any shorter.

Application Information: Calculation and Selection Suggestions for Inductance

Selection of inductance value

Under the high-speed driving input voltage of the switch, an inductor is required to provide a constant current to the load.

Experience has shown that the optimal value for inductor ripple current is 40% of the maximum load current. Please note that when selecting ripple current for applications where the maximum load is much smaller than the maximum available load of the device, please use the maximum device current. The constant K is the percentage of inductor current ripple. For most applications, the inductor value can be calculated from the following equation:

$$L = \frac{V_{IN} \times (V_{OUT} - V_{IN})}{f_{SW} \times V_{OUT} \times K \times I_{LOAD(MAX)}}$$

As the ripple current increases with the input voltage, the maximum input voltage also determines the inductance value accordingly.

A larger inductance value can reduce ripple current. But it also requires a larger output capacitor to ensure the same output voltage ripple. However, inductors with larger values will have larger physical dimensions, higher DC resistance, and lower saturation current. The size of the inductor needs to be determined by balancing efficiency and transient response. Small inductors can cause significant ripple in inductor current, providing excellent transient response but reducing system efficiency.

For LMR64010,the optmal selection range for constant voltage output topology inductance in typical application circuits is 2.2 μ H to 10 μ H.

Continue to select inductors that meet the requirements for peak current (to avoid saturation), average current (to limit heating), and fault current. If the inductor overheats, the insulation layer in the winding will melt, causing a short circuit between the coils of the winding. The peak current of an inductor can be calculated according to the following formula:

$$I_{L(PEAK)} = I_{LOAD(MAX)} + \frac{V_{IN} \times \left(V_{OUT(MAX)} - V_{IN}\right)}{2 \times V_{OUT(MAX)} \times f_{SW} \times L}$$

In an ideal situation, the saturation current rating of an inductor should be at least as large as the high voltage side switch current limit. This ensures that the inductor does not saturate. When the inductor core material saturates, the inductor drops to a very low value, causing the inductor current to rapidly increase. Although the current limit ILIMIT SW (PEAK) is designed to reduce the risk of current runaway, but saturated inductors can quickly increase the current to a high value. This may result in component damage. So it is absolutely not allowed for inductors to saturate!

The DC resistance of an inductor is a key parameter that affects efficiency. In terms of efficiency, it is recommended that the DCR of the inductor be less than 200m Ω.

Consideration of magnetic core material

Once the value of L is known, the type of inductor must be selected. The demand for high efficiency often cannot afford the iron core losses in low-cost powder iron cores, forcing the use of more expensive ferrite iron cores. For a fixed inductance value, the actual iron core loss is independent of the iron core size, but is closely related to the selected inductance. As the inductance increases, the iron core loss decreases. Unfortunately, the increased inductance requires more wire turns, so copper losses will increase.

Ferrite materials have extremely low iron core losses and are more susceptible to corrosion at high switching frequencies, so the design goal can focus on copper losses and preventing saturation. The saturation of iron powder magnetic cores exhibits a certain degree of flexibility and is more abundant, but ferrite magnetic cores will rapidly saturate. Other magnetic core materials fall between the two. The ferrite core material is saturated and "hard", which means that when the peak design current is exceeded, the inductance will suddenly collapse. Do not let the inductance saturate!

Different magnetic core materials and shapes can alter the size/current and price/current relationships of inductors. The annular or shielded bowl shaped magnetic core in ferrite or Permalloy materials has a small volume and does not radiate energy, but is usually more expensive than powder iron core inductors with similar characteristics. The type of inductor used mainly depends on price and size requirements, as well as any radiation field EMI requirements.

EMI requirements

Determine whether the design can accept an "open" inductor: they have high magnetic field radiation. Or whether a closed inductor is needed to prevent EMI issues. For example, open inductors cannot be used

next to magnetic storage media! This is a difficult decision because open inductors are both cheap and compact.

Summarize

When choosing an inductor, you may need to consider the maximum load current, core and copper losses, allowable component height, output voltage ripple EMI、

The fault current and saturation in the inductor, as well as the cost.

Remember: all good things, such as high efficiency, low ripple, and high operating temperatures, come at a cost, sometimes even very high.

Application Information: Considerations and Experience in Selecting Output Capacitors

Output capacitance, output ripple, and transient response

The choice of COUP is mainly driven by three main factors. Requirements for external poles, output voltage ripple, and load transient changes generated by output capacitors. The output capacitor needs to be selected based on the strictest of these three standards.
The first criterion is the expected response to changes in load current:
Voltage regulators typically require three or more clock cycles in order for the control circuit to see changes in load current and output voltage, and adjust the duty cycle to respond to the changes. The output capacitor must be large enough to provide a current difference of two clock cycles while meeting the tolerance for output voltage drop. The following formula can be used to estimate the lower limit of the total output capacitance that meets the specified load transient requirements:

$$C_{OUT} \geq \Delta I_{OUT\_STEP} \times \left(\frac{3}{f_{SW} \times \Delta V_{DROP}}\right)$$

其中：

ΔI_{OUT_STEP} The step value of the load (ampere).
f_{SW} Switching frequency (Hz).
ΔV_{DROP} Maximum allowable output voltage drop/overshoot (volts) for load step.

Note that the calculation of the above formula is an approximate value and is based on the following assumptions:

The inductance value is determined by the peak to peak current value, which is 30% of the maximum load current.

The voltage drop across the internal MOSFET switch and the DC resistance of the inductor can be ignored。

The premise for the formula to hold is that the loop requires three switching cycles before adjusting the inductor current according to the load step.

The second standard is the expected requirement for ripple current, and the size of the output voltage ripple depends on the specific application. The following formula can be used to estimate the lower limit of total output capacitance and the upper limit of capacitance ESR:

$$C_{OUT} \geq \frac{I_{L(Ripple)}}{8 f_{SW} \times V_{OUT(Ripple)}} \cong \frac{V_{IN}}{(2\pi \times f_{SW})^2 \times L \times V_{OUT(Ripple)}}$$

Among them:
$I_{L(Ripple)}$ Ripple current of inductor (ampere).
f_{SW} Switching frequency (Hz).
$V_{OUT(Ripple)}$ To achieve the desired output ripple voltage (in volts).

Then, using the following formula, calculate the maximum ESR of the output capacitor that must meet the output voltage ripple specification.

$$ESR_{COUT} \leq \frac{V_{OUT(Ripple)}}{I_{L(Riplle)}}$$

The size of the output capacitor and its ESR value determine the output voltage ripple and load transient performance.
In practical applications, the output capacitance has the greatest impact on transient response and loop phase margin. Load transient testing and Bode plots are the best methods for validating any given design, and must be carefully validated for their own application scenarios before the application is put into production.

Application Information: Considerations and Experience in Selecting Output Capacitors

Effective capacity and medium

A higher output capacitance value reduces output voltage ripple and improves load transient response. When selecting the type of ceramic capacitor for this value, it is also important to consider the capacitance loss caused by the DC bias of the output voltage.
Ceramic capacitors are made of various dielectrics, and their characteristics vary depending on the temperature and applied voltage. Capacitors must have a dielectric that is sufficient to ensure minimum capacitance within the necessary temperature range and DC bias conditions. The most commonly used dielectrics are Z5U, Y5V, X5R, and X7R. Z5U and Y5V dielectrics are suitable for providing high capacitance in small packages, but exhibit strong voltage and temperature coefficients, as shown in Figures 17. a and 17. b. When used with a 5V regulator, a 10 μ F Y5V capacitor can only exhibit effective values as low as 1 μ F to 2 μ F within the operating temperature range. X5R and X7R dielectrics have more stable characteristics and are more suitable for use as output capacitors. The X7R model has better cross temperature stability, while the XSR has a lower price and higher available capacitance value.
It is recommended to use X5R or X7R dielectric with a rated voltage of 6.3V or 10V,
To achieve optimal performance. It is recommended not to use Y5V and Z5U dielectrics with any DC-DC converter, as these dielectrics have poor temperature and DC bias performance.
Figure16.a Ceramic Capacitor DC Bias Characteris
When considering the variation of capacitance with temperature, component tolerance, and voltage, the worst-case condition capacitance can be calculated using the following formula: $C_{EFF} = C_{OUT} \times (1 - TEMOPCO) \times (1 - TOL)$

Among them:
C_{EFF} The effective capacitance under working voltage.
$TEMOPCO$ The worst capacitance temperature coefficient.
TOL For the worst component tolerance.

To ensure the performance of the booster, it is necessary to evaluate the impact of DC bias, temperature, and tolerance on capacitor performance for each application.
Therefore, when selecting ceramic capacitors for the output filter of the converter, it is necessary to choose capacitors with nominal capacities that are 20% to 30% higher than the calculated results. In addition, the rated voltage of the capacitor must be higher than the output voltage of the converter.

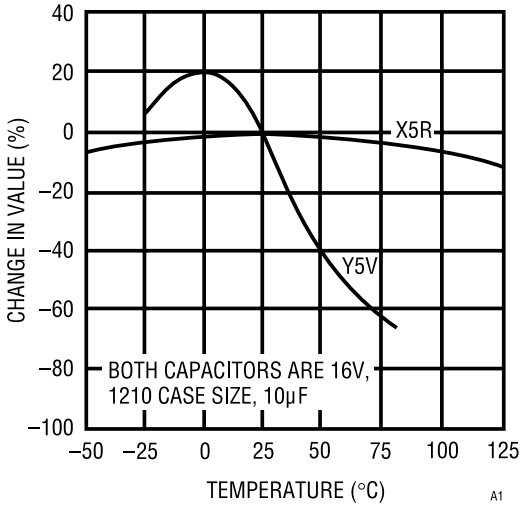


Figure16. b. Ceramic Capacitor DC Bias Characteris.

Application information: Dissipation power and high temperature considerations of voltage regulators

High temperature considerations: composition and calculation of dissipated power

When the ambient temperature and chip temperature rise reach the over temperature protection threshold TOTP-R, OTP protection may be triggered. To estimate the core temperature of LMR64010, it is necessary to first understand the composition of the heat source and under what operating conditions it becomes dominant, and adopt reasonable optimization methods.

The efficiency and loss composition of the voltage regulator conversion circuit:

Total conversion efficiency of voltage regulator:

$$\eta = \frac{P_{OUT}}{P_{IN}} \times 100\%$$

Among them:

P_{IN} The total input power of the voltage regulator.

P_{OUT} The total output power of the voltage regulator.

The total power loss is calculated as follows:

$$P_{LOSS} = P_{IN} - P_{OUT}$$

This total loss is mainly composed of several parts, approximately:

$$P_{LOSS} = P_{LOSS(DBUCK)} - P_L - P_{Catch}$$

Among them:

$P_{LOSS(DBUCK)}$ *The power consumption generated within the device.*

P_L *For inductor power consumption.*

P_{Catch} *The power consumption on the external freewheeling diode.*

Power consumption can be calculated through various methods. The simplest rough estimate can be obtained by comparing the efficiency curve of the regulator in the "Chart" section with one's own working scenario to obtain the total power loss. Then subtract the loss of external components to obtain the device loss.

If the magnetic core loss is ignored, the inductance loss can be estimated by the following equation:

$$P_L \cong I_{OUT}^2 \times DCR_L$$

Among them:

I_{OUT} *For DC load current.*

DCR_L *Connect an inductor in series with a resistor.*

Modeling the internal loss composition of the device:

The second method for estimating device power consumption is to conduct analysis, which requires modeling the internal power consumption of the device using the following formula.

The internal power consumption P_ (LOSS (DBUCK)) of the device includes power switch conduction loss, switch loss, and conversion loss. There are other sources of losses, but in high output load current applications involving heat dissipation limitations, these losses are generally not significant.

$$P_{LOSS(DBUCK)} = P_{COND} + P_{SW} + P_{TRAN}$$

The conduction loss of power switch is caused by the output current IOUT flowing through the NMOSFET power switch with internal resistance RDS (ON). The calculation formula for conductive power loss is as follows:

$$P_{COND} = (R_{DSON-N} \times V_{OUT} \times I_{OUT}^2)/V_{IN}$$

The switching loss is related to the traction current generated by the driver, which opens and closes the power supply device at the switching frequency. The calculation formula for switch loss is as follows:

$$P_{SW} = \left(C_{GATE-N} + C_{J\_Catch}\right) \times V_{IN}^2 \times f_{SW}$$

Among them:

C_{GATE-N} *The gate capacitance of NMOSFET. This device is approximately 75pF.*

C_{J_Catch} *The junction capacitance of the external freewheeling diode.*

The conversion loss is caused by the inability to immediately turn on or off the N-channel power MOSFE. The calculation formula for conversion loss is as follows:

$$P_{TRAN} = V_{IN} \times I_{OUT} \times (t_{RISE} + t_{FALL}) \times f_{SW}$$

Among them:

t_{RISE} *The rise time of the switch node SW*

t_{FALL} *The descent time of the switch node SW*

When using the above formulas and parameters to estimate converter efficiency, it must be noted that these formulas do not cover all converter losses, and the parameter values given are typical. The performance of the converter also depends on the selection of passive components and the layout of the circuit board, so sufficient safety margin should be considered when estimating.

The power consumption caused by ground current is quite small and can be ignored.

Application information: Dissipation power and high temperature considerations of voltage regulators

In summary, we can draw the following conclusions and optimization measures:

- When the pressure difference between input and output is large, efficiency will decrease. This is because the freewheeling diode CJ will cause both Psw and P_{TRAN} to increase simultaneously, resulting in chip heating. Usually, diodes with smaller CJ have higher forward conduction voltage drop: this means that the internal power loss of the device is reduced, but the conduction loss of the external diode is increased. So, when the input voltage is high and the output current is low in an application, choosing a diode with a smaller C_J_catch and combining it with the next suggestion will be a good strategy to reduce the internal heat of the regulator.
- It is worth noting that the heat generated by the power consumption of inductors and freewheeling diodes can also be appropriately addressed using the "heat island" method to prevent this heat from being conducted into the chip through PCBs or trace lines.
- In addition, it is worth noting. Due to the positive temperature coefficient of RDS (ON) on the MOSFET of the voltage regulator (see "Boost Switching Voltage Regulator: Chart" for details), when the TJ temperature increases, the conductive power loss of the voltage regulator will further increase. Therefore, the core temperature TJ should be minimized as much as possible to achieve better efficiency characteristics.

Consideration for heat dissipation

At high ambient temperatures, the device's ability to control the power supply is limited by the maximum rated junction temperature (125 ° C). Therefore, all thermal resistances from the chip junction temperature to the casing should be carefully considered, as well as other heat sources fixed around it.

For surface mount devices, the thermal conductivity of PCBs and their copper printed wires can be utilized for heat dissipation. Thickened copper plates and through-hole pads can also be used to dissipate the heat generated by power devices.

The following table lists the thermal resistance of PCBs with different board areas and copper foil areas. All tests were conducted under windless conditions and on FR-4 boards made of 1 ounce copper foil.

Table 18. Measurement values of thermal resistance

Copper foil area（mm^2）		PCB area (mm^2)	thermal resistance θ_{JA} (℃/W)
top	bottom		
2500	2500	2500	125
1000	2500	2500	125
225	2500	2500	130
100	2500	2500	135
50	2500	2500	130

（1）The device is installed on the top floor.

If the temperature TA of the circuit board is known, the thermal resistance parameter JA can be used to estimate the magnitude of the junction temperature rise. TJ is calculated by TA and PD, and the formula is as follows:

$$T_J = T_A + (P_D \times \theta_{JA})$$

A very important consideration is that JA is based on a 4-layer 4 in x 3 in, 2.5 oz copper circuit board (compliant with JEDEC standards), and the size and number of layers used in actual applications may vary. Copper must be used as much as possible to facilitate device heat dissipation.

The heat dissipation effect of copper exposed to the air is better than that of copper used in the inner layer. If the shell temperature can be measured, the junction temperature can be calculated using the following formula:

$$T_J = T_C + (P_D \times \psi\ )$$

Among them, TC is the shell temperature, and PSI JB is the thermal resistance shown in Table 4.

设When designing applications in special environmental temperature ranges, the expected device power consumption P_{LOSS} (D_{BOOST}) caused by losses should be calculated using a formula, and then the junction temperature TJ can be estimated using the above formula based on this power calculation.

Only when the estimated chip junction temperature based on the formula is below 125 ℃, can the reliable operation of the charger be guaranteed. The increase in junction temperature will seriously affect reliability and mean time between failures (MTBF).

Application information: Other considerations and design experience suggestions

Hot dip safety

Ceramic capacitors have the advantages of small size, good stability, and low impedance, making them an ideal choice for input bypass capacitors in the LMR64010 circuit. However, if LMR64010 is plugged into a live power source, these capacitors may cause issues.Ceramic capacitors with low ESR characteristics and stray inductance in series with the power supply form an "underdamped slot circuit", and the voltage at the VIN pin of LMR64010 may exceed the nominal input voltage, which may exceed the rated value of LMR64010 and damage the parts. If the input power control is improper or the user needs to plug the LMR64010 into a power source, the design of the input network should prevent this overshoot.

Figure 20 shows the waveform generated when the LMR64010 circuit is connected to a 24V power supply through a 6-foot (2m) 24AW twisted pair cable. The first figure shows the instantaneous response of a ceramic capacitor with a 2.2 μ input terminal. The input voltage is as high as 35V, and the peak input current is 20A.

One way to improve and prevent the impact of this issue is to add another capacitor with a series resistor in the circuit. An aluminum electrolytic capacitor has been added in Figure 20b. The damping generated by the high equivalent series resistance of this capacitor can eliminate voltage overshoot. The additional capacitance improves the input ripple and can slightly increase the efficiency of the circuit, although it may be the largest component in the circuit.

Another solution is shown in Figure 20C. A 1 Ω resistor is connected in series with the input to eliminate voltage overshoot (which also reduces peak input current). A 0.1 μ F capacitor improves high-frequency filtering. This solution is smaller and cheaper than electrolytic capacitors. For high input voltage, its impact on efficiency is minimal.

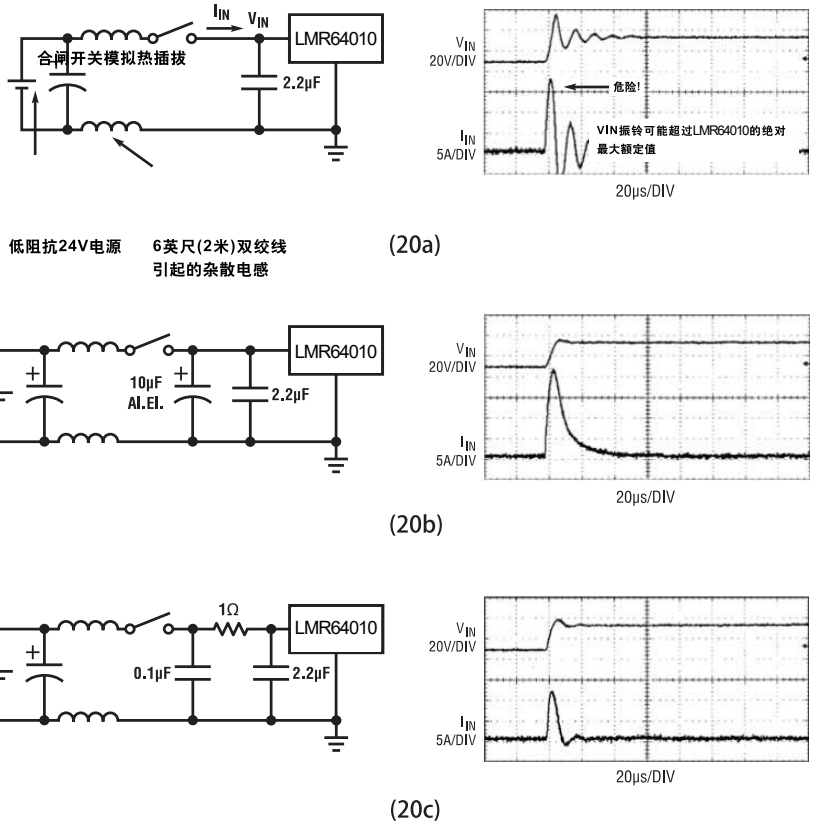


Figure 19. Carefully selected input network prevents input voltage overshoot and ensures reliable operation of LMR64010 when connected to a live power source

Application Information: Reference Layout Example

Summary

The high integration of LM64010 makes PCB board layout very simple and easy.Poor layout can affect the performance of LMR64010.causing electromagnetic interference(EMI),poor electromagnetic compatibility(EMC) ground jumping, and voltage loss, which in turn affects voltage regulation and stability. In order to optimize its electrical and thermal performance, the following rules should be applied to achieve good PCB layout and wiring, ensuring optimal performance:

- The high-frequency ceramic input capacitor CIN must be placed as close as possible to the VIN and GND pins to minimize high-frequency noise.
- For high current paths, a larger PCB copper-clad area should be used, including the GND pin. This helps to minimize PCB conduction losses and thermal stress to the greatest extent possible.
- It is necessary to reduce the PCB copper plating area related to SW pins to avoid potential noise interference issues.
- To minimize via conduction loss and reduce module thermal stress, multiple vias should be used to achieve interconnection between the top layer and other power layers or strata.
- The impedance of the FB pin is relatively high, and the lead trajectory should be as short as possible and kept away from high noise SW nodes or shielded.
- The bottom heat dissipation pads of ESOP8 packaged chips with through-hole openings help improve the efficiency of chip heat dissipation.

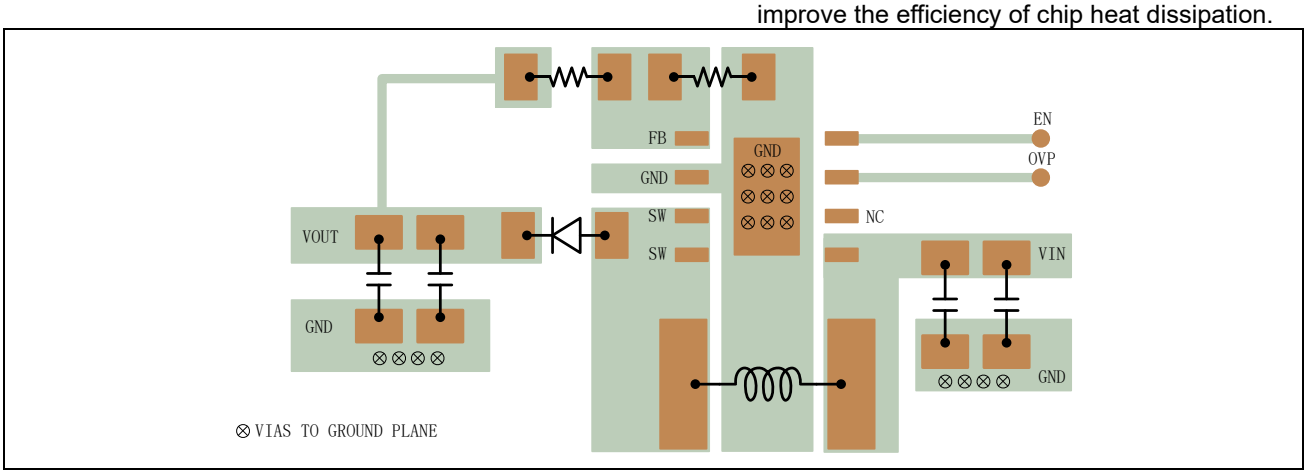


Figure 20.1 Recommended Circuit ESOP8 Package PCB Layout Example

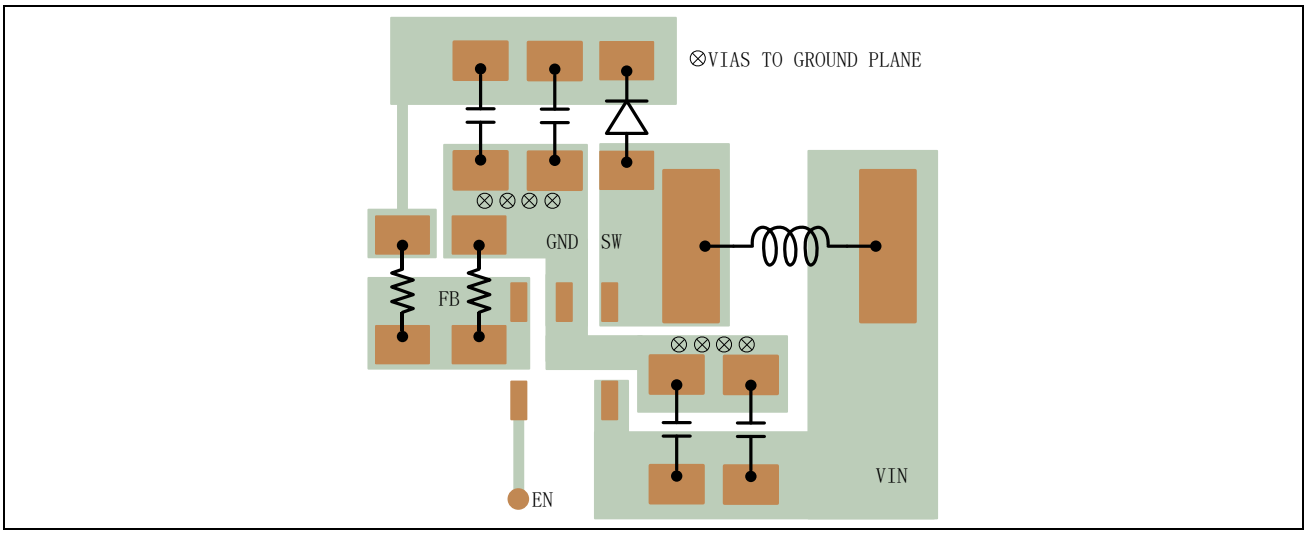
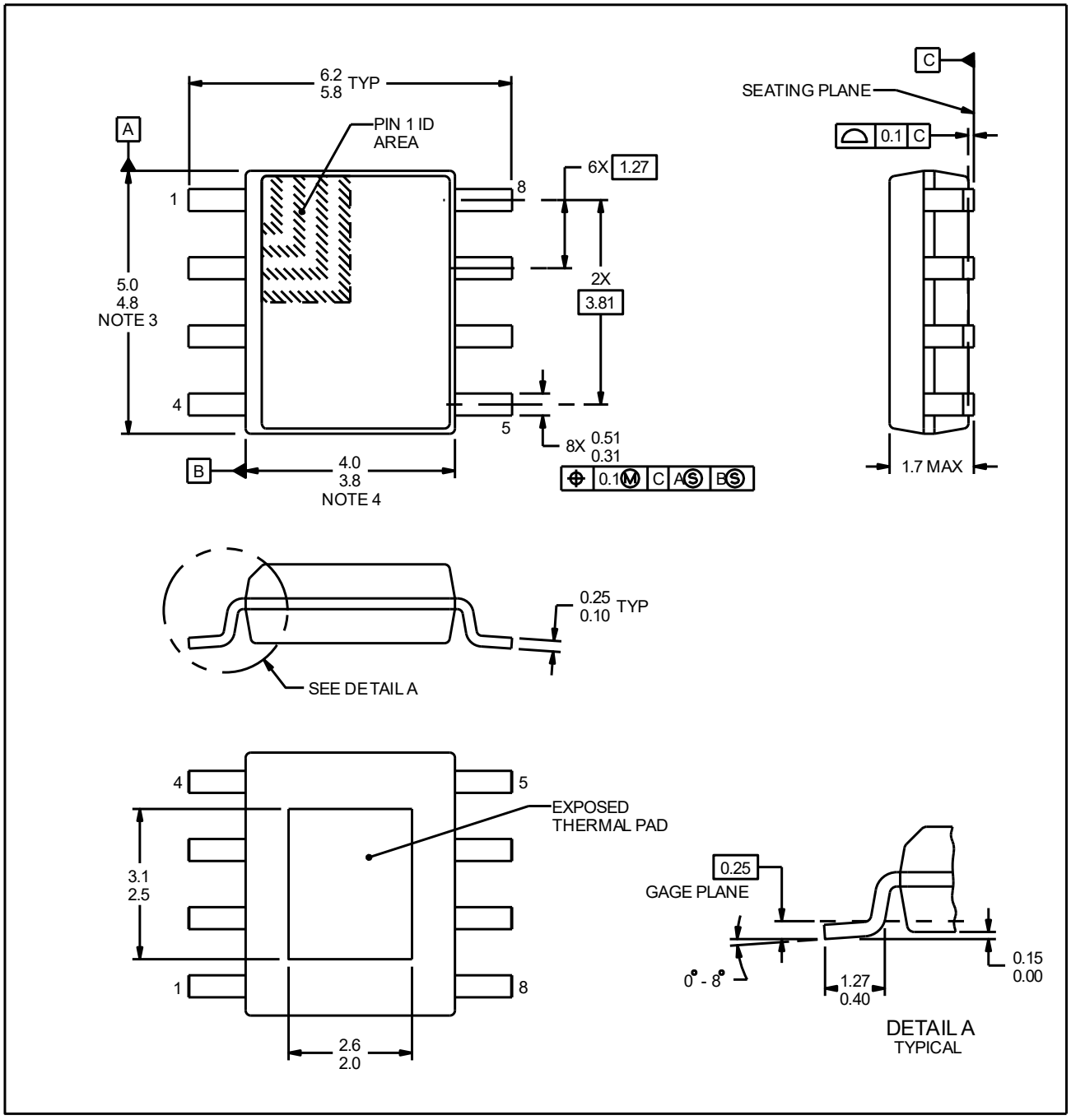


Figure 20.2 Recommended SOT23-5 Package PCB Layout Example for Circuit

Package Description (ESOP8)

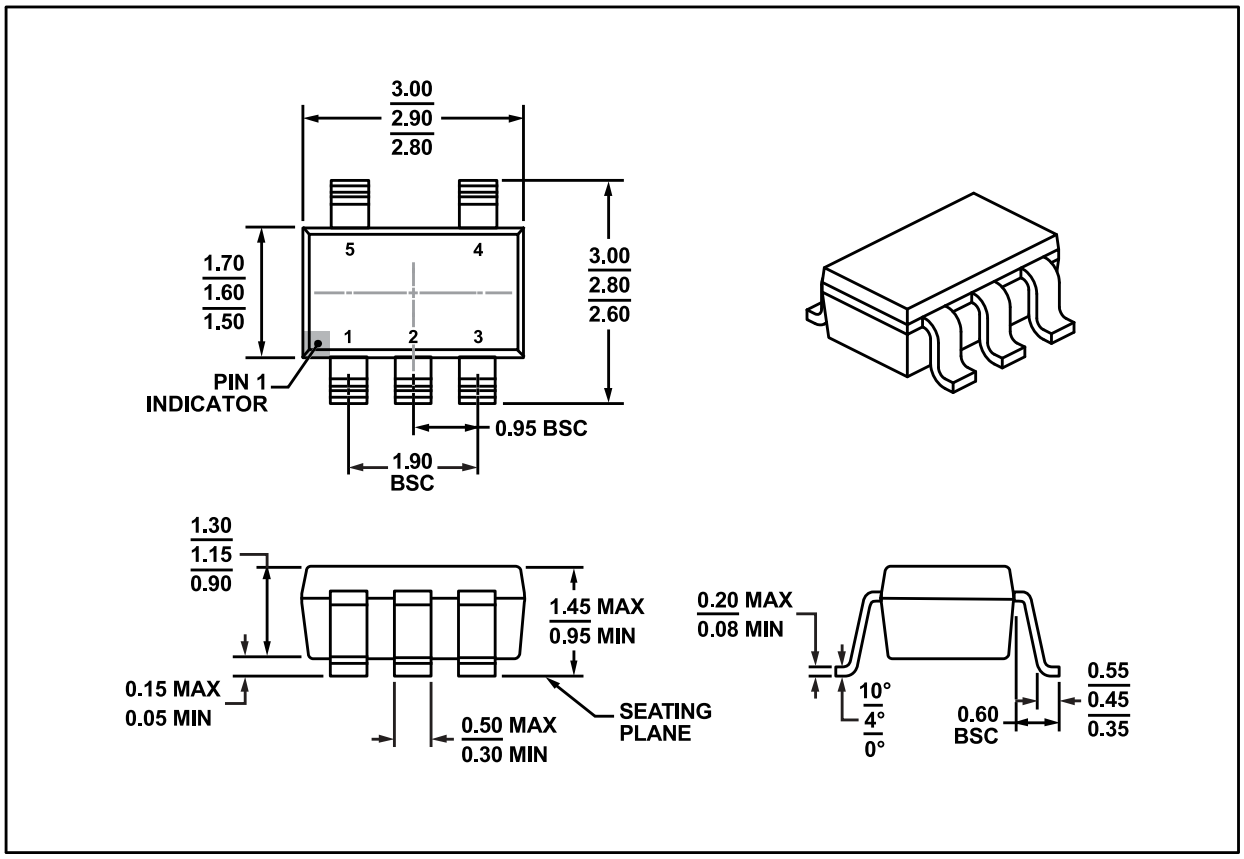
8-pin plastic encapsulated SOIC with bottom EPAD



注:

(1) All data units are in millimeters, and any dimensions in parentheses are for reference only.
(2) This image is subject to change without prior notice.
(3) This size does not include mold burrs, protrusions, or nozzle burrs.
(4) This size does not include mold burrs.

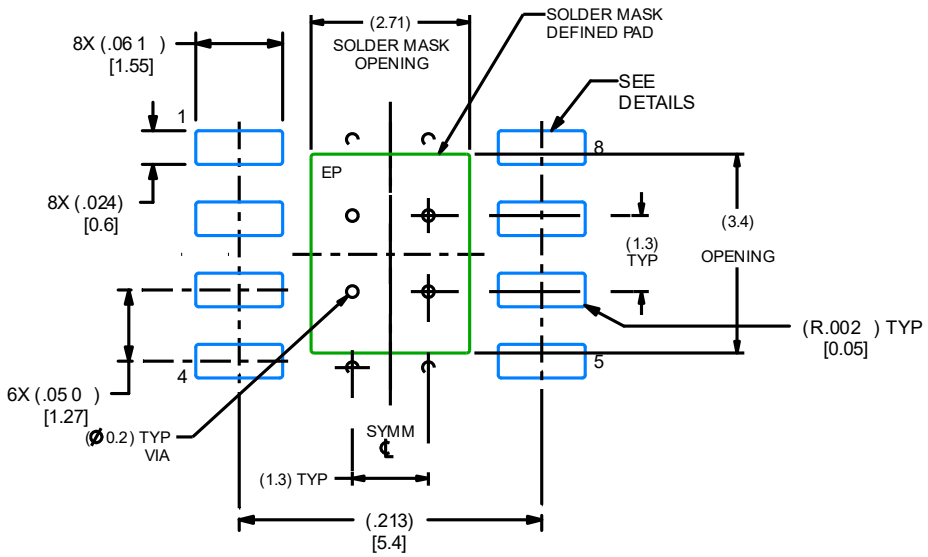
Package appearance description
1.45mm height 5-pin SOT-23 plastic encapsulated SOIC



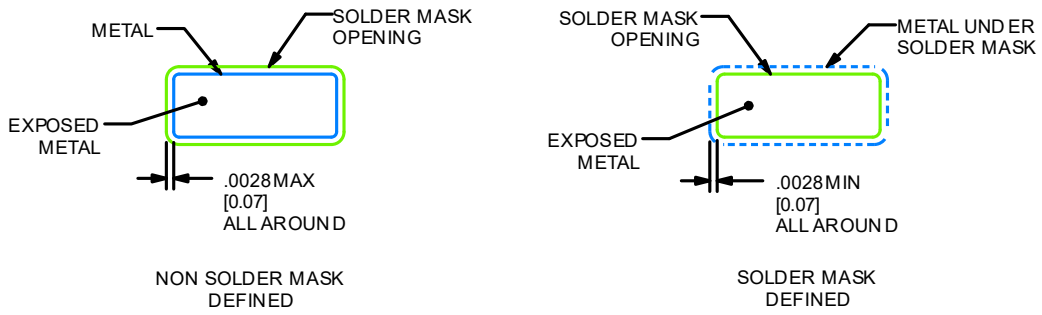
Note:

(1) All data units are in millimeters, and any dimensions in parentheses are for reference only.
(2) This image is subject to change without prior notice.
(3) This size does not include mold burrs, protrusions, or nozzle burrs.
(4) This size does not include mold burrs.

Example of Device Packaging Pad Layout (ESOP8)
8-pin plastic encapsulated SOIC with bottom EPAD



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:8X



SOLDER MASK DETAILS

Note:

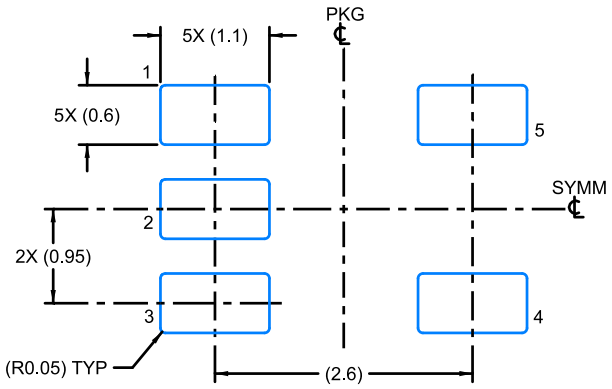
(1) Based on IPC-7351, which relies on proven mathematical algorithms and comprehensively considers manufacturing, assembly, and component tolerances, the solder pad pattern is accurately calculated.(2) The tolerance of the solder mask between and around signal pads may vary depending on the manufacturing of the circuit board.

(2) The size of the metal pad may vary due to creepage requirements.

(3) Through holes are optional, depending on the application, please refer to the device data sheet. If via holes are used, please refer to the via hole positions shown in this view. Suggest filling or covering the via under the solder pad with solder paste.

Example of Device Packaging Pad Layout

1.45mm height 5-pin SOT-23 plastic encapsulated SOIC



器件封装焊盘布局举例
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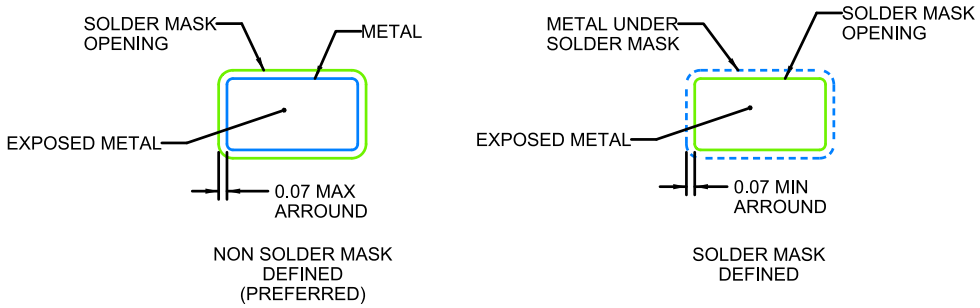


焊盘阻焊部详解
PADS 1-6

Note：

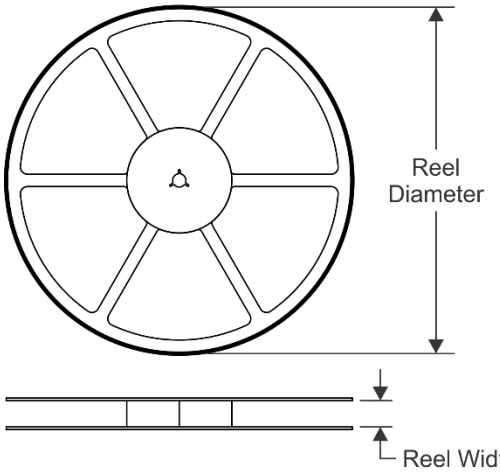
(1) Based on IPC-7351, which relies on proven mathematical algorithms and comprehensively considers manufacturing, assembly, and component tolerances, the solder pad pattern is accurately calculated.

(2) The tolerance of the solder mask between and around signal pads may vary depending on the manufacturing of the circuit board.

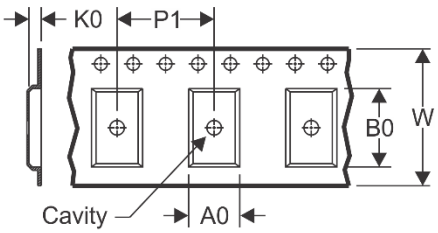
(3) The size of the metal pad may vary due to creepage requirements.

TAPE AND REEL INFORMALEGEND-SION

REEL DIMENSIONS

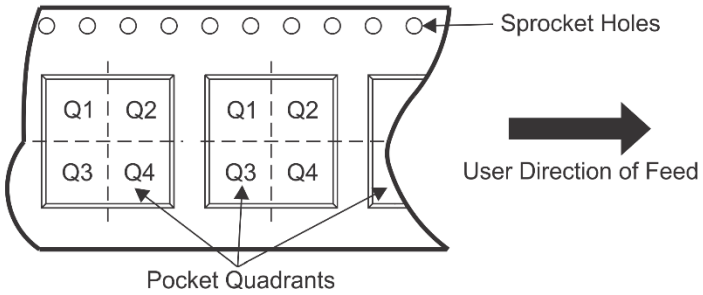


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*ALL dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Width W1(mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
LMR64010XMFX	SOT23-5	B5	5	3000	180.0	8.4	3.2	3.2	1.4	1.4	Q3
LMR64010XMF	ESOP8	EP	8	4000	330	6.5	5.3	2.1	8	12	Q1