NSA2300

General Sensor Conditioner with Digital Temperature Calibration

Datasheet (EN) 2.3

Product Overview

The NSA2300 is a highly integrated, low power high precision sensor conditioner for general resistive bridge sensors, which features a low noise instrument amplifier, a low power 24-bit Σ-Δ ADC, a digital sensor calibration DSP and a 12-bit DAC. The NSA2300 can provide an on-chip digital compensation of sensor offset, gain, temperature drift and non-linearity based on the internal fuse banks (OTP). Multiple temperature sensing methods are supported by NSA2300 for sensor's temperature calibrating. Once calibrated, the pin VOUT can provide a selectable absolute or ratio-metric analog output, and I²C, SPI and one wire (OWI) interfaces are supported for chip configuration, sensor calibrating and digital output.

Applications

- Pressure sensor conditioner
- Magnetic sensor conditioner
- Strain gauge interface
- Industrial process control

Key Features

- Ultra-low power-down current (< 0.2μA @ 25℃)
- Low input referred RMS noise (600nV @ OSR=1024X, GAIN=32X
- Full set of diagnostic features
- Low power PGA and 24-bit Σ-Δ ADC
- 1X~128X programmable gain for sensors
- Multiple temperature sensing methods
- 8-level resolution settings for conversion time and accuracy trade off
- Built in sensor calibration logic
- OTP based digital calibration of sensor offset, sensitivity, temperature drift and non-linearity
- Ratio-metric or absolute voltage output
- I²C, SPI, OWI output
- Supply voltage 1.8V ~ 5.5V
- Operation temperature: -40℃~125℃
- RoHS & REACH compliance

Device Information

Part Number	*Package*	*Body Size*
NSA2300_QBW	Bare die	1.23mm × 1.19mm
NSA2300-QMOR	MSOP10	3mm × 3mm
NSA2300-QSOR	SOP8	4.9mm × 3.9mm

Functional Block Diagrams

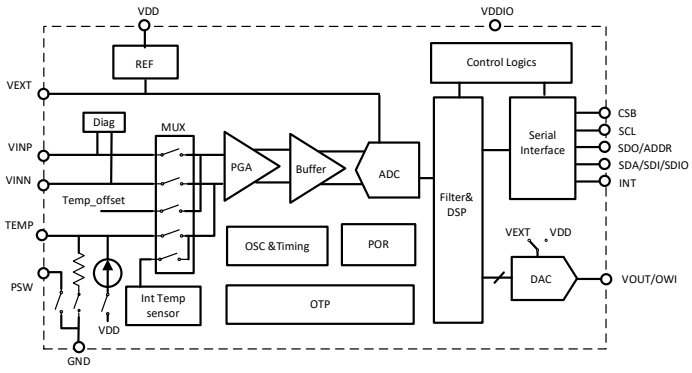

Figure 1. NSA2300 Block Diagram

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1. Pin Configuration and Wafer Information

The NSA2300 is offered either via bare die or SOP-8 Package or MSOP10 Package. The Pin of MSOP10 and SOP8 are shown in Figure1.1 and description of MSOP10 and SOP8 are shown in table1.1.

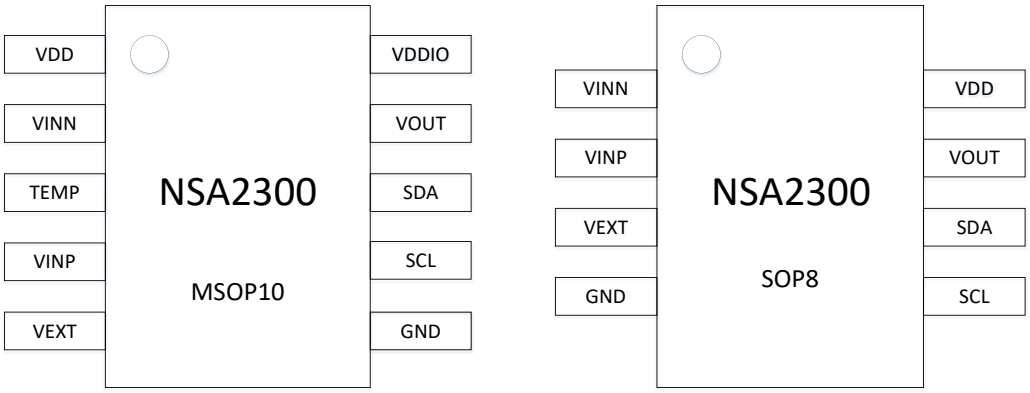


Figure 1.1 NSA2300 Package

Table 1.1 NSA2300 Pin Configuration and Description

Bare Die Pin No.	*MSOP10 Pin No.*	*SOP8 Pin No.*	*Symbol*	*Type*	*Function*
1	1	8	VDD	Power supply	Power Supply for core circuits
2	-	-	PSW	Analog output	Low-side power switch connection for pressure sensor
3	2	1	VINN	Analog input	Analog input positive
4	3	-	TEMP	Analog output	External temperature sensor input
5	4	2	VINP	Analog input	Analog input positive
6	5	3	VEXT	Analog output	Excitation voltage for external sensor
7	6	4	GND	Ground supply	Ground
8	-	-	SDO/ADDR	Digital output	Serial data output in 4-wire SPI mode Address selection in I^2C mode
9	7	5	SCL	Digital input	Serial clock
10	8	6	SDA/SDI/SDIO	Digital input	Serial data input/output in I^2C mode (SDA) Serial data input in 4-wire SPI mode (SDI) Serial data input/output in 3-wire SPI mode (SDIO)
11	-	-	TP1	Analog output	Test pad, internal use
12	9	7	VOUT	Analog Output	DAC output / One Wire Interface
13	-	-	TP2	Analog Output	Test pad, internal use
14	-	-	CSB	Digital input	Chip select
15	-	-	INT	Digital output	Data ready interrupt output
16	10	8	VDDIO	Power supply	Power supply for I/O circuits

Note 1: For NSA2300 SOP8 package, VDD and VDDIO pads both are connected to pin 8.

The pad location of bare dies is shown in Fig1.2, The description of bare dies is shown in Table1.2

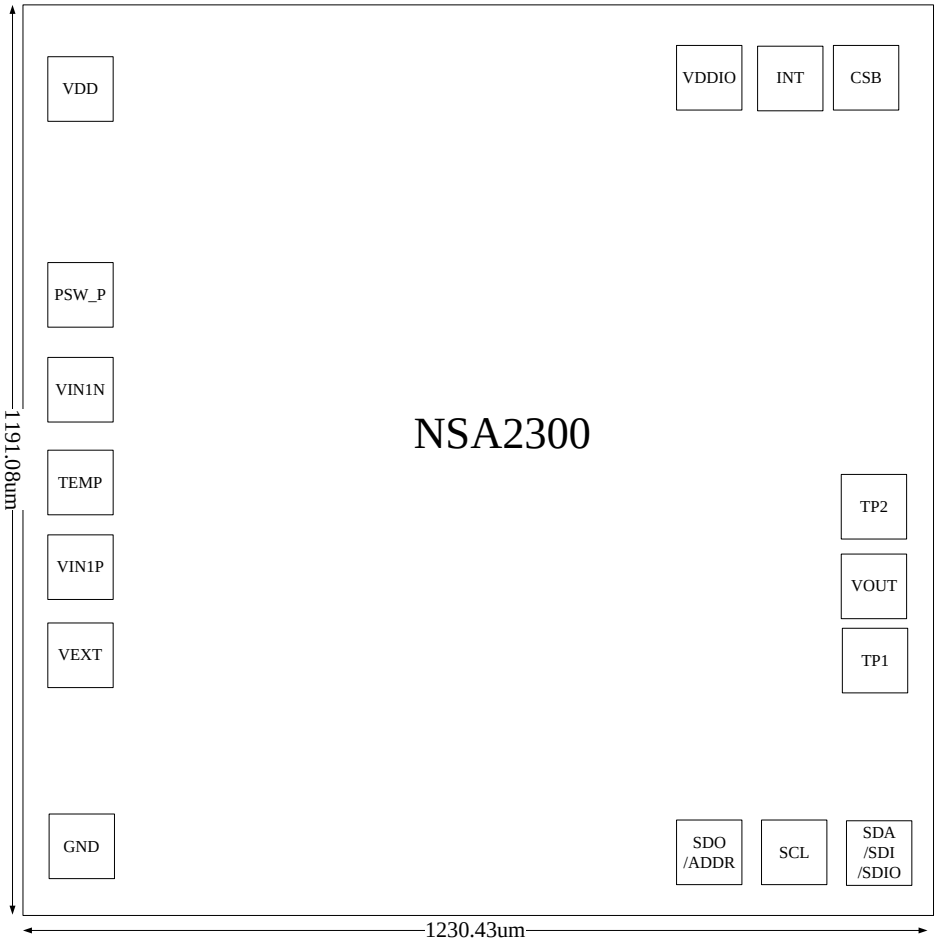


Figure 1.2 NSA2300 PIN Assignment

Table 1.2 NSA2200 PAD Description

Bare Die Pin No.	***Symbol***	***Type***	***Function***
1	VDD	Power supply	Power Supply for core circuits
2	PSW	Analog output	Low-side power switch connection for pressure sensor
3	VINN	Analog input	Analog input positive
4	TEMP	Analog output	External temperature sensor input
5	VINP	Analog input	Analog input positive
6	VEXT	Analog output	Excitation voltage for external sensor
7	GND	Ground supply	Ground
8	SDO/ADDR	Digital output	Serial data output in 4-wire SPI mode Address selection in I^2C mode

9	SCL	Digital input	Serial clock
10	SDA/SDI/SDIO	Digital input	Serial data input/output in I²C mode (SDA) Serial data input in 4-wire SPI mode (SDI) Serial data input/output in 3-wire SPI mode (SDIO)
11	TP1	Analog output	Test pad, internal use
12	VOUT	Analog Output	DAC output / One Wire Interface
13	TP2	Analog Output	Test pad, internal use
14	CSB	Digital input	Chip select
15	INT	Digital output	Data ready interrupt output
16	VDDIO	Power supply	Power supply for I/O circuits

2. Absolute Maximum Ratings

Parameters	*Symbol*	*Min*	*Typ*	*Max*	*Unit*	*Comments*
Power Supply Voltage	VDD	-0.3		6.5	V	
	VDDIO	-0.3		6.5	V	
Analog Pin Voltage		-0.3		VDD+0.3	V	
Analog Pin Current				40	mA	
Digital Pin Voltage		-0.3		VDDIO+0.3	V	25℃
Maximum Junction Temperature	T_j			155	℃	
Operating Temperature	T_{opr}	-40		125	℃	
Storage Temperature	T_{stg}	-60		150	℃	

3. ESD Ratings

	Ratings	*Value*	*Unit*
Electrostatic Discharge	Human body model (HBM), per ESDA/JEDEC JS-001-2017 All pins	±2.0	kV
	Charged device model (CDM), per ESDA/JEDEC JS-002-2018 All pins	±500	V

4. Electrical Characteristics

Parameters	*Symbol*	*Min*	*Typ*	*Max*	*Unit*	*Comments*
Power Supply and Regulation						
Power Supply Voltage	VDD	1.8		5.5	V	
	VDDIO	1.2		5.5	V	
Operating Current (Sensor not included)	I_{DD_PGAoff}		0.9		mA	PGA off (Gain <= 2), DAC off
	I_{DD_PGAon}		1.5		mA	PGA on (Gain >= 4), DAC off
	I_{DD_DAC}		1.7		mA	PGA on, DAC on
Standby Current	I_{stb}		100		nA	25℃
Regulator Output		1.62	1.8	1.98	V	'Regulator_sel' = 0
		3.24	3.6	3.96	V	'Regulator_sel' = 1
Regulator PSRR			60		dB	
Current Load on Regulator				5	mA	
Signal Chain (MUX+PGA+BUFFER+ADC)						
ADC Resolution			24		Bits	
Conversion Time	T_{cnv}	Refer to Table 6.1			ms	
Primary Data Resolution			24		Bits	LSB = (1/2^23)*(VEXT-PSW) ('Raw_data_on' = 1)
Effective Resolution	ENOB	Refer to Table 6.1			Bits	
Gain Setting	GAIN	1		128		
Integral Nonlinearity	INL			15	ppm/FS	
Input Common Mode Rejection	CMRR	80	110		dB	
Power Supply Rejection	PSRR	90	110		dB	
Temperature Sensor						
Temperature Data Resolution			16		Bits	
Internal Temperature Sensor Accuracy				±0.5	℃	'Temp_sel' = 2'b11, 25 ℃
				±1	℃	'Temp_sel' = 2'b11, -40 to 85 ℃
External Temperature Sensor Sensing	R_{REF}	4.5	5	5.5	kohm	'Temp_sel' = 2'b00
	I_{EXC}		20		μA	'Temp_sel' = 2'b01
External Temperature Sensor Offset Voltage		0		1	VEXT	Configured by T_offset_trim, 'Temp_sel' = 2'b00/2'b01/2'b10
Analog Input Pins						

Input Voltage of VINP, VINN		GND+0.1		VDD-0.1	V	PGA off
		GND+0.4		VDD-0.8	V	PGA on
Differential Input Range	V_{RANGE}		±VEXT/GAIN		V	
Input Leakage			±1		nA	PGA off
Low-side Switch Resistance	R_{SW}			8	ohm	
DAC						
DAC Resolution			12		Bits	
Differential Nonlinearity	DNL			0.5	LSB	
Integral Nonlinearity	INL			1	LSB	
Output Load Resistance	R_{LOAD}	1			kohm	
Output Load Capacitance	C_{LOAD}			15	nF	
Output Shorted Current	I_{LIMIT}		20		mA	
DAC Clamp High Level	V_{clampH}	0.75		1	VFS	Set by 'DAC_limit_h'
DAC Clamp Low Level	V_{clampL}	0		0.25	VFS	Set by 'DAC_limit_l'
Serial Interface						
Serial Clock Frequency	F_{sclk}			10	MHz	SPI Interface
				400	kHz	I^2C Interface

5. Register Description

All the NSA2300 registers can be departed into normal registers and OTP registers. The normal registers are used to send a conversion command to the NSA2300, read back the conversion data and perform the OTP blowing. The OTP registers are used to store the configurations and calibration coefficients for the NSA2300, whose default values can be programmed by the inside OTP banks.

5.1. Normal Registers

IF_CTRL(R/W)

Address	*Bit*	*Register Name*	*Default*	*Description*
0x00	7, 0	SDO_active	1'b1	0: SPI3-wire. 1: SPI4-wire (SDO as serial output).
	6, 1	LSB_first	1'b0	0: SPI MSB first. 1: SPI LSB first.
	5, 2	Soft_reset	1'b0	Reset all the NSA2300 registers (except 'Margin'), automatically come back to 0 after reset complete.
	4, 3	Reserved	1'b0	Reserved.

Part_ID(Read only)

Address	Bit	Register Name	Default	Description
0x01	7 – 3	Part_ID<7:0>	0x00	OTP programmed 8 bits Part ID, corresponding to OTP register Reg0xA4. Read only from the address 0x01.

Status(Read only)

Address	Bit	Register Name	Default	Description
0x02	7 – 4	Error_code<7:0>	4'b0000	When diagnostic function enabled, These bits store the error information. 4'b1000: VINP short to VDD. 4'b0100: VINP short to GND. 4'b0010: VINN short to VDD. 4'b0001: VINN short to GND.
	3 – 1	Reserved	3'b000	Reserved.
	0	DRDY	1'b0	1: Conversion complete indicator, output data is ready for reading.

Data_out (Read only, Primary channel data register)

Address	Bit	Register Name	Default	Description
0x06	7 – 0	Data_out<23:16>	0x00	When 'Raw_data_on' = 1, stores the ADC output data. When 'Raw_data_on' = 0, stores the calibrated data.
0x07	7 – 0	Data_out<15:8>	0x00	
0x08	7 – 0	Data_out<7:0>	0x00	

Temp_out (Read only, temperature channel data register)

Address	Bit	Register Name	Default	Description
0x09	7 – 0	Temp_out<15:8>	0x00	Temperature output with an LSB equals to (1/256) °C.
0x0a	7 – 0	Temp_out<7:0>	0x00	

CMD (R/W, command register)

Address	Bit	Register Name	Default	Description
0x30	7 – 4	Sleep_time<3:0>	0x00	Only active during sleep mode conversion. LSB = 62.5 ms.
	3	Sco	1'b0	Start of conversion, automatically return to 0 after conversion ends (except sleep mode conversion).
	2 – 0	Measurement_ctrl<2:0>	2'b00	3'b000: single shot temperature signal conversion. 3'b001: single shot sensor signal conversion. 3'b010: combined conversion (once temperature conversion immediately followed by once sensor signal conversion). 3'b011: sleep mode conversion (periodically perform once combined conversion with an interval time of 'Sleep_time'). 3'b100: OTP programming mode.

OTP_CMD (Write only)

Address	Bit	Register Name	Default	Description
0x6c	7 – 1	Blow_start<6:0>	0x00	Write these bits into 7'b0110101 to start the OTP blowing. The whole OTP banks would be automatically programmed as what stored in the corresponding OTP registers. The OTP banks can only be programmed once.
	0	Margin	1'b0	Provides a critical read condition to filter out 'weak programmed' bits when OTP reloading during soft reset. It is recommended to set this bit after OTP programmed in factory to check if the OTP banks are reliably programmed.

5.2. OTP Registers

Part_ID(R/W)

Address	Bit	Register Name	Description
0xa4	7 – 0	Part_ID<7:0>	OTP programmed 8 bits Part ID, also can be read from address 0x01.

Sys_config (R/W)

Address	Bit	Register Name	Description
0xa5	7	DAC_on	1: enable analog output. When analog output enabled, NSA2300 continuously performs once temperature conversion after 64/32/16/1 (configured by 'P_T_ratio') times sensor signal conversions, regardless of 'CMD' (reg0x30) register settings.
	6 – 5	P_T_ratio	Set how many sensor signal conversions performed after once temperature conversion during analog output mode. 00: 64 times, 01: 32 times, 10: 16 times, 11: once.
	4	Vout_sel	Set the DAC output full scale range. 0: set the DAC output voltage range to 0 ~ VDD. 1: set the DAC output fixed at a voltage range of 0 ~ 1.5*VEXT.
	3	Regulator_sel	0: set the VEXT voltage to 1.8V. 1: set the VEXT voltage to 3.6V.
	2	Unipolar	0: ADC output in bipolar format. 1: ADC output in unipolar format. (Only take effect when 'Raw_data_on' = 1)
	1	Raw_data_on	0: output calibrated data. 1: output ADC raw data. (Only take effect in single shot sensor signal conversion and single shot temperature conversion)
	0	DIAG_on	1: Enable input diagnosis function.

P_config(R/W)

Address	Bit	Register Name	Description
0xa6	7	Reserved	Reserved
	6	Input_swap	1: swap VINP and VINN inside the NSA2300.

	5 – 3	Gain_P<1:0>	Set the gain of the sensor signal conversion channel. 3'b000: gain=1, 3'b001: gain=2, 3'b010: gain=4, 3'b011: gain=8, 3'b100: gain=16, 3'b101: gain=32, 3'b110: gain=64, 3'b111: gain=128.
	2 – 0	OSR_P<3:0>	Set the over sampling ratio of the sensor signal conversion channel. 3'b000: 1024X, 3'b001: 2048X, 3'b010: 4096X, 3'b011: 8192X, 3'b100: 256X, 3'b101: 512X, 3'b110: 16384X, 3'b111: 32768X.

T_config1(R/W)

Address	*Bit*	*Register Name*	*Description*
0xa7	7 – 6	Temp_sel<1:0>	Select different temperature sensing methods. 2'b00: external temperature sensor with a resistance connected between TEMP and GND inside. 2'b01: external temperature sensor with a current source output via TEMP pin. 2'b10: external temperature sensor. 2'b11: internal temperature sensor.
	5 – 3	Gain_T	Set the gain of the temperature conversion channel. 3'b000: gain=1, 3'b001: gain=2, 3'b010: gain=4, 3'b011: gain=8, 3'b100: gain=16, 3'b101: gain=32, 3'b110: gain=64, 3'b111: gain=128.
	2 – 0	OSR_T	set the over sampling ratio of the temperature conversion channel. 3'b000: 1024X, 3'b001: 2048X, 3'b010: 4096X, 3'b011: 8192X, 3'b100: 256X, 3'b101: 512X, 3'b110: 16384X, 3'b111: 32768X.

T_config2(R/W)

Address	*Bit*	*Register Name*	*Description*
0xa8	7 – 4	Reserved	Reserved
	3 – 0	T_offset_trim<3:0>	Set the offset voltage for external temperature conversion from 0V to VEXT. Refer to Table 6.3.

DAC_limit(R/W)

Address	*Bit*	*Register Name*	*Description*
0xa9	7 – 4	DAC_limit_h<3:0>	Set an upper clamping limit for the analog output from 0.75 ~ 1 VFS.
	3 – 0	DAC_limit_l<3:0>	Set a lower clamping limit for the analog output from 0 ~ 0.25 VFS.

CAL_OTP(R/W)

Address	*Bit*	*Register Name*	*Description*
0xaa	7 – 0	Cal_coeff_1<7:0>	Calibration coefficient.
0xab	7 – 0	Cal_coeff_2<7:0>	Calibration coefficient.
…	…	….	….
0xbb	7 – 0	Cal_coeff_18<7:0>	Calibration coefficient.

Redundancy(R/W)

Address	*Bit*	*Register Name*	*Description*
0xbc	7 – 0	Redundancy <7:0>	A pointer, make the OTP bit it pointed functioning as programmed even if it is programming failed. This is a method to improve the yield of OTP blowing.

6. Function Description

6.1. Overview

The NSA2300 is a highly integrated 24-bit sensor conditioner for applications of high precision low frequency measurement such as pressure transducer, weight scale. It can provide fully calibration for the sensor inherent temperature drift and non-linearity with multiple temperature sensing methods supported. The chip incorporates an in-amp, a buffer and a 24-bit sigma delta modulator followed by a calibration DSP and a 12-bit DAC for the analog output. With wide gain and OSR range, the NSA2300 could be suitable for variance sensors. One-time-programmable fuses are used to store the calibration coefficients for on-chip calibration calculations. SPI, I^2C and OWI interfaces are supported for serial communication.

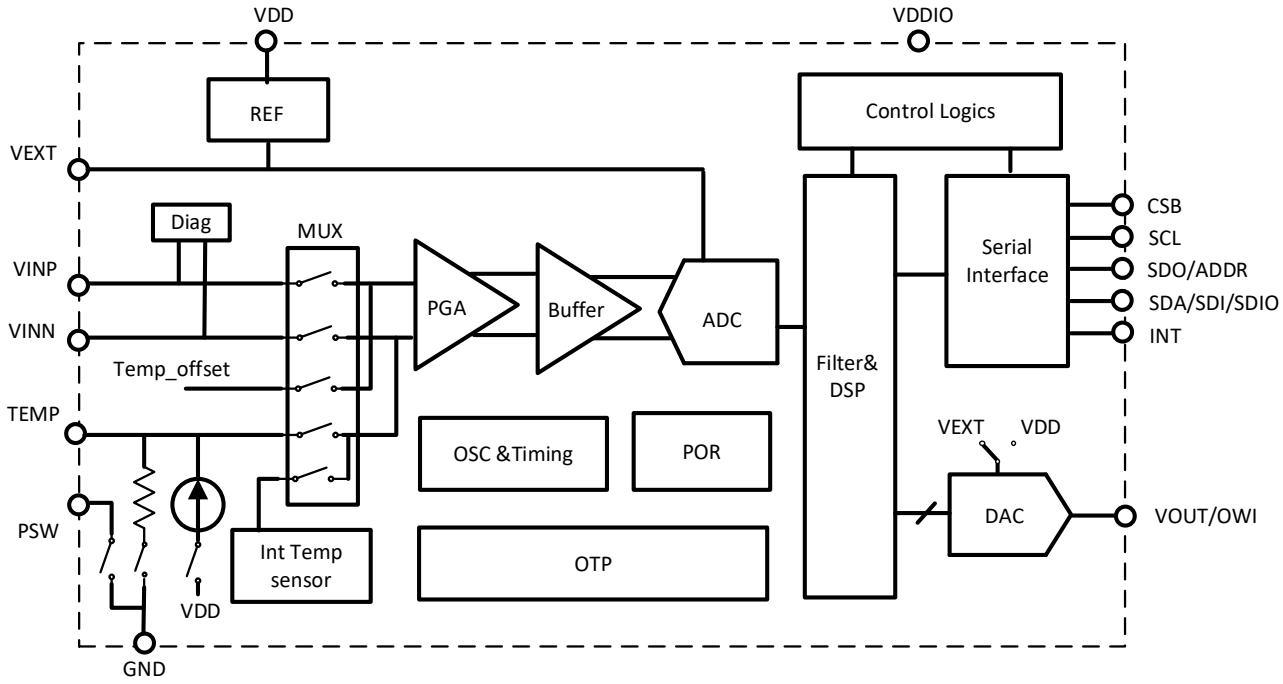


Figure 6.1 Block diagram of the NSA2300

6.2. Signal Path

6.2.1. Analog Inputs and Reference

The reference voltage VREF is defined as the voltage difference between VEXT pin and PSW pin. VEXT pin is powered by the internal 1.8V/3.6V regulator for higher PSRR on a noisy system. The user could also bias this pin externally at a higher voltage, for example, short to VDD, to increase the dynamic range.

A low side switch on the PSW pin connected the low-side of the sensor. Sensor current could be automatically turned off when not in measurement mode.

TEMP pin is used for the external temperature sensor input. With an optional low drift 5kohm pulled down resistance and an optional low drift excitation current source connected, TEMP pin can support multiple external temperature sensing methods.

6.2.2. PGA, Buffer and Modulator

The total gain of the analog path can be separately set for sensor signal channel and temperature channel as 1X, 2X, 4X, 8X, 16X, 32X, 64X and 128X by bits 'Gain_P' and 'Gain_T'. The allowed input range is +-VREF/GAIN where VREF is the voltage difference between VEXT and PSW.

6.2.3. Digital Filter with Programmable Over Sampling Factor

The NSA2300 has a digital decimation filter followed the modulator. The output data rate could be separately programmable for sensor signal channel and temperature channel from 256X to 32768X by setting bits 'OSR_P' and 'OSR_T'. Table 6.1 shows the effective number of bit (ENOB) and Conversion time (T_{cnv}) under different gain, OSR settings. Table6.2 shows the input referred RMS noise.

Table 6.1 ENOB under different OSR and Gain settings (VEXT = 1.8V)

OSR_P	*T_{cnv} (ms)*	*ADC ENOB (Bits)*							
		gain=1	*gain=2*	*gain=4*	*gain=8*	*gain=16*	*gain=32*	*gain=64*	*gain=128*
256X	1.54	17.7	17.6	17.1	17	17.1	16.8	16.4	16
512X	1.86	18	18	17.4	17.3	17.3	17.1	16.8	16.1
1024X	2.5	18.4	18.3	17.8	17.8	17.7	17.5	17	16.3
2048X	3.78	18.9	18.8	18.2	18.2	18.2	17.9	17.4	16.5
4096X	6.34	19.2	19.2	18.6	18.7	18.5	18.3	17.9	17.2
8192X	11.46	19.8	19.8	19	19.1	19.1	18.8	18.4	17.5
16384X	21.7	20.3	20.2	19.5	19.4	19.5	19.3	19	18.1
32768X	42.18	20.8	20.7	20.1	19.7	20.1	19.7	19.4	18.5

Table 6.2 Input Referred RMS noise under different OSR and Gain settings (VEXT = 1.8V)

OSR_P	*T_{cnv} (ms)*	*Input RMS Noise(nV)*							
		gain=1	*gain=2*	*gain=4*	*gain=8*	*gain=16*	*gain=32*	*gain=64*	*gain=128*
256X	1.54	16907.2	9060.3	6406.6	3433.2	1601.7	985.9	650.5	429.2
512X	1.86	13732.9	6866.5	5203.8	2788.6	1394.3	800.8	493.0	400.4
1024X	2.5	10407.6	5577.3	3943.7	1971.9	1056.7	606.9	429.2	348.6
2048X	3.78	7359.3	3943.7	2988.8	1494.4	747.2	460.0	325.2	303.5
4096X	6.34	5977.6	2988.8	2265.1	1056.7	606.9	348.6	230.0	186.8
8192X	11.46	3943.7	1971.9	1716.6	800.8	400.4	246.5	162.6	151.7
16384X	21.7	2788.6	1494.4	1213.8	650.5	303.5	174.3	107.3	100.1
32768X	42.18	1971.9	1056.7	800.8	528.3	200.2	132.1	81.3	75.9

6.3. Function Mode

6.3.1. Single-shot Sensor Signal Conversion

Setting 'Measurement_ctrl' = 01 and 'Sco' = 1 will initiate once single-shot sensor signal conversion. After the chip performs once sensor signal conversion, it returns back to standby mode with automatically changing 'Sco' to 0. INT goes high when data is ready and returns low after the data value (0x06-0x08) has been read out from the 'Data_out' registers. The 'Data_out' registers can be read several times if required, even when the INT pin is low, but care must be taken not to read data when the 'Data_out' registers are just in refreshing.

The gain of the sensor signal conversion channel can be configured by the bits 'Gain_P' from 1X to 128X and the OSR for the sensor conversion is configured by the 'OSR_P' bits from 256X to 32768X, the tradeoff of the conversion time and the output RMS noise under different OSR settings is shown in Table 6.1/6.2.

A following calibration DSP is optional during the single-shot sensor signal conversion. When the DSP is enabled ('Raw_data_on'=0), a 24-bit calibrated sensor data will be stored in the 'Data_out' registers after conversion ends, and else, the raw 24-bit ADC output is stored there. The relationship between the raw ADC data and the input signals for the sensor signal conversion is shown below.

$$RAW_{Data} = \frac{VINP-VINN}{VREF} * Gain\_P * 2^{23} \quad \text{('Unipolar' = 0)}$$

$$RAW_{Data} = \frac{VINP-VINN}{VREF} * Gain\_P * 2^{23} + 2^{23} \quad \text{('Unipolar' = 1)}$$

6.3.2. Single-shot Temperature Conversion

Different temperature sensing methods are supported by the NSA2300, either internally or externally. The 'Temp_sel' bits support four configures for the temperature measurement. Set 'Temp_sel' = 2'b11 to choose the internal temperature sensor.

For the external temperature sensing methods, the pin TEMP is used as the temperature signal input and the other end of the differential temperature signal pair is generated inside and can be configured by 'T_offset_trim' bits from 0 to VEXT with an minimum step of 1/15VEXT (Table 6.3).

Table 6.3 Temp offset voltage under different 'T_offset_trim' settings

T_offset_trim	*Offset Voltage*
4'b0000	8/15 VEXT
4'b0001	9/15 VEXT
4'b0010	10/15 VEXT
4'b0011	11/15 VEXT
4'b0100	12/15 VEXT
4'b0101	13/15 VEXT
4'b0110	14/15 VEXT
4'b0111	VEXT
4'b1000	0
4'b1001	1/15 VEXT
4'b1010	2/15 VEXT
4'b1011	3/15 VEXT
4'b1100	4/15 VEXT
4'b1101	5/15 VEXT
4'b1110	6/15 VEXT
4'b1111	7/15 VEXT

During external temperature sensing, a low temperature drift 5kohm pulled down resistance or a low temperature drift excitation current source can be optional connected to the TEMP pin to support multiple temperature sensing methods. Typical applications for these temperature measurement methods are shown below. Rt could be either the sensor bridge itself or an extra temperature sensing element close to the senor.

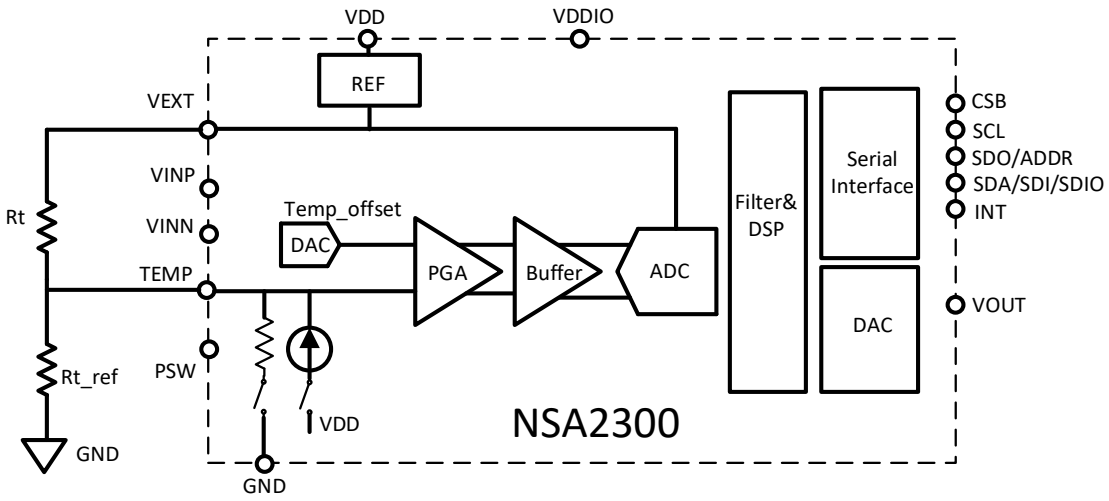


Figure 6.2 External Temperature Sensing ('Temp_sel' = 2'b10)

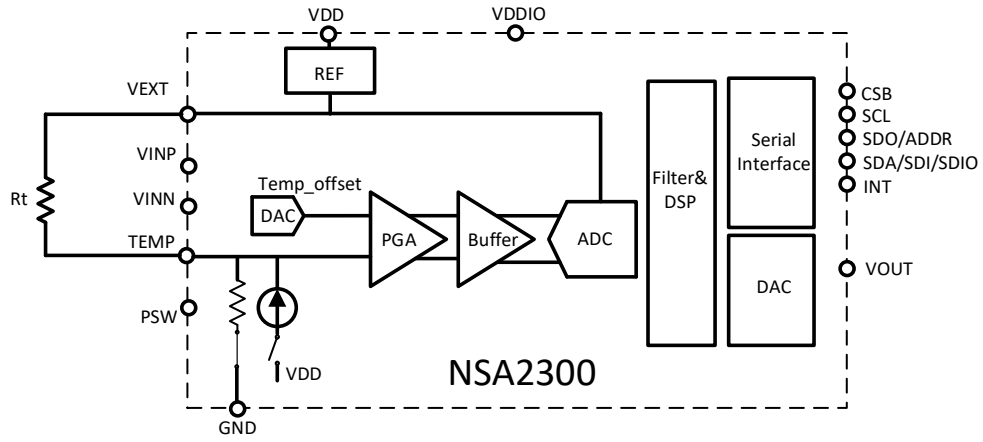


Figure 6.3 External Temperature Sensing with a 5kohm Pull-down Resistor ('Temp_sel' = 2'b00)

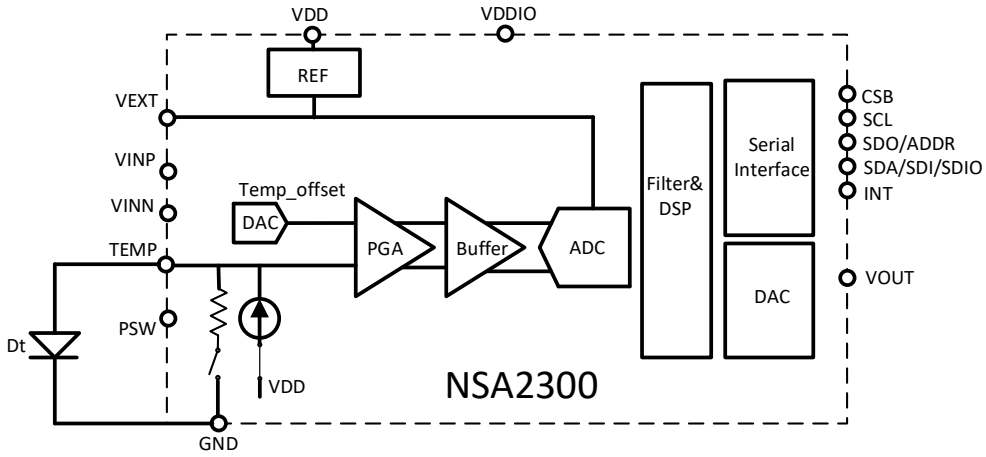


Figure 6.4 External Temperature Sensing with a 20μA Current Source ('Temp_sel' = 2'b01)

Setting 'Measurement_ctrl' = 2'b00 and 'Sco' = 1'b1 will initiate once single-shot temperature conversion. After the chip performs once temperature conversion, it returns back to standby mode with automatically changing 'Sco' to 1'b0. When setting 'Raw_data_on' = 1'b0, the calibrated temperature data is stored in "Temp_out" registers and else, the raw ADC data of the temperature channel conversion would be stored in the "Data_out" registers. INT pin also goes high when the conversion ends and will return low after a reading of the "Temp_out" or "Data_out" registers.

The gain of the external temperature conversion channel can be configured by the bits 'Gain_T' from 1X to 128X and the gain of the internal temperature conversion channel is fixed. The OSR for the sensor conversion is configured by the 'OSR_T' bits from 256X to 32768X.

6.3.3. Combined Conversion

Setting 'Measurement_ctrl' = 2'b10 and 'Sco' = 1'b1 will initiate once combined conversion. After the chip successively performs once temperature conversion and once sensor signal conversion, it returns back to standby mode with automatically changing 'Sco' to 1'b0. The 'Raw_data_on' bit should be set 0 during combined conversion and the calibrated temperature data and sensor signal data are separately stored in 'Temp_out' and 'Data_out' registers. INT pin will go high when the sensor signal conversion ends and will return low after a reading of the "Data_out" registers.

The gain and OSR of the temperature channel and sensor signal channel are separately configured by the bits 'Gain_P', 'OSR_P', 'Gain_T' and 'OSR_T' just as the single shot conversions.

6.3.4. Sleep Conversion

Setting 'Measurement_ctrl' = 2'b11 and 'Sco' = 1'b1 will get the chip into sleep conversion mode. The chip periodically performs once temperature conversion, once sensor signal conversion and a sleep phase. The duration of the sleep phase is configured by the 'Sleep_time' bits from approximately 64ms to 1s. The chip will not get back to standby mode until manually setting 'Sco' bit to '0'. The 'Raw_data_on' bit will be forced to 0 during sleep conversion and the calibrated temperature data and sensor signal are separately stored in 'Temp_out' and 'Data_out' registers. INT pin will go high when the sensor signal conversion ends and will automatically return low before next temperature conversion starting or after a reading of the "Data_out" registers.

The gain and OSR of the temperature channel and sensor signal channel are separately configured by the bits 'Gain_P', 'OSR_P', 'Gain_T' and 'OSR_T' just as the single shot conversions.

6.4. Analog Output Mode

Setting 'DAC_on' = 1'b1 will get the chip into analog output mode (regardless of 'CMD' registers contents). During analog output mode, the NSA2300 alternately performs 64/32/16/1 times pressure conversions and once temperature conversion automatically. The higher 12 bits (without the sign bit) of the calibrated pressure data will be mapped to the VOUT pin with the equations below and all negative 'Data_out' values will be mapped to the lower limit voltage. Calibration coefficients must be carefully set in this mode to make the full span of the pressure data occupies the full span of the output voltage.

$$VOUT = \frac{Data\_out[22:11]}{4096} * VDD \qquad \text{('Vout_sel' = 1'b0)}$$

$$VOUT = \frac{Data\_out[22:11]}{4096} * 1.5 * VEXT \qquad \text{('Vout_sel' = 1'b1)}$$

The DAC allows programming a lower and upper clamping limit for the output signal. The internal 12-bit calculated value is compared with the 12-bit value formed by {11, DAC_limit_h[3:0],111111} for the upper limit and {00,DAC_limit_l[3:0],000000} for the lower limit. If the calculated value is higher than the upper limit or less than the lower limit, the analog output value is clamped to this value; otherwise it is output as is.

6.5. Diagnosis

A suite of input diagnostic feature is provided on NSA2300 through several fault monitor comparators, refer to Figure 6.5.

When diagnostics are enabled by setting 'DIAG_on' to 1'b1, two branches of 100nA current sources are added on the input pair from sensor power supply. This will add some voltage shift to the input signal, but mostly common mode drift and any error introduced could be minimized during sensor calibration. Four comparators are used to monitor if the voltage is in 100mV range of VEXT or ground. User could use this information to find out sensor faults like loss of bridge positive, loss of bridge negative, open sensor connection and sensor input short.

The outputs of all the comparators are locked into the 'Error_code<3:0>' register at the end of every data conversion. When either of the fault comparator outputs is asserted, indicating a fault, NSA2300 analog output VOUT will be forced to a fault indicating voltage level of 2.5% of VDD. Together with the lower or upper clip limit function, system diagnostic can be performed to determine if the sensor is detective, or the process being monitored by the sensor is out of range.

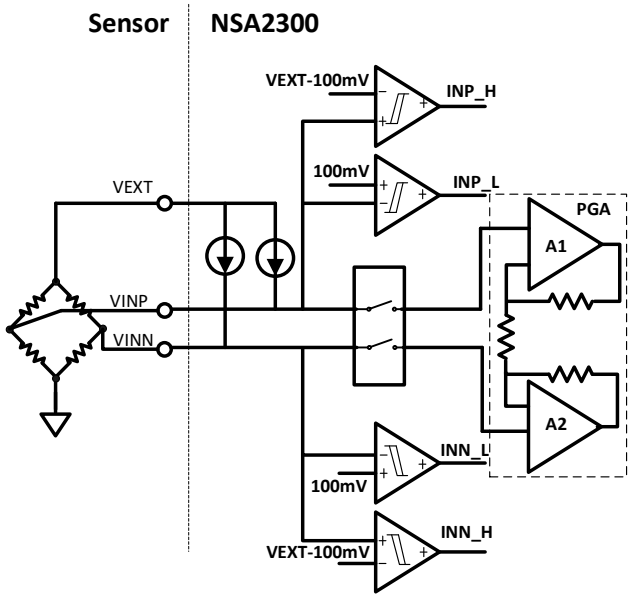


Figure 6.5 NSA2300 Input Diagnostic Diagram

6.6. OTP

The NSA2300 contains 224 OTP bits. The lower 200 bits are released to customer to program the default configurations and the sensor calibration coefficients, and the higher 24bits are reserved for internal trimming and will be pre-programmed in factory. The reg0xbc and its corresponding OTP bits are used as OTP redundancy pointer, which can write one OTP bit address and make this OTP bit functioning as programmed even if it has not been programmed or programming failed. For example, writing 0x1a to Reg0xbc make the 26th OTP bit functioning as being programmed. It's been successfully written, even though the 26th OTP didn't be actually programmed. This design is to improve the OTP burn yield in the production process.

To program the OTP bits, please follow steps below:

1. Write all OTP registers what you want to program.
2. Switch the supply voltage on the VDD pin to 6.5V
3. Write Reg0x30 with 0x0C to enter OTP program mode.
4. Write Reg0x6C with 8'b01101010 to start OTP programming.
5. Waiting 10ms.
6. Switch the supply voltage on the VDD back to 2.5V.
7. Write Reg0x6C with 8'b00000001 to set the OTP read out margin.
8. Write Reg0x00 with 0x24 to soft reset the NSA2300.
9. Read the OTP banks back to check if program succeeded.

6.7. Sensor Calibration

NSA2300 offers an on-chip calibration for sensor offset, sensitivity, temperature drift and non-linearity with the equations below and the maximum range for sensors that can be calibrated by NSA2300 is shown in Table 6.4. To get the calibration coefficient for a particular sensor, please contact NOVOSENSE for coefficient calculating kits.

$$P' - P_0 = (CNT_{sense} - (CNT_{off} + CTC_1(T - T_0) + CTC_2(T - T_0)^2)) * (S_0 + STC_1(T - T_0) + STC_2(T - T_0)^2)$$

$$P - P_0 = (P' - P_0) + K_s \cdot (P' - P_0)^2 + K_{ss} \cdot (P' - P_0)^3$$

Table 6.4 Maximum range of sensors allowed for NSA2300

Symbol	Description	Min	Max	Unit
V_{fs}	Full Span	+/-0.001	+/-1	V/V
STC1	1st order temperature coefficient of sensitivity	-0.0078	0.0078	Vfs/℃
STC2	2nd order temperature coefficient of sensitivity	-1.5e-5	1.5e-5	Vfs/℃²
V_{off}	Sensor offset	-1/GAIN < V_{off}+V_{fs}< 1/GAIN		V/V
CTC1	1st order temperature coefficient of sensitivity	-0.0078	0.0078	V/V/℃
CTC2	2nd order temperature coefficient of sensitivity	-1.5e-5	1.5e-5	V/V/℃²
Ks	2nd order nonlinearity coefficient	-0.25	0.25	1/Vfs
Kss	3rd order nonlinearity coefficient	-0.25	0.25	1/Vfs

Also, NSA2300 offers an on-chip calibration for both external and internal temperature sensing methods. After calibration, the NSA2300 can offer a real time temperature value of +/- 1℃ accuracy with the built-in temperature sensor during -40℃ and 85℃. Please contact NOVOSENSE for coefficient calculating kits.

6.8. Serial Interface

NSA2300 provides both SPI and I²C interface for serial communication and 'CSB' pin is used to switch between these two protocols. Pulling 'CSB' pin low selects the SPI interface, leaving 'CSB' pin float or puling it high selects the I²C interface.

6.8.1. SPI Interface

Table 6.5 SPI interface specifications

Symbol	Parameter	Condition	Min	Max	Unit
f_{sclk}	Clock frequency	Max load on SDIO or SDO = 25pF		10	MHz
t_{sclk_l}	SLCK low pulse		20		ns
t_{sclk_h}	SLCK high pulse		20		ns
T_{sdi_setup}	SDI setup time		20		ns
T_{sdi_hold}	SDI hold time		20		ns
T_{sdo_od}	SDO/SDI output delay	Load = 25pF		30	ns
		Load = 250pF		40	ns
T_{csb_setup}	CSB setup time		20		ns
T_{csb_hold}	CSB hold time		40		ns

The figure below shows the definition of the SPI timing given in Table 6.5.

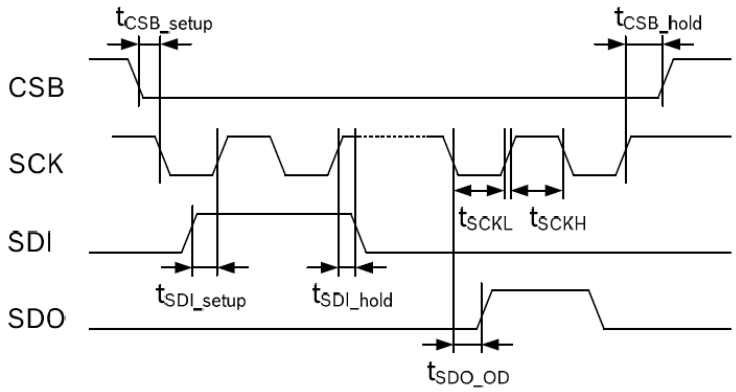


Figure 6.6 SPI timing diagram

The falling edge of CSB, in conjunction with the rising edge of SCLK, determines the start of framing. Once the beginning of the frame has been determined, timing is straightforward. The first phase of the transfer is the instruction phase, which consists of 16 bits followed by data that can be of variable lengths in multiples of 8 bits. If the device is configured with CSB tied low, framing begins with the first rising edge of SCLK.

The instruction phase is the first 16 bits transmitted. As shown in Figure 6.7, the instruction phase is divided into several bit fields.

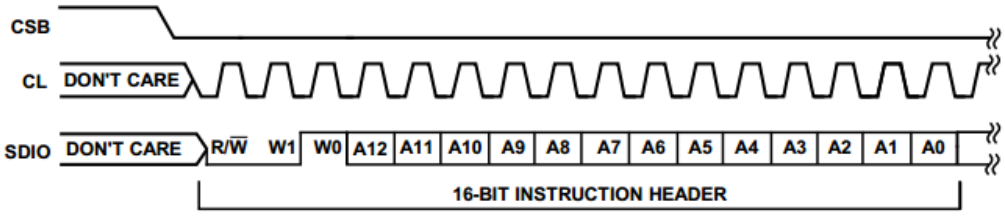


Figure 6.7 Instruction Phase Bit Field

The first bit in the stream is the read/write indicator bit (R/W). When this bit is high, a read is being requested, otherwise indicates it is a write operation.

W1 and W0 represent the number of data bytes to transfer for either read or write (Table 6.6). If the number of bytes to transfer is three or less (00, 01, or 10), CSB can stall high on byte boundaries. Stalling on a non-byte boundary terminates the communications cycle. If these bits are 11, data can be transferred until CSB transitions high. CSB is not allowed to stall during the streaming process.

The remaining 13 bits represent the starting address of the data sent. If more than one word is being sent, sequential addressing is used, starting with the one specified, and it either increments (LSB first) or decrements (MSB first) based on the mode setting.

Table 6.6 W1 and W0 settings

W1:W0	***Action***	***CSB Stalling***
00	1 byte of data can be transferred.	Optional
01	2 bytes of data can be transferred.	Optional
10	3 bytes of data can be transferred.	Optional
11	4 or more bytes of data can be transferred. CSB must be held low for entire sequence; otherwise, the cycle is terminated.	No

Data follows the instruction phase. The amount of data sent is determined by the word length (Bit W0 and Bit W1). This can be one or more bytes of data. All data is composed of 8-bit words.

Data can be sent in either MSB-first mode or LSB-first mode (by setting 'LSB_FIRST' bit). On power up, MSB-first mode is the default. This can be changed by programming the configuration register. In MSB-first mode, the serial exchange starts with the highest-order bit and ends with the LSB. In LSB-first mode, the order is reversed.

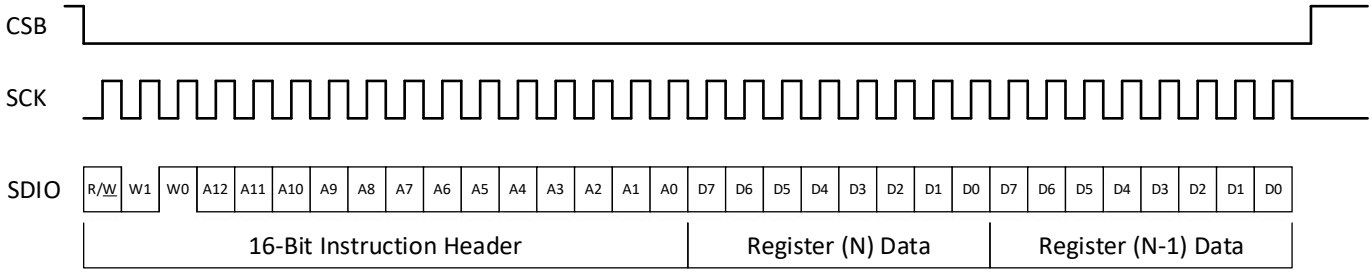


Figure 6.8 MSB First Instruction and Data Phases

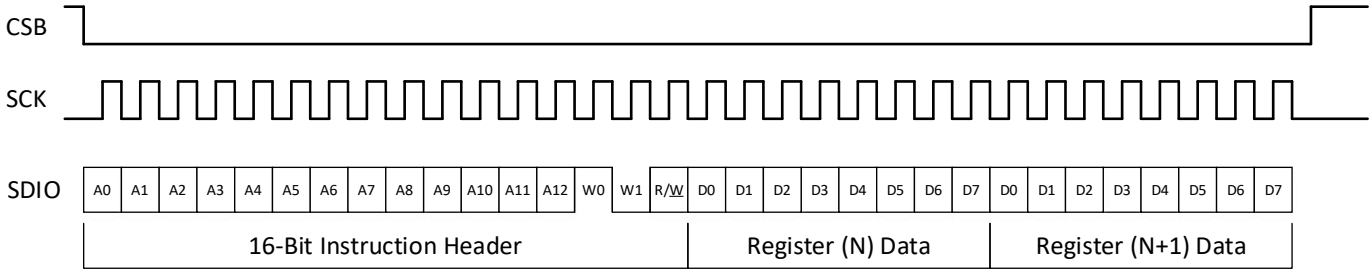


Figure 6.9 LSB First Instruction and Data Phases

Register bit 'SDO_ACTIVE' is responsible for activating SDO on devices. If this bit is cleared, then SDO is inactive and read data is routed to the SDIO pin. If this bit is set, read data is placed on the SDO pin. The default for this bit is 1, making SDO active.

6.8.2. I²C Interface

I²C bus uses SCL and SDA as signal lines. Both lines are connected to VDDIO externally via pull-up resistors so that they are pulled high when the bus is free. The I²C device address of NSA2300 is shown below. The LSB bit of the 7bits device address is configured via SDO/ADDR pin.

Table 6.7 I²C Address.

A7	*A6*	*A5*	*A4*	*A3*	*A2*	*A1*	*W/R*
1	1	0	1	1	0	SDO/ADDR	0/1

Table 6.8 Electrical specification of the I²C interface pins

Symbol	*Parameter*	*Condition*	*Min*	*Max*	*Unit*
f_{scl}	Clock frequency			400	kHz
t_{LOW}	SCL low pulse		1.3		µs
t_{HIGH}	SCL high pulse		0.6		µs
t_{SUDAT}	SDA setup time		0.1		µs
t_{HDDAT}	SDA hold time		0.0		µs
t_{SUSTA}	Setup Time for a repeated start condition		0.6		µs
t_{HDSTA}	Hold time for a start condition		0.6		µs
t_{SUSTO}	Setup Time for a stop condition		0.6		µs
t_{BUF}	Time before a new transmission can start		1.3		µs

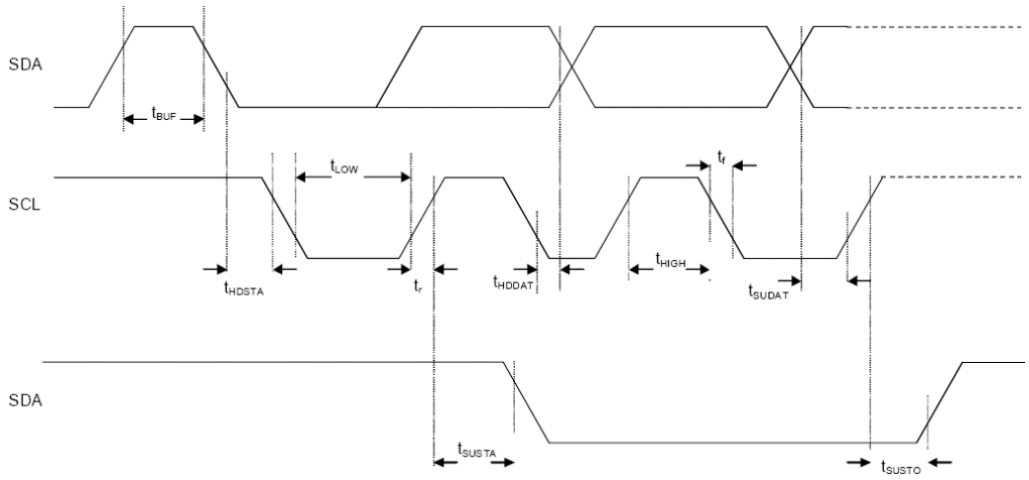


Figure 6.10 I²C Timing Diagram

The I²C interface protocol has special bus signal conditions. Start (S), stop (P) and binary data conditions are shown below. At start condition, SCL is high and SDA has a falling edge. Then the slave address is sent. After the 7 address bits, the direction control bit R/W selects the read or write operation. When a slave device recognizes that it is being addressed, it should acknowledge by pulling SDA low in the ninth SCL (ACK) cycle.

At stop condition, SCL is also high, but SDA has a rising edge. Data must be held stable at SDA when SCL is high. Data can change value at SDA only when SCL is low.

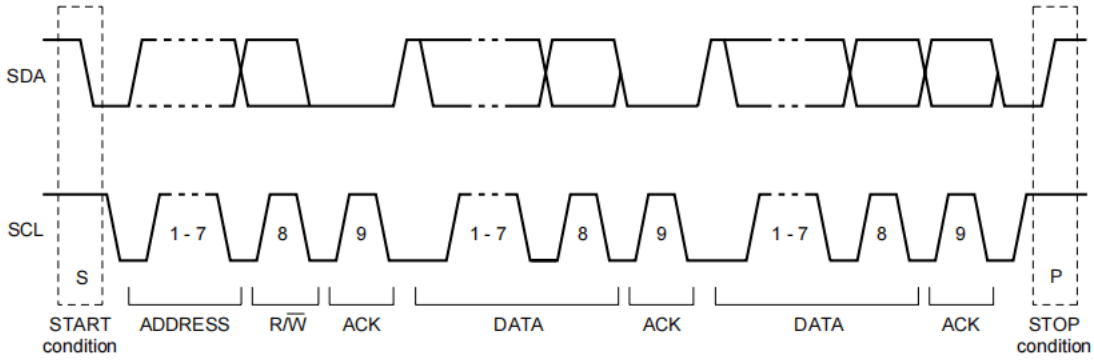


Figure 6.11 I2C Protocol

NSA2300 can support single byte and multiple bytes operation. The data format is shown in the figure below.

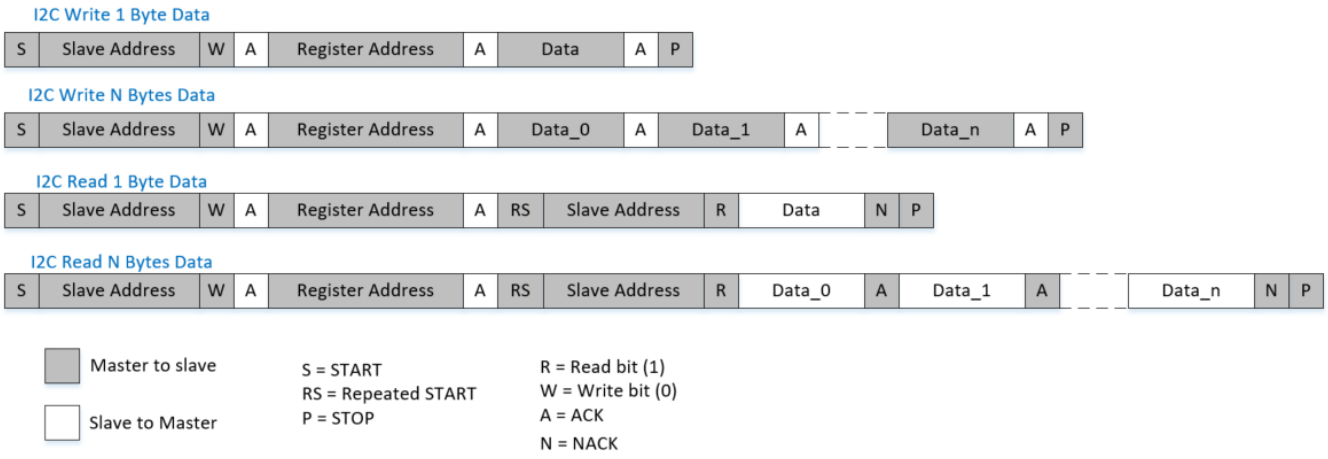


Figure 6.12 I²C Transfer Format

6.8.3. OWI Interface

Besides the SPI and I²C interfaces, the NSA2300 also employs a one wire digital interface (OWI), which combines a simple and easy protocol with a cost saving pin sharing. Both the analog voltage output and this digital interface occur over the same pin. An advantage of this OWI interface is that it enables "end of line" calibration – no additional pins are required to digitally calibrate a finished assembly.

6.8.3.1 Timing Specification

Table 6.9 OWI Timing Specification

Symbol	*Description*	*Min.*	*Typ.*	*Max.*	*Unit*
t_{period}	OWI bit period	20		100	µs
t_{pulse_0}	Duty cycle for 0	1/8	1/4	3/8	t_{period}
t_{pulse_1}	Duty cycle for 1	5/8	3/4	7/8	t_{period}
t_{start}	Start low pulse time	10			µs
t_{stop}	Stop condition time		512		µs
t_{OWI_IDLE}	Bus free time between start and stop condition	10			µs
t_{Bit_dev}	Bit period deviation	0.75	1	1.25	t_{period}

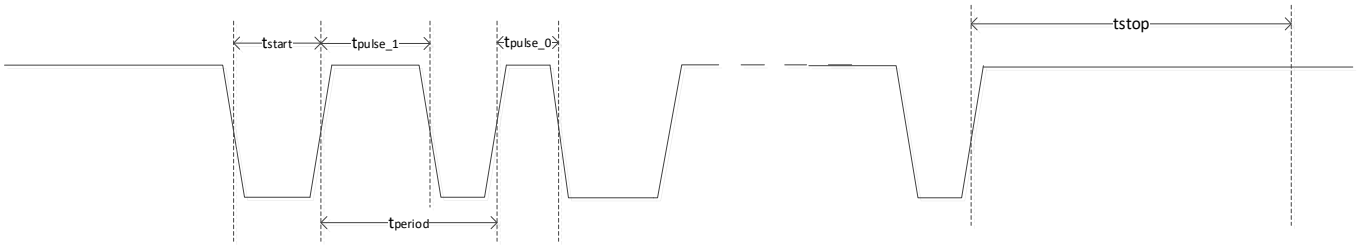


Figure 6.13 OWI Timing

6.8.3.2 Enter OWI Mode

The NSA2300 opens a 20ms-time-slot after power-on – the one wire start window. If in this time-slot one wire communication (a transition from high voltage to low voltage) is detected, the device enters the one wire mode. If no one wire communication occurs in the start window the interface leaves the one wire mode and changes to I²C or SPI mode. The one wire start window can be suppressed by configuration (OWI_dis = 1) if no access via one wire communication is desired.

6.8.3.3 OWI Protocol

The OWI protocol used is defined as follows:

a) Idle State

During inactivity of the bus, OWI line is pulled-up to high voltage level.

b) Start Condition

When OWI line is in idle mode a low pulse (return to high) with minimum width of 10us indicates a start condition. Every command has to be initiated by a start condition sent by a master. A master can generate a start condition only when OWI line is in idle mode.

c) Stop Condition

The master finishes a transmission by changing back to high level (idle mode). Every command (refer "write operation") has to be closed by a stop condition to start processing the command. The master can interrupt a sending slave after data request (refer "read operation") by clamping the OWI line to low level for generating a stop condition. No transition from low to high

or from high to low (constant level) at OWI line for at least twice the period of last transmitted valid bit indicates a stop condition. A stop condition without considering last bit-time (secure stop condition) is generated at constant level at OWI line for more than 512us.

d) Addressing

After the start condition the master has to send a register address, consisting of an 8-bit register address and a read/write–bit (0–write, 1–read). The register address is part of the protocol and indicates which register you will write into or read from.

e) Valid Data

One byte data (8 bits) will be transmitted during once transmission (write or read) with the most significant bit (MSB) first. Transmitted bits are recognized after a start condition at every transition from low to high at OWI line. The value of the transmitted bit depends on the duty ratio between high phase and high/low period. A duty ratio greater than 1/8 and less than 3/8 is detected as '0', a duty ratio greater than 5/8 and less than 7/8 is detected as '1'. The bit period of consecutive bits may not change more than with factor of 2 because stop condition is detected in this case.

f) Write Operation

During transmission from master to slave (WRITE), the read/write bit is followed by 1/2/3/4 bytes (according to the byte NO. bits) transmitted data (MSB first), and the addressed register and follows will be refreshed to the written data after a stop condition.

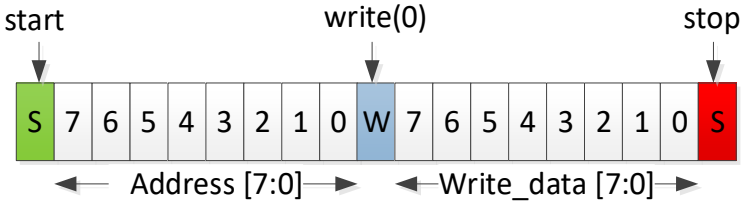


Figure 6.14 OWI Write Operation

g) Read Operation

After a data request from master to slave by sending a register address byte and a read-bit, the slave answers by sending data from the activated registers. The slave generates the data bits with a bit period equal to last received bit (R/W bit). After 8 bits data transmitted, the slave goes back to idle period automatically. Or the master can interrupt a sending slave after data request by clamping the OWI line to low level for at least twice the period of last transmitted valid bit to generate a stop condition to make the salve back to idle period.

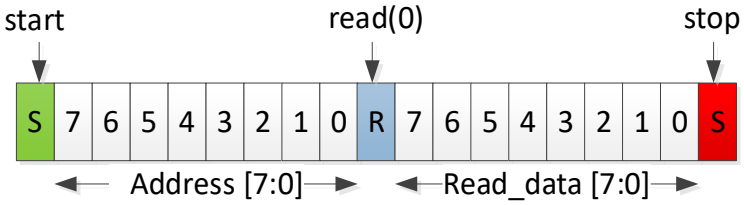


Figure 6.15 OWI Read Operation

7. Application Note

7.1. Typical Application 1: I²C Mode for Bare Die

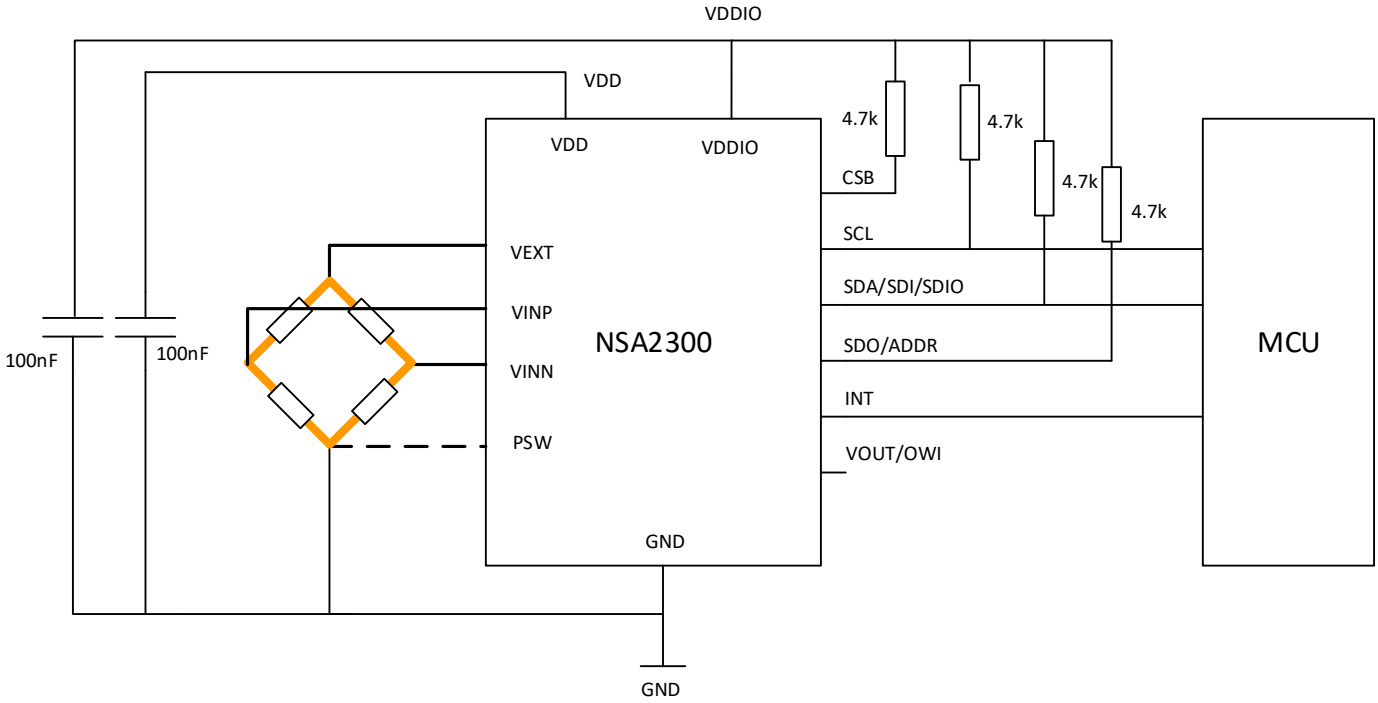


Figure 7.1 Typical Application (I²C Mode)

7.2. Typical Application 2: SPI Mode for Bare Die

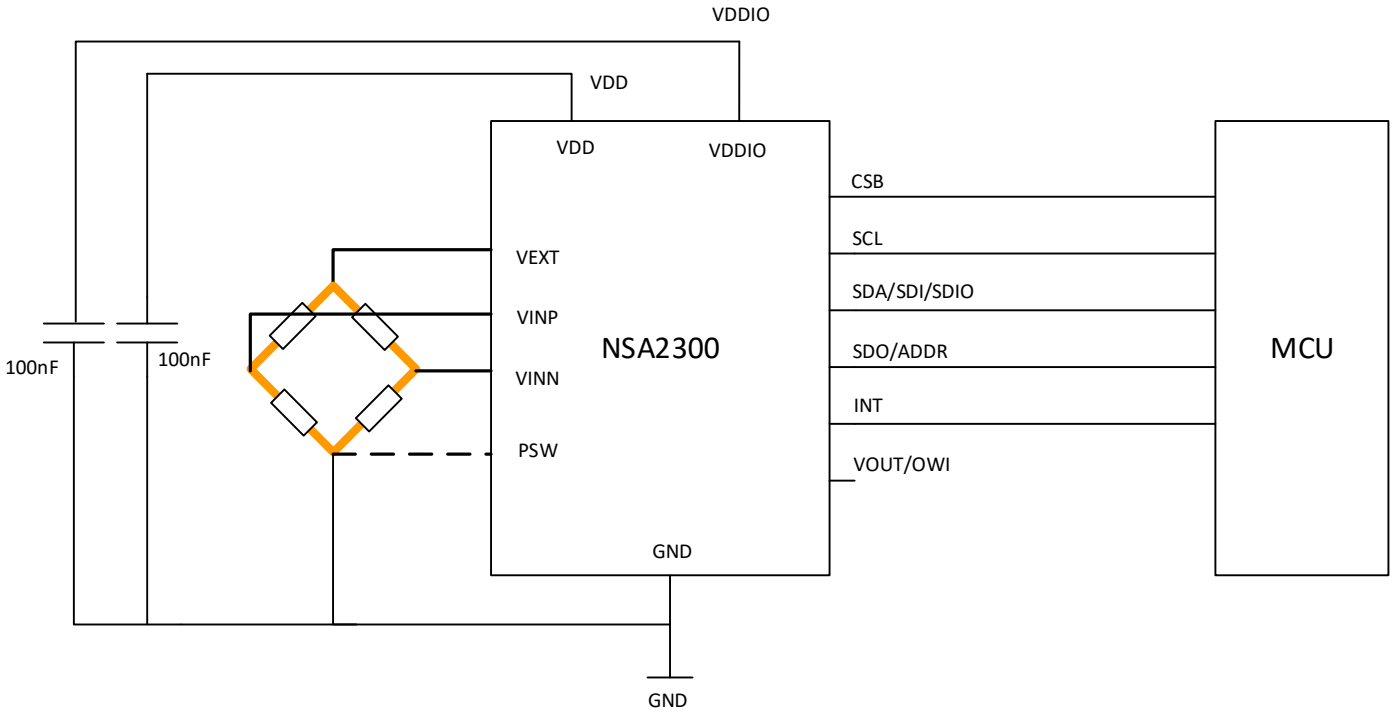


Figure 7.2 Typical Application (SPI Mode)

7.3. Typical Application 3: OWI Mode for Bare Die

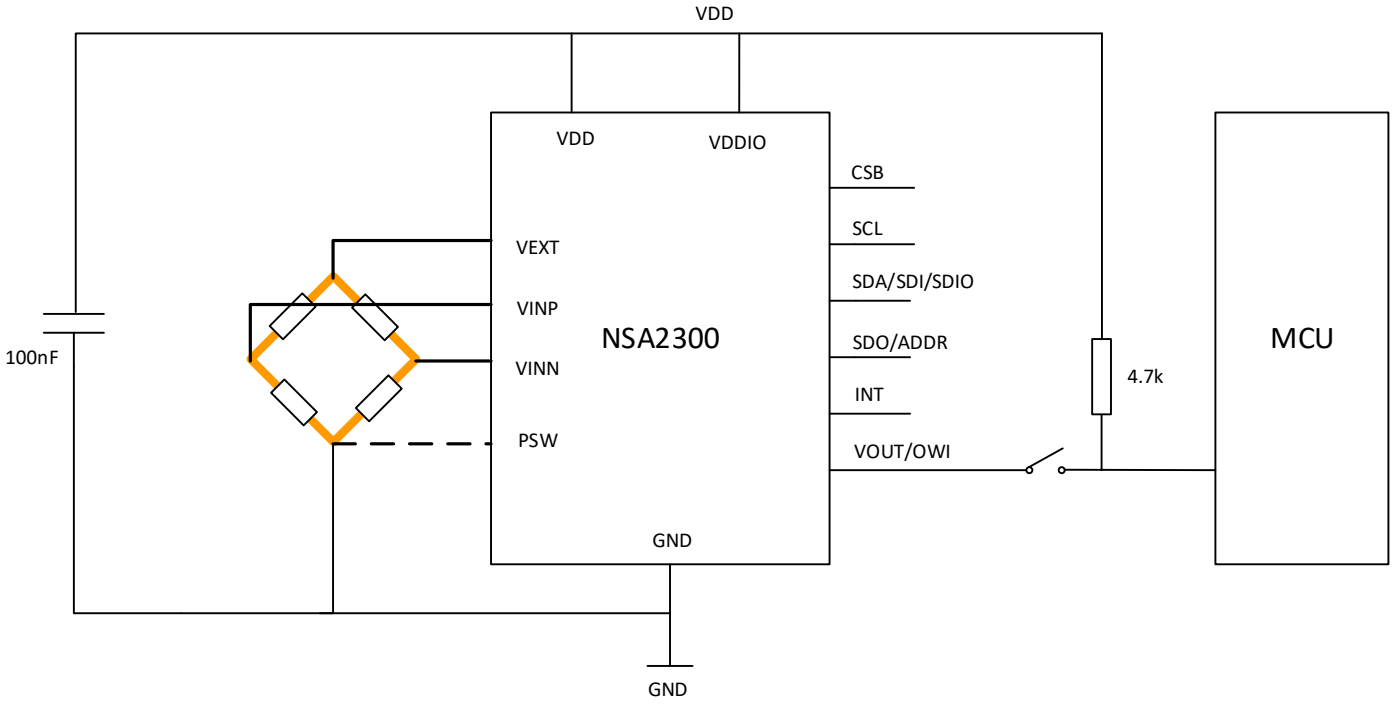


Figure 7.3 Typical Application (OWI Mode)

7.4. Typical Application 4: I²C Mode for SOP8 Packaged Chip

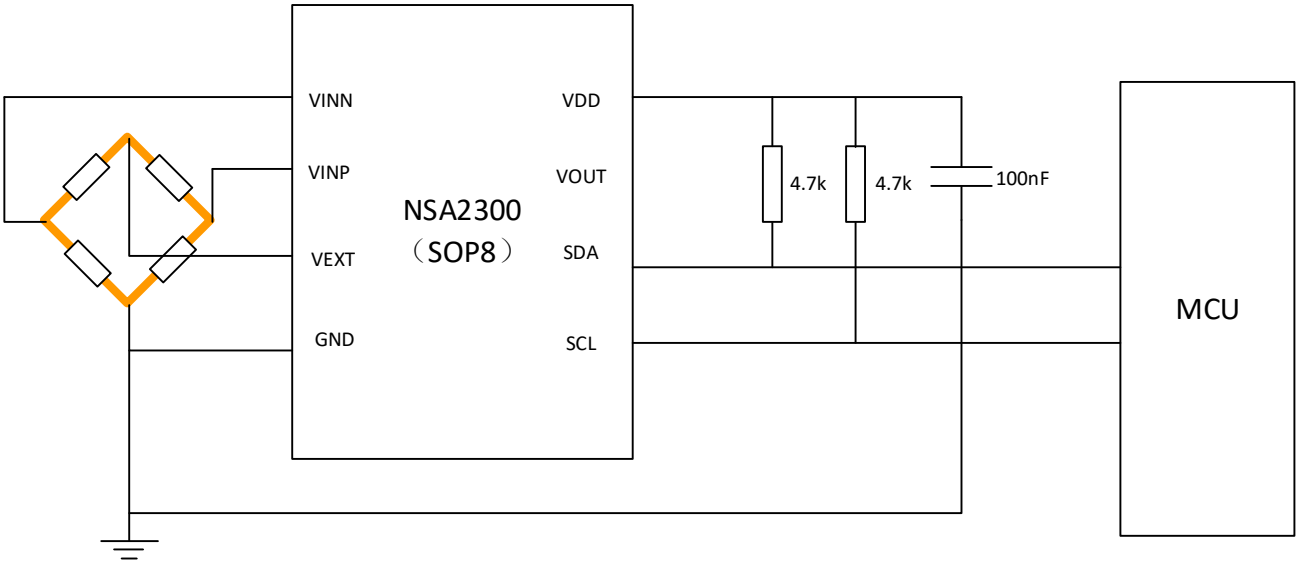


Figure 7.4 Typical Application for SOP8 packaged chip (I²C Mode)

7.5. Typical Application 5: OWI Mode for SOP8 Packaged Chip

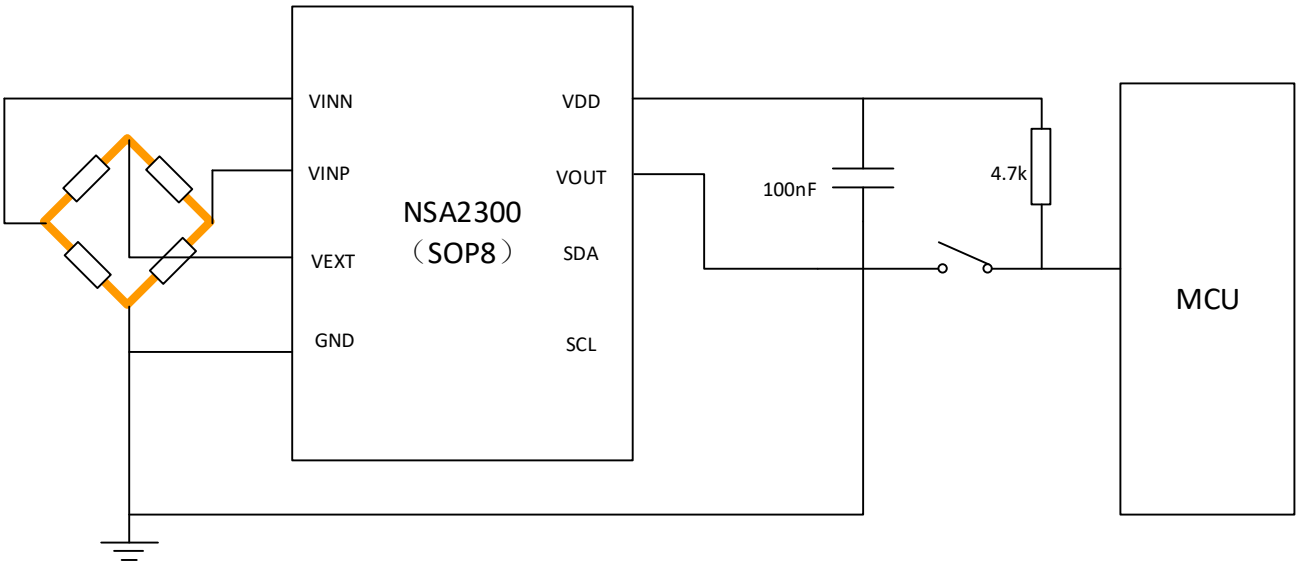


Figure 7.5 Typical Application for SOP8 packaged chip (I^2C Mode)

8. Package Information

8.1. Bare Die

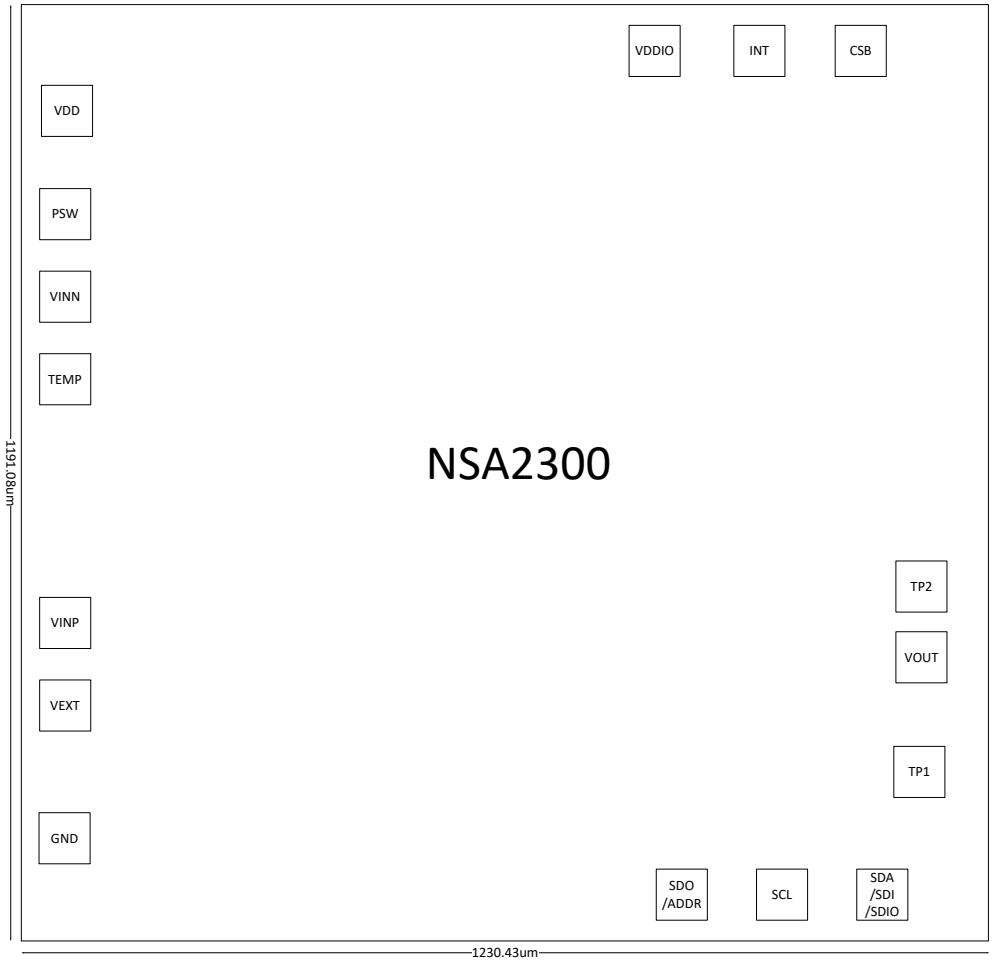


Figure 8.1 NSA2300 Die Pin Assignment

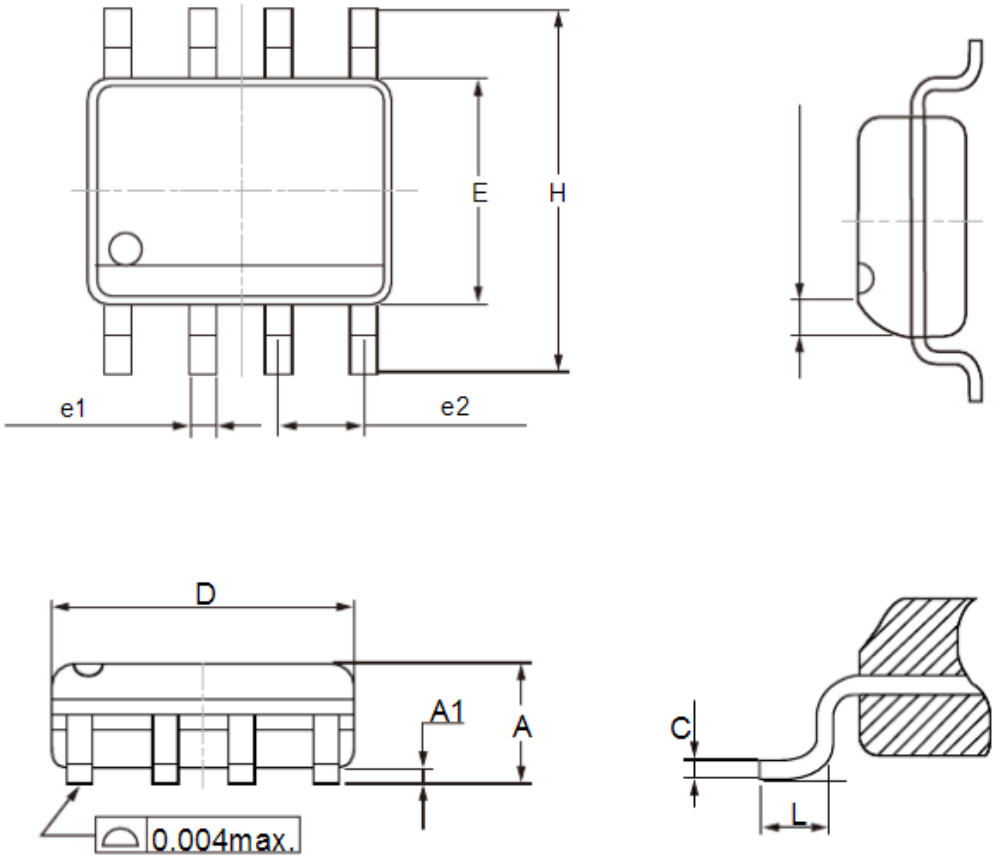
Table 8.1 NSA2300 Wafer Information

Wafer Size	8	inch
Die Size (Without S/L)	1230.43*1191.08	μm
Scribe Line	80	μm
Top Metal Thickness	0.99	μm
Pad Size	64*64	μm
Circuit Under Pad (CUP)	Yes	
Initial Point	Bottom left	

Table 8.2 NSA2300 Pad Location

Bare Die Pin No.	*PAD*	*X (μm)*	*Y (μm)*
1	VDD	58.125	1055.915
2	PSW	55.800	924.515
3	VINN	55.800	819.515
4	TEMP	55.800	714.515
5	VINP	55.800	404.515
6	VEXT	55.800	299.515
7	GND	55.000	130.660
8	SDO/ADDR	840.325	58.900
9	SCL	967.865	58.900
10	SDA/SDI/SDIO	1095.420	58.900
11	TP1	1142.555	215.035
12	VOUT	1145.210	360.845
13	TP2	1145.210	450.845
14	CSB	1067.995	1132.180
15	INT	939.020	1132.180
16	VDDIO	805.730	1132.180

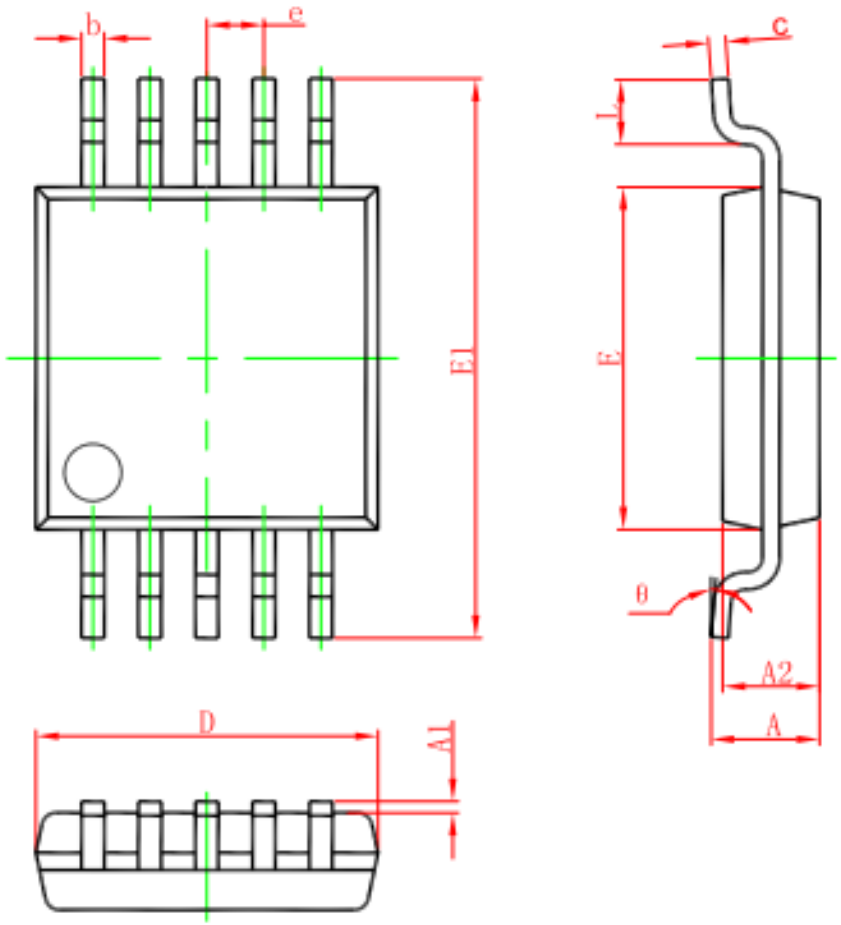
8.2. SOP8 Package



SYMBOLS	Millimeters			Inches		
	MIN.	Nom.	MAX.	MIN.	Nom.	MAX.
A	1.35	1.55	1.75	0.053	0.061	0.069
A1	0.10	0.17	0.25	0.004	0.007	0.010
C	0.18	0.22	0.25	0.007	0.009	0.010
D	4.80	4.90	5.00	0.189	0.193	0.197
E	3.80	3.90	4.00	0.150	0.154	0.158
H	5.80	6.00	6.20	0.229	0.236	0.244
e1	0.35	0.43	0.56	0.014	0.017	0.022
e2	1.27BSC			0.05BSC		
L	0.40	0.65	1.27	0.016	0.026	0.050

Figure 8.2 SOP8 Package Shape and Dimension

8.3. MSOP10 Package



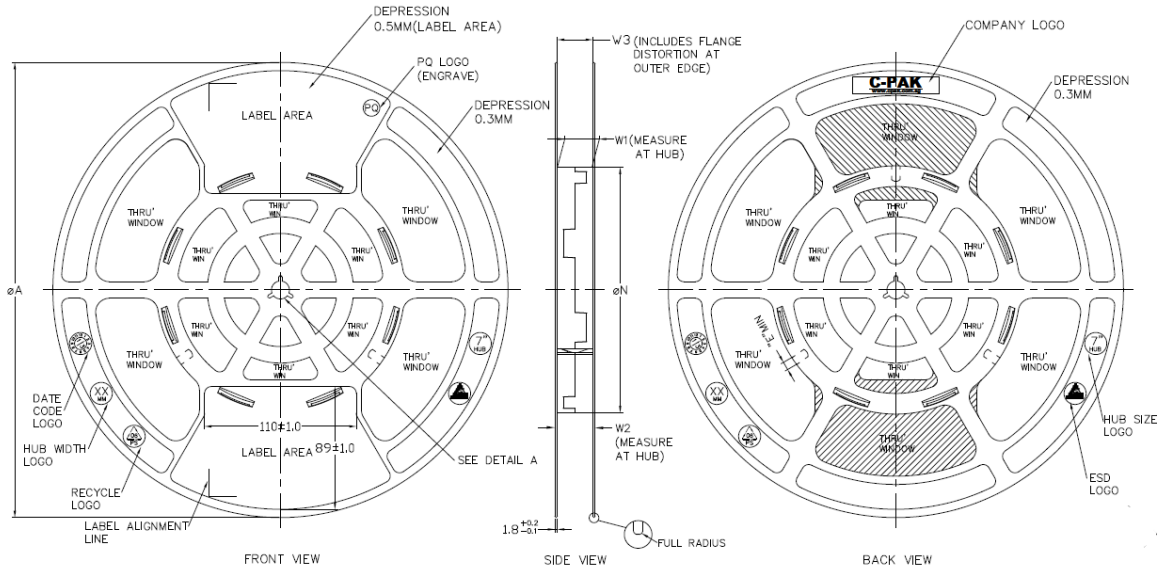
Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min	Max	Min	Max
A	0.820	1.100	0.032	0.043
A1	0.020	0.150	0.001	0.006
A2	0.750	0.950	0.030	0.037
b	0.180	0.280	0.007	0.011
c	0.090	0.230	0.004	0.009
D	2.900	3.100	0.114	0.122
e	0.50(BSC)		0.020(BSC)	
E	2.900	3.100	0.114	0.122
E1	4.750	5.050	0.187	0.199
L	0.400	0.800	0.016	0.031
θ	0°	6°	0°	6°

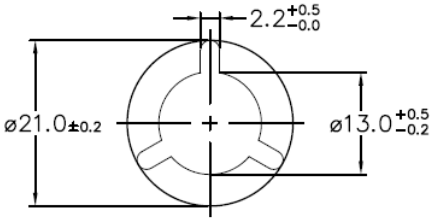
Figure 8.3 MSOP10 Package Shape and Dimension

9. Ordering Information

Part Number	Temperature	MSL	Package Type	SPQ
NSA2300_QBW	-40 to 125℃	-	Bare Die	KGD
NSA2300-QMOR	-40 to 125℃	3	MSOP10	3000
NSA2300-QSOR	-40 to 125℃	3	SOP8	4000

10. Tape and Reel Information





ARBOR HOLE
DETAIL A
SCALE : 3:1

PRODUCT SPECIFICATION						
TAPE WIDTH	øA ±2.0	øN ±2.0	W1	W2 (MAX)	W3	E (MIN)
08MM	330	178	8.4 +1.5 -0.0	14.4	SHALL ACCOMMODATE TAPE WIDTH WITHOUT INTERFERENCE	5.5
12MM	330	178	12.4 +2.0 -0.0	18.4		5.5
16MM	330	178	16.4 +2.0 -0.0	22.4		5.5
24MM	330	178	24.4 +2.0 -0.0	30.4		5.5
32MM	330	178	32.4 +2.0 -0.0	38.4		5.5

SURFACE RESISTIVITY			
LEGEND	SR RANGE	TYPE	COLOUR
A	BELOW 10^{12}	ANTISTATIC	ALL TYPES
B	10^{8} TO 10^{11}	STATIC DISSIPATIVE	BLACK ONLY
C	10^{5} & BELOW 10^{5}	CONDUCTIVE (GENERIC)	BLACK ONLY
E	10^{9} TO 10^{11}	ANTISTATIC (COATED)	ALL TYPES

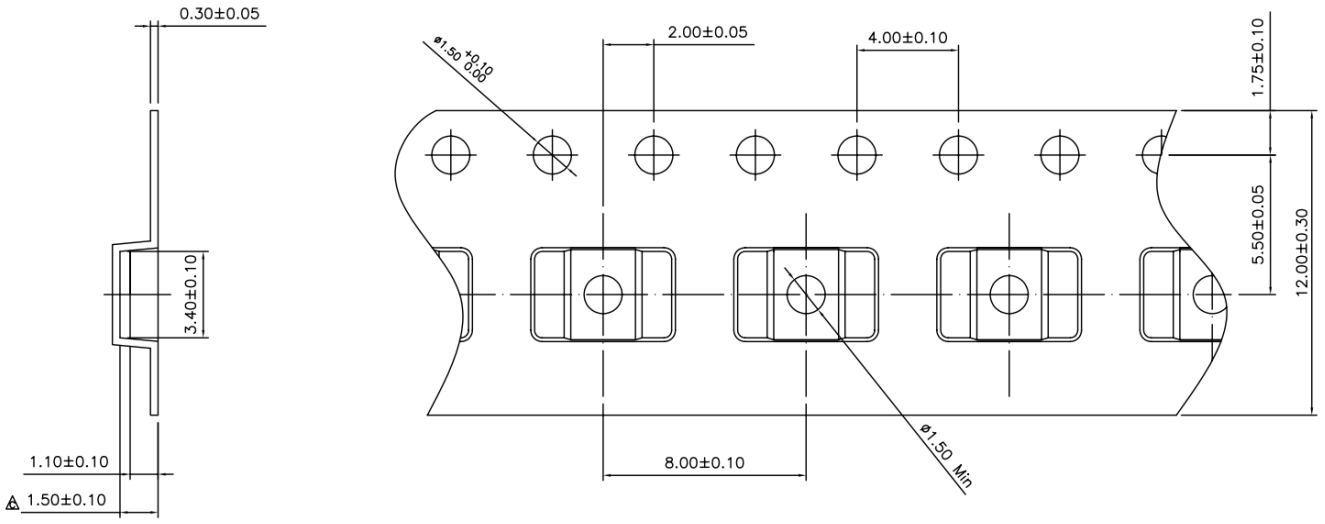


Figure 9.1 Tape and Reel Information of MSOP10

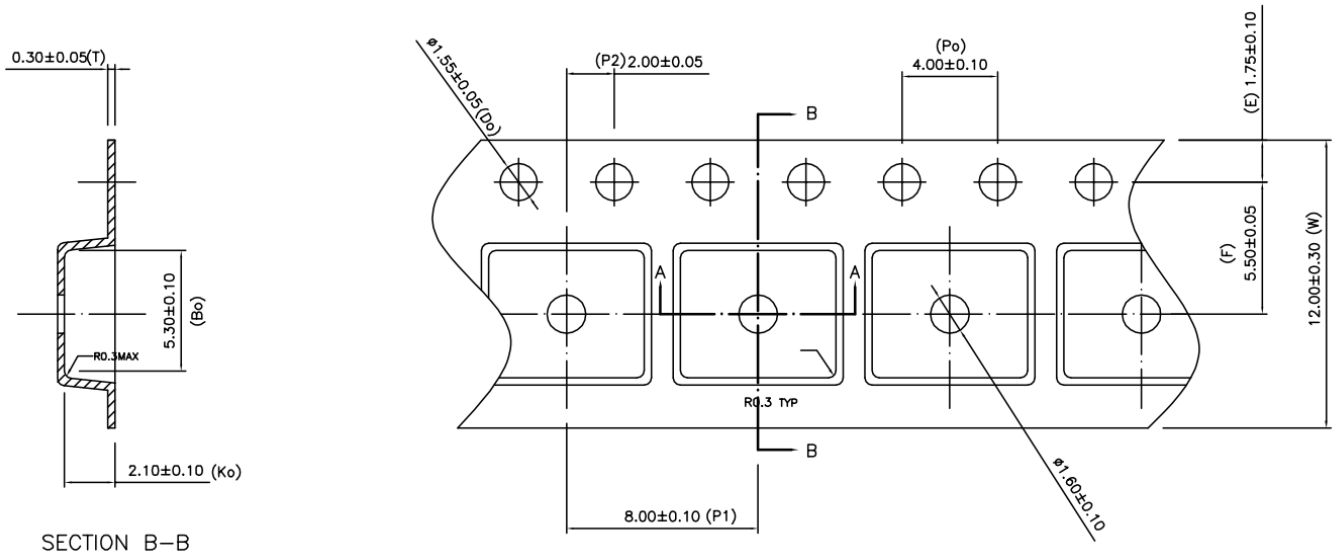
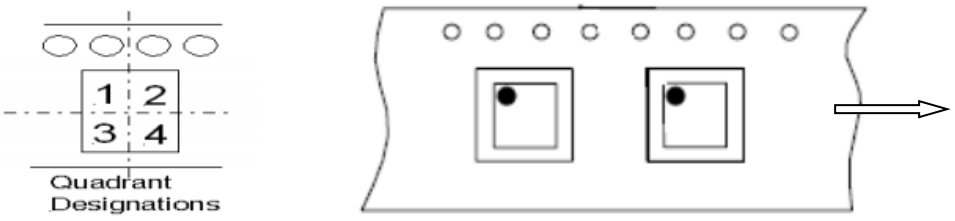


Figure 10.2 Tape and Reel Information of SOP8

Pin 1 is located at the first quadrant, as shown in the following figure.



11. Revision History

Revision	Description	Date
1.0	Initial version	2013/12/20
1.1	Add SOP-8 Package information	2013/3/5
1.2	Add application note for SOP8 package	2014/4/1
1.4	Correct the application Diagram	2014/06/03
1.5	Add gain=2X, 128X	2014/7/22
1.6	Update Diagnostic features, in both register map and block description Update bare die pad floor plan	2014/12/05
1.7	TEMP sensors select mode change	2015/6/26
1.8	Update ENOB data, typical application circuit	2015/8/24
1.9	Add MSOP10 Package information	2015/12/11
2.0	Update T_offset_trim	2016/10/10
2.1	Update order information	2020/6/3
2.2	Add tape/reel information	2022/5/20
2.3	Adjust ESD form 4kV to 2kV,updata to new template	2023/12/13

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