

Silicon N-Channel Power MOSFET

Description

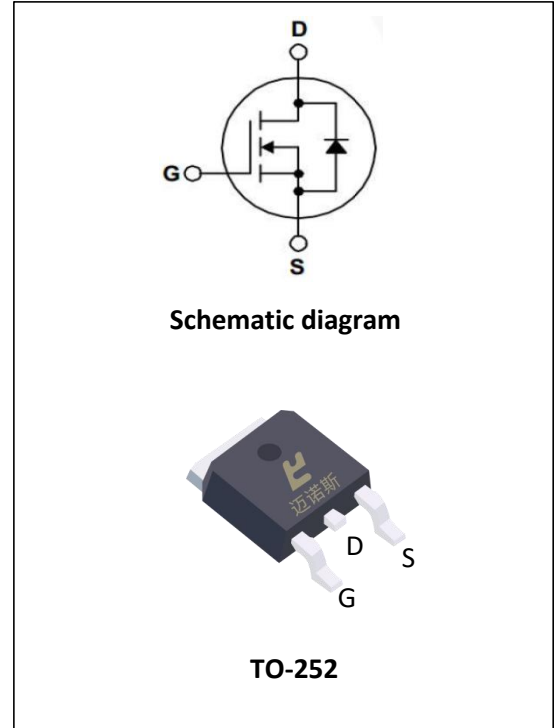
The IRLR2905TRPBF uses advanced trench technology to provide excellent $R_{DS(ON)}$, low gate charge. It can be used in a wide variety of applications.

General Features

- ① $V_{DS}=60V, I_D=50A$
 $R_{DS(ON)} < 18m\Omega @ V_{GS}=10V$
- ② Special process technology for high ESD capability
- ③ High density cell design for ultra low R_{dson}
- ④ Fully characterized avalanche voltage and current
- ⑤ Good stability and uniformity with high EAS
- ⑥ Excellent package for good heat dissipation

Application

- ① Power switching application
- ② Hard switched and High frequency circuits
- ③ Uninterruptible power supply



Package Marking And Ordering Information

Ordering Codes	Package	Product Code	Packing
IRLR2905TRPBF	TO-252	LR2905	Reel

ABSOLUTE RATINGS (at $T_C=25^\circ C$ unless otherwise specified)

Symbol	Parameter	Value	Units
V_{DS}	Drain-Source Voltage	60	V
V_{GS}	Gate-Source Voltage	± 20	V
I_D	Drain Current-Continuous	50	A
I_{DM}	Drain Current-Pulsed (Note 1)	200	A
P_D	Maximum Power Dissipation($T_C=25^\circ C$)	87	W
E_{AS}	Single pulse avalanche energy (Note 2)	120	mJ
T_J, T_{STG}	Operating Junction and Storage Temperature Range	-55 To 175	$^\circ C$

Thermal Characteristic

Symbol	Parameter	Typ	Units
$R_{\theta JC}$	Junction-to-Case	1.72	$^\circ C/W$

Electrical Characteristics (Tc=25 °C unless otherwise noted)

Symbol	Parameter	Condition	Min	Typ	Max	Units
Off Characteristics						
B _{VDS}	Drain-Source Breakdown Voltage	V _{GS} =0V I _D =250μA	60	--	--	V
I _{DSS}	Zero Gate Voltage Drain Current	V _{DS} =60V, V _{GS} =0V	--	--	1	μA
I _{GSS}	Gate-Body Leakage Current	V _{GS} =±20V, V _{DS} =0V	--	--	±100	nA
On Characteristics						
V _{GS(th)}	Gate Threshold Voltage	V _{DS} =V _{GS} , I _D =250μA	0.8	1.2	1.5	V
R _{DS(ON)}	Drain-Source On-State Resistance ^(Note 3)	V _{GS} =10V, I _D =25A	--	15	18	mΩ
G _{FS}	Forward Transconductance	V _{DS} =25V, I _D =25A	--	25	--	S
Dynamic Characteristics						
C _{ISS}	Input Capacitance	V _{DS} =25V, V _{GS} =0V, F=1.0MHz	--	910	--	pF
C _{OSS}	Output Capacitance		--	100	--	pF
C _{RSS}	Reverse Transfer Capacitance		--	30	--	pF
Switching Characteristics ^(Note 4)						
t _{d(on)}	Turn-on Delay Time	V _{DD} =30V, I _D =20A, V _{GS} =10V, R _{GEN} =5Ω	--	26	--	nS
t _r	Turn-on Rise Time		--	6	--	nS
t _{d(off)}	Turn-Off Delay Time		--	52	--	nS
t _f	Turn-Off Fall Time		--	7	--	nS
Q _g	Total Gate Charge	V _{DS} =30V, I _D =50A V _{GS} =10V	--	31	--	nC
Q _{gs}	Gate-Source Charge		--	9	--	nC
Q _{gd}	Gate-Drain Charge		--	5	--	nC
Drain-Source Diode Characteristics						
V _{SD}	Diode Forward Voltage(Note 3)	V _{GS} =0V, I _S =50A	--	--	1.2	V

Notes:

- 1.Repetitive Rating: Pulse width limited by maximum junction temperature.
- 2.EAS condition :T_J=25 °C, V_{DD}=30V, V_G=10V, L=0.5mH, R_g=25Ω
- 3.Pulse Test: Pulse Width ≤ 300μs, Duty Cycle ≤ 2%.
- 4.Guaranteed by design, not subject to production.

Characteristics Curves

Figure 1 Output Characteristics

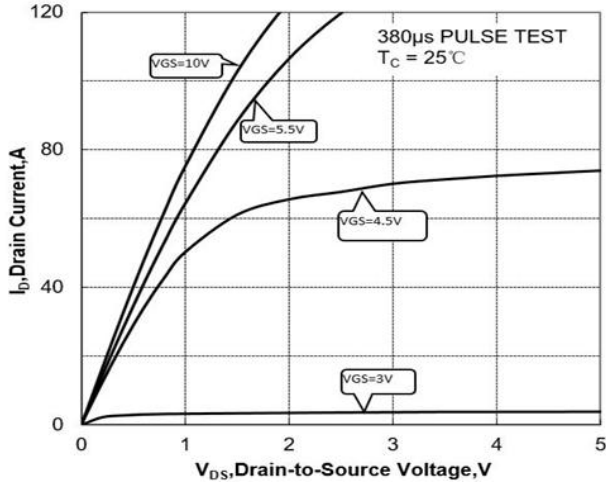


Figure 2 Transfer Characteristics

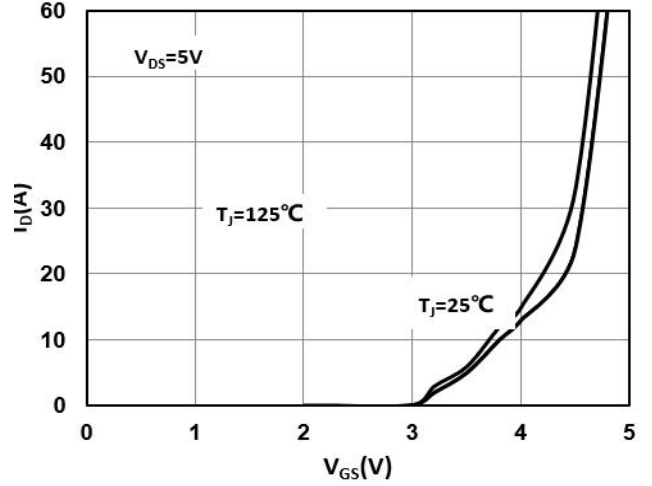


Figure 3 On-Resistance vs. ID and VGS

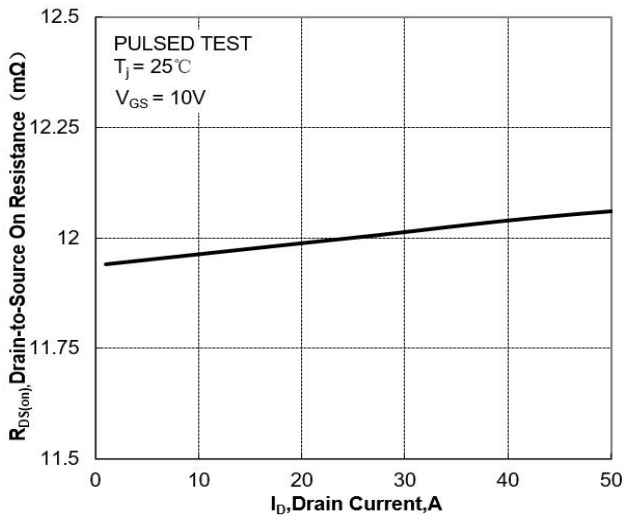


Figure 4 On-Resistance vs. Junction Temperature

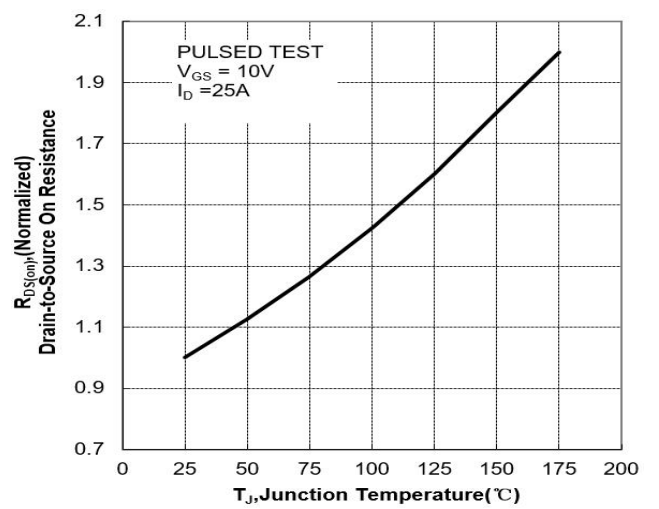


Figure 5 On-Resistance vs. VGS

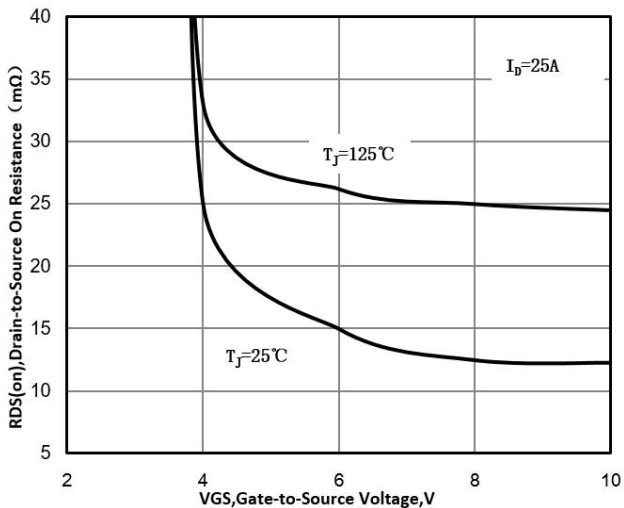


Figure 6 Body Diode Forward Voltage

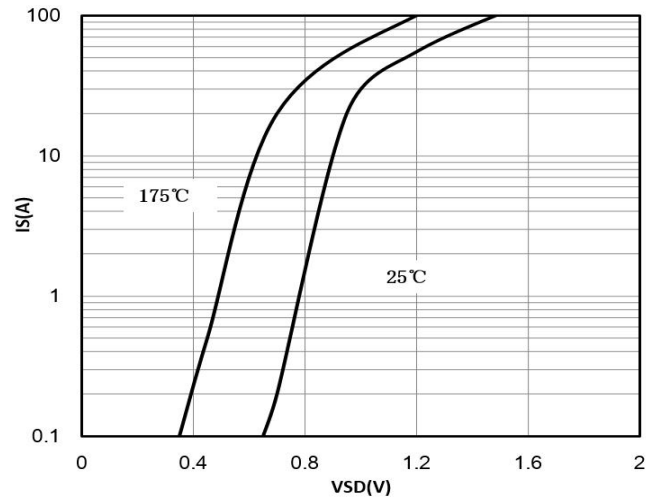


Figure 7 Gate-Charge Characteristics

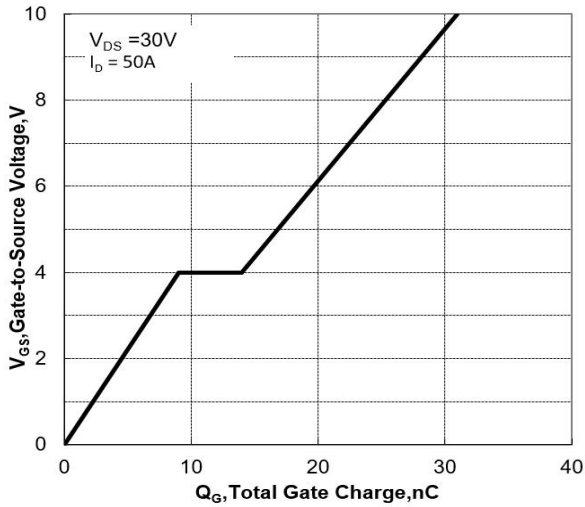


Figure 8 Capacitance Characteristics

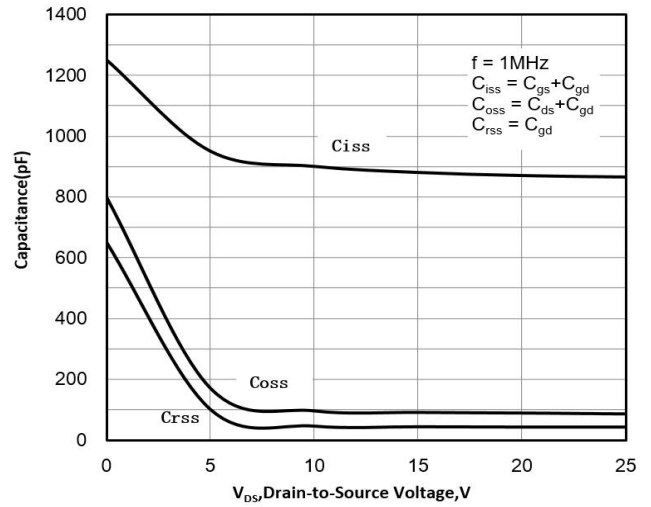


Figure 9 Maximum Forward Biased Safe Operation Area

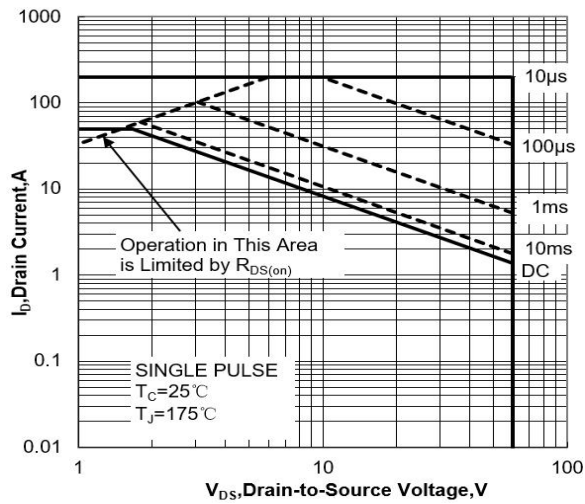


Figure 10 Single Pulse Power Rating Junction-to-Ambient

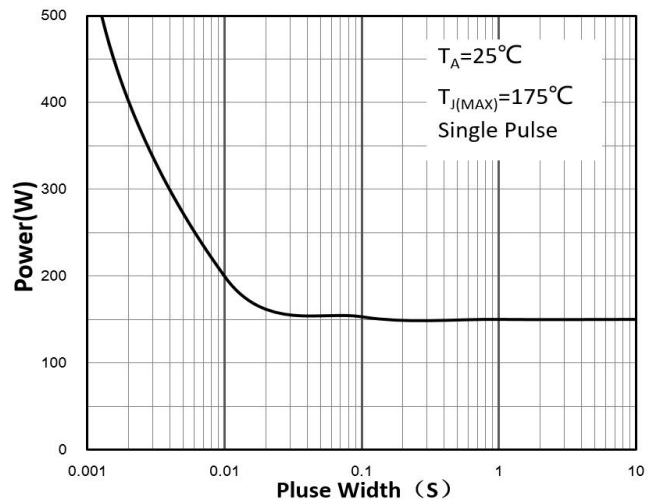
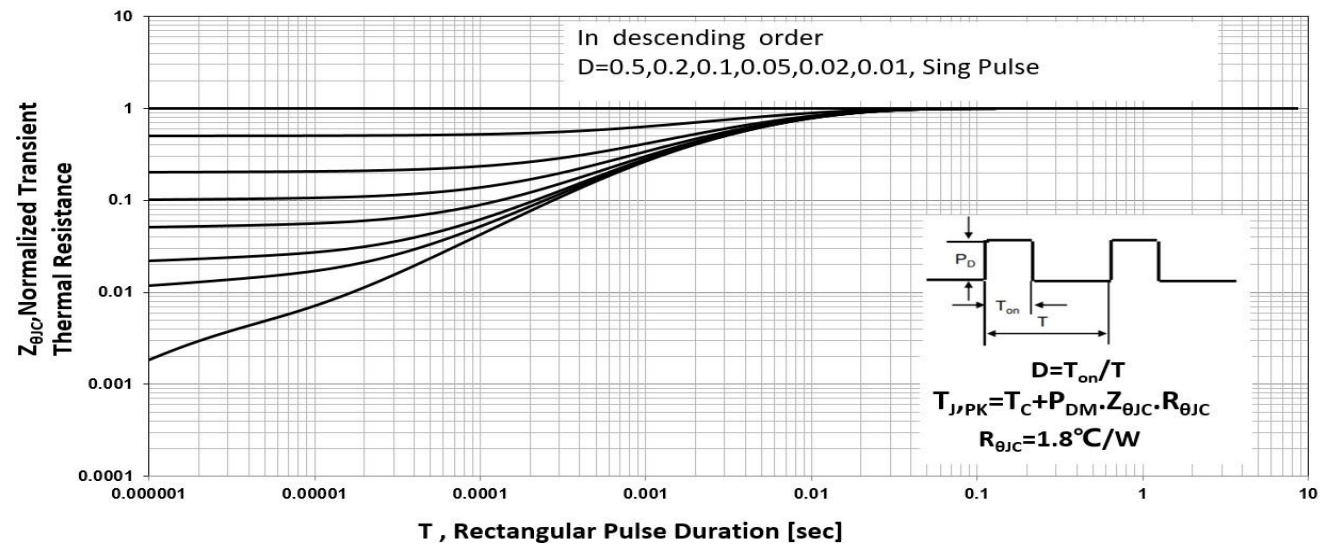
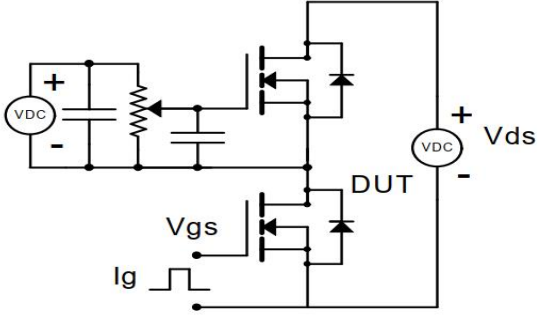
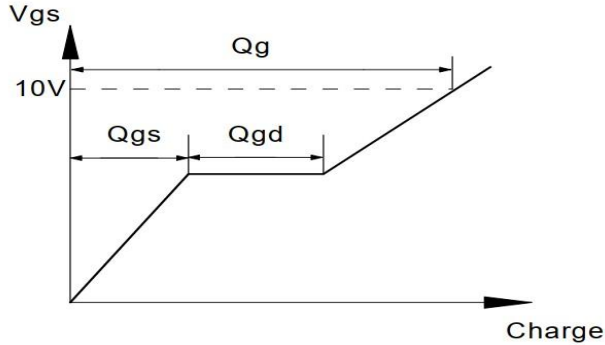
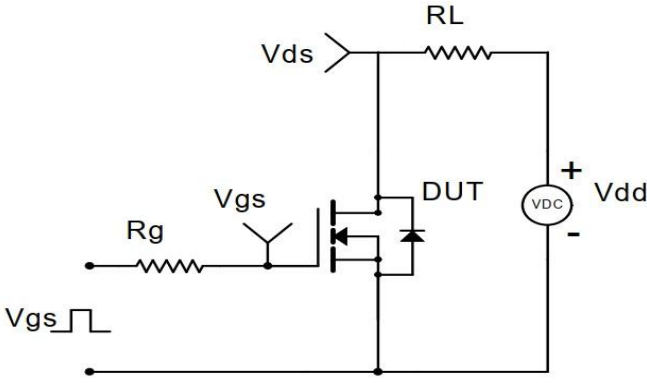
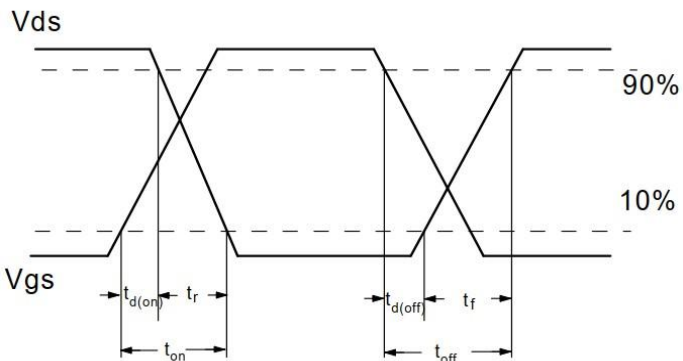
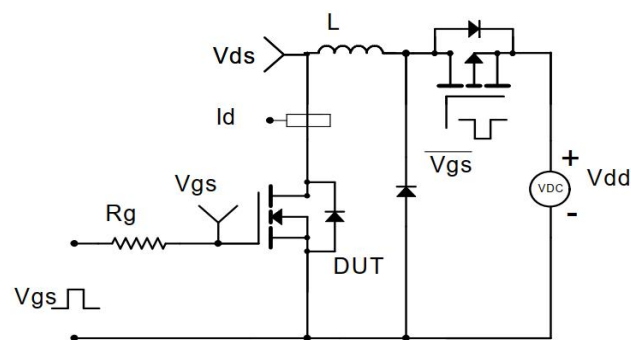
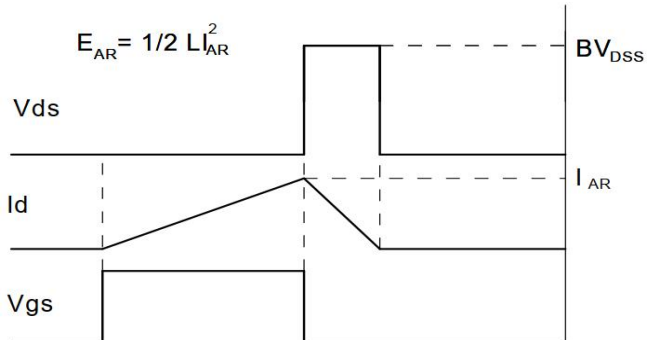
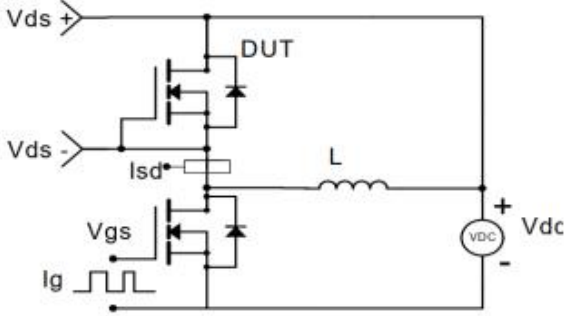
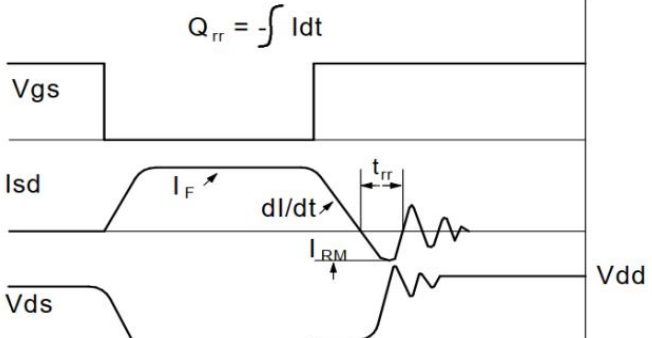


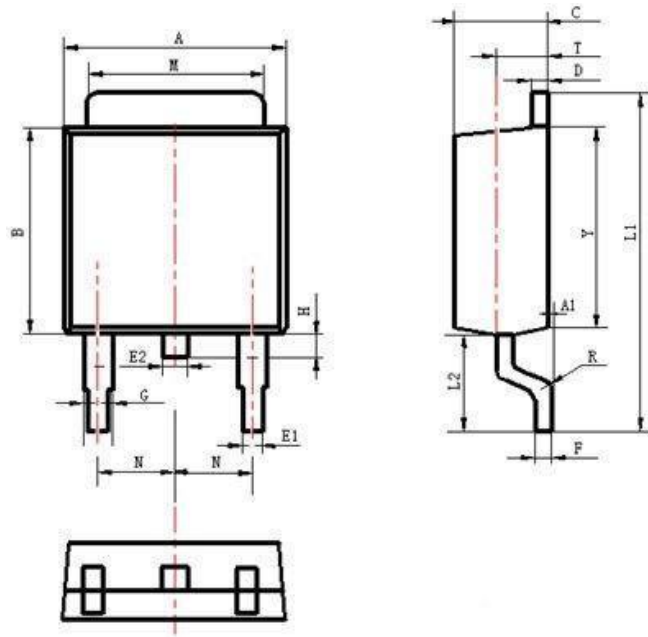
Figure 11 Normalized Maximum Transient Thermal Impedance



Test Circuit and Waveform

Gate Charge Test Circuit	Gate Charge Test Waveform
 <p>The diagram shows a MOSFET circuit for gate charge testing. A VDC source is connected to the drain through a resistor. The gate is driven by a pulse source I_g through a resistor. The MOSFET is connected to a load resistor and a diode. The drain-source voltage is labeled V_{ds} and the gate-source voltage is V_{gs}. The device under test is labeled DUT.</p>	 <p>The waveform shows V_{gs} on the y-axis and Charge on the x-axis. The gate voltage rises linearly to 10V, stays constant for a duration Q_{gs}, falls linearly for a duration Q_{gd}, and then rises again. The total gate charge is labeled Q_g.</p>
Resistive Switching Test Circuit	Resistive Switching Test Waveforms
 <p>The diagram shows a MOSFET switching a load resistor R_L. The gate is driven by a pulse source V_{gs} through a resistor R_g. The drain is connected to a VDC source V_{dd} through R_L. The drain-source voltage is V_{ds}. The device under test is labeled DUT.</p>	 <p>The waveforms show V_{ds} and V_{gs} over time. V_{gs} is a square wave. V_{ds} shows a trapezoidal switching transient. Key timing parameters are labeled: $t_{d(on)}$, t_r, t_{on}, $t_{d(off)}$, t_f, and t_{off}. The voltage levels are marked at 90% and 10%.</p>
Unclamped Inductive Switching (UIS) Test Circuit	Unclamped Inductive Switching (UIS) Test Waveforms
 <p>The diagram shows a MOSFET switching an inductor L. The gate is driven by a pulse source V_{gs} through a resistor R_g. The drain is connected to a VDC source V_{dd} through L. The drain-source voltage is V_{ds} and the drain current is I_d. The device under test is labeled DUT.</p>	 <p>The waveforms show V_{ds}, I_d, and V_{gs} over time. V_{gs} is a square wave. I_d shows a linear ramp up and down. V_{ds} shows a trapezoidal switching transient. The equation $E_{AR} = 1/2 L I_{AR}^2$ is shown. The peak drain-source voltage is BV_{DSS} and the average current is I_{AR}.</p>
Diode Recovery Test Circuit	Diode Recovery Test Waveforms
 <p>The diagram shows a MOSFET switching an inductor L. The gate is driven by a pulse source I_g through a resistor. The drain is connected to a VDC source V_{dc} through L. The drain-source voltage is V_{ds} and the drain current is I_{sd}. The device under test is labeled DUT.</p>	 <p>The waveforms show V_{gs}, I_{sd}, and V_{ds} over time. V_{gs} is a square wave. I_{sd} shows a trapezoidal current pulse with peak current I_F and di/dt slope. V_{ds} shows a trapezoidal voltage pulse with peak voltage V_{dd} and di/dt slope. The reverse recovery time t_{rr} is indicated. The equation $Q_{rr} = -\int I_{sd} dt$ is shown.</p>

Package Description



Items	Values(mm)	
	MIN	MAX
A	6.30	6.90
A1	0	0.13
B	5.70	6.30
C	2.10	2.50
D	0.30	0.60
E1	0.60	0.90
E2	0.70	1.00
F	0.30	0.60
G	0.70	1.20
L1	9.60	10.50
L2	2.70	3.10
H	0.60	1.00
M	5.10	5.50
N	2.09	2.49
R	0.3	
T	1.40	1.60
Y	5.10	6.30

TO-252 Package

NOTE:

1. Exceeding the maximum ratings of the device in performance may cause damage to the device, even the permanent failure, which may affect the dependability of the machine. Please do not exceed the absolute maximum ratings of the device when circuit designing.
2. When installing the heat sink, please pay attention to the torsional moment and the smoothness of the heat sink.
3. MOSFETs is the device which is sensitive to the static electricity, it is necessary to protect the device from being damaged by the static electricity when using it.
4. Shenzhen Minos reserves the right to make changes in this specification sheet and is subject to change without prior notice.

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