

80V N-Channel Power MOSFE

Description

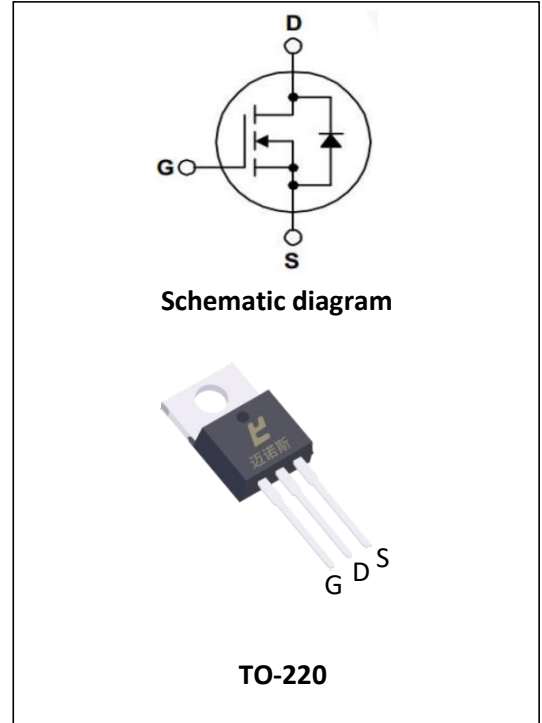
The IRFB3207PBF uses advanced trench technology and design To provide Excellent $R_{DS(ON)}$. It can be used in a wide variety of applications.

General Features

- ① $V_{DS}=80V$, $R_{dson}<4m\Omega$ @ $V_{GS}=10V$, $I_D=200A$ (Typ:3m Ω)
- ② Special process technology for high ESD capability
- ③ High density cell design for ultra low R_{dson}
- ④ Fully characterized avalanche voltage and current
- ⑤ Good stability and uniformity with high EAS
- ⑥ Excellent package for good heat dissipation

Application

- ① Power switching application
- ② Hard switched and High frequency circuits
- ③ Uninterruptible power supply



Package Marking And Ordering Information:

Ordering Codes	Package	Product Code	Packing
IRFB3207PBF	TO-220	IRFB3207PBF	Tube

Absolute maximum ratings (TA = 25°C unless otherwise noted)

Symbol	Parameter	Value	Units
V_{DS}	Drain-Source Voltage	80	V
V_{GS}	Gate-Source Voltage	± 20	V
I_D	Drain Current-Continuous	200	A
I_{DM}	Drain Current-Pulsed ^(Note 1)	800	A
P_D	Maximum Power Dissipation($T_c=25^\circ C$)	270	W
E_{AS}	Single pulse avalanche energy ^(Note 2)	1600	mJ
T_J, T_{STG}	Operating Junction and Storage Temperature Range	-55 To 175	$^\circ C$

Thermal characteristics

Symbol	Parameter	Typ	Units
$R_{\theta JC}$	Junction-to-Case	0.41	$^\circ C/W$

Electrical Characteristics(at $T_c = 25^\circ\text{C}$, unless otherwise specified)

Parameter	Symbol	Condition	Min	Typ	Max	Units
Off Characteristics						
$B_{V_{DS}}$	Drain-Source Breakdown Voltage	$V_{GS}=0V, I_D=250\mu A$	80	--	--	V
I_{DSS}	Zero Gate Voltage Drain Current	$V_{DS}=80V, V_{GS}=0V$	--	--	1	μA
I_{GSS}	Gate-Body Leakage Current	$V_{GS}=\pm 20V, V_{DS}=0V$	--	--	± 100	nA
On Characteristics						
$V_{GS(th)}$	Gate Threshold Voltage	$V_{DS}=V_{GS}, I_D=250\mu A$	2	3	4	V
$R_{DS(ON)}$	Drain-Source On-State Resistance ^(Note 3)	$V_{GS}=10V, I_D=50A$	--	3	4	m Ω
G_{FS}	Forward Transconductance	$V_{DS}=5V, I_D=15A$	--	17	--	S
Dynamic Characteristics						
C_{iss}	Input Capacitance	$V_{DS}=25V, V_{GS}=0V,$ $F=1.0MHz$	--	13200	--	pF
C_{oss}	Output Capacitance		--	950	--	pF
C_{rss}	Reverse Transfer Capacitance		--	810	--	pF
Switching Characteristics ^(Note 4)						
$t_{d(on)}$	Turn-on Delay Time	$V_{DD}=40V, I_D=40A,$ $V_{GS}=10V, R_{GEN}=3\Omega$	--	26	--	nS
t_r	Turn-on Rise Time		--	20	--	nS
$t_{d(off)}$	Turn-Off Delay Time		--	50	--	nS
t_f	Turn-Off Fall Time		--	18	--	nS
Q_g	Total Gate Charge	$V_{DS}=64V, I_D=80A, V_{GS}=10V$	--	257	--	nC
Q_{gs}	Gate-Source Charge		--	76	--	nC
Q_{gd}	Gate-Drain Charge		--	80	--	nC
Drain-Source Diode Characteristics						
V_{SD}	Diode Forward Voltage(Note 3)	$V_{GS}=0V, I_S=80A$	--	--	1.2	V

Notes:

1. Repetitive Rating: Pulse width limited by maximum junction temperature.
2. EAS condition : $T_j=25^\circ\text{C}, V_{DD}=50V, V_G=10V, L=0.5mH, R_g=1\Omega$
3. Pulse Test: Pulse Width $\leq 300\mu s$, Duty Cycle $\leq 2\%$.
4. Guaranteed by design, not subject to production.

Characteristics Curves

Figure 1 Output Characteristics

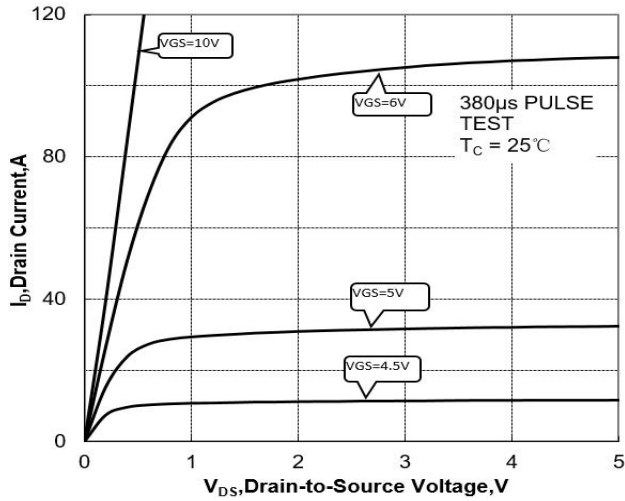


Figure 2 Transfer Characteristics

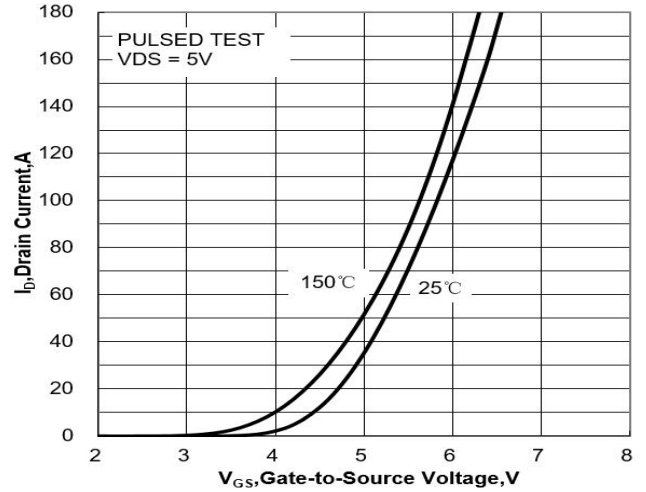


Figure 3 On-Resistance vs. ID and VGS

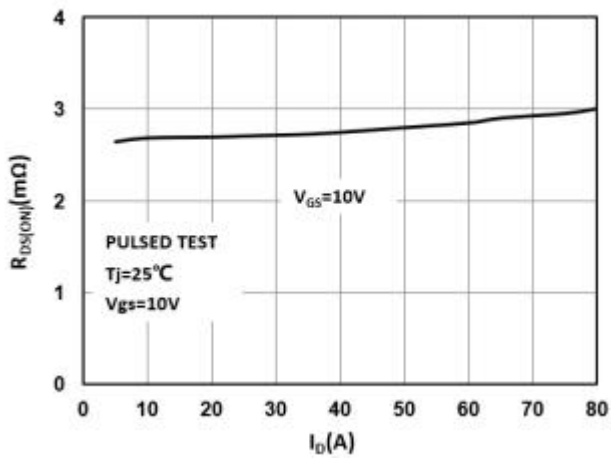


Figure 4 On-Resistance vs. Junction Temperature

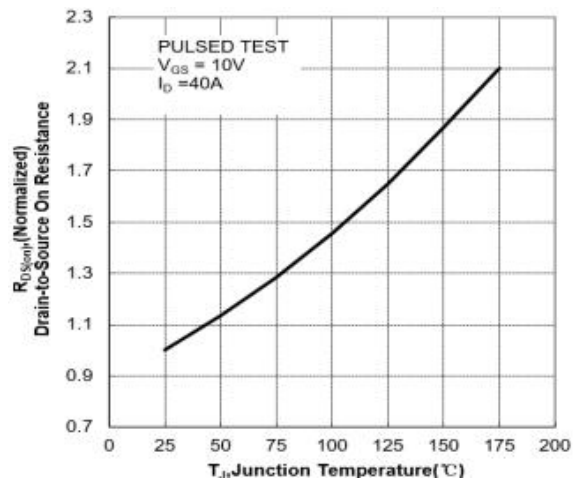


Figure 5 On-Resistance vs. VGS

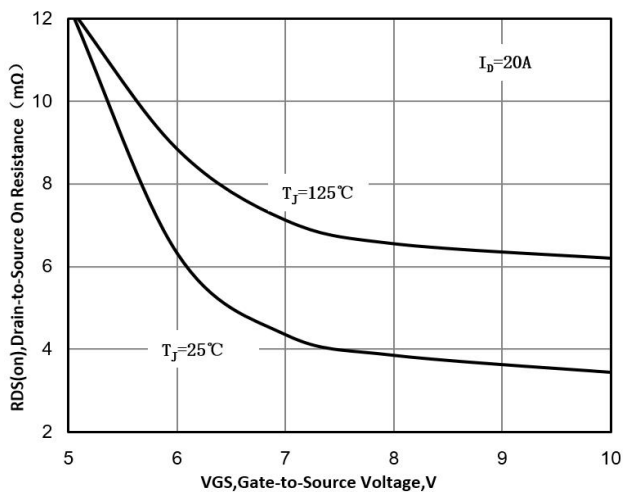


Figure 6 Body Diode Forward Voltage

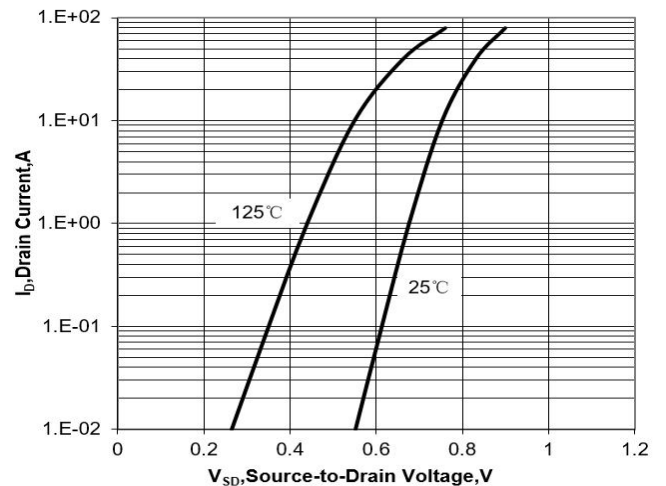


Figure 7 Gate-Charge Characteristics

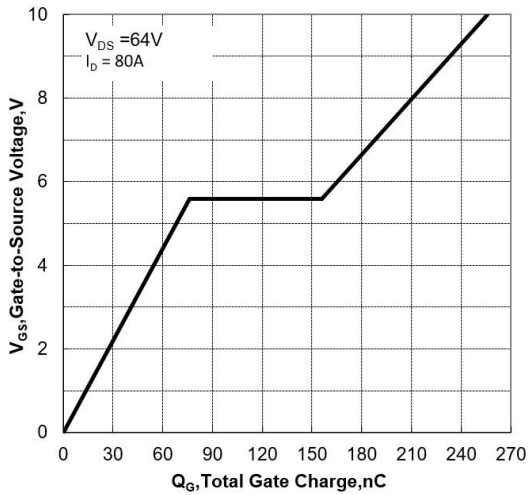


Figure 8 Capacitance Characteristics

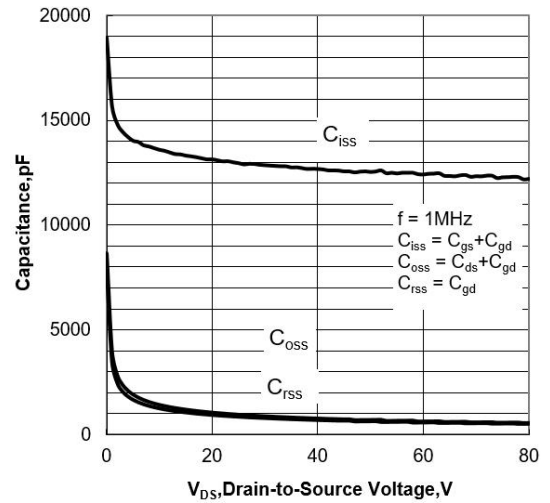


Figure 9 Maximum Forward Biased Safe Operation Area

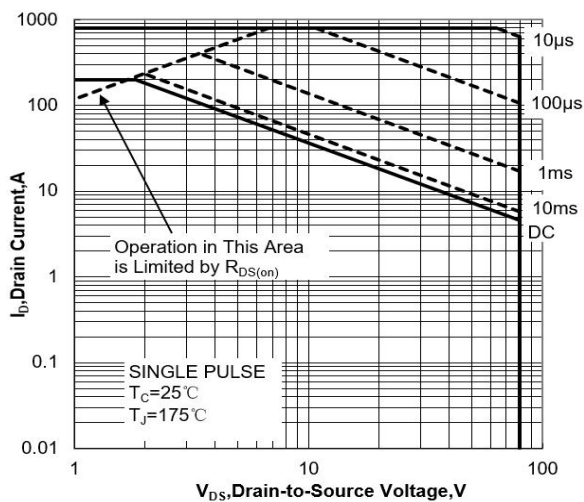


Figure 10 Single Pulse Power Rating Junction-to-Ambient

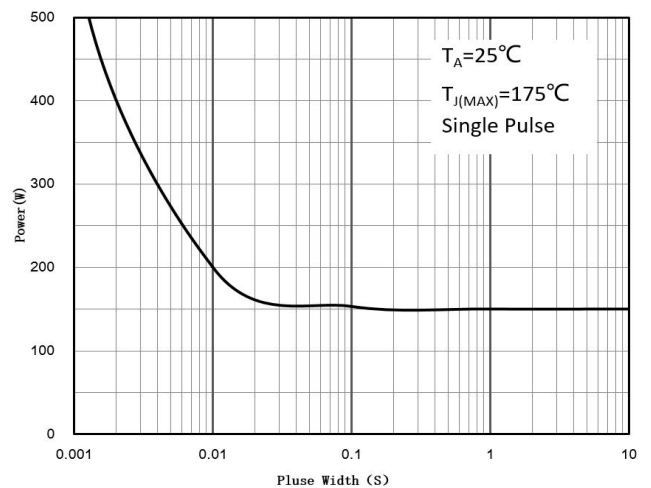
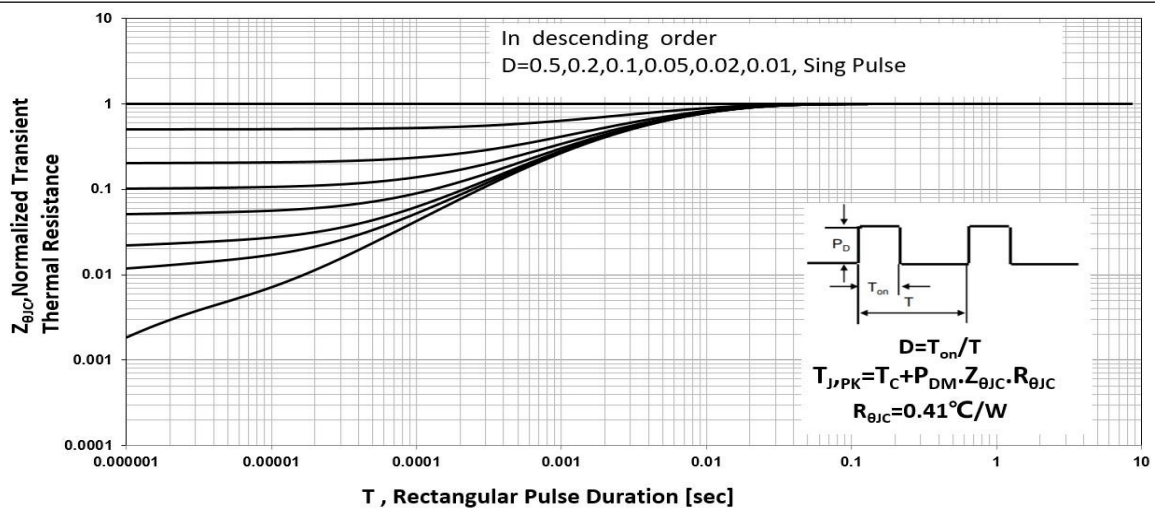
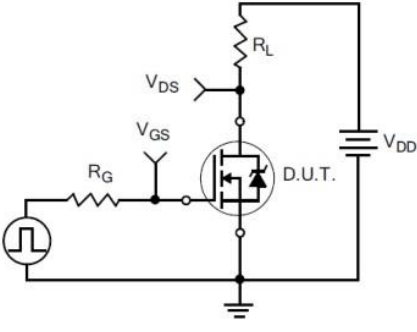
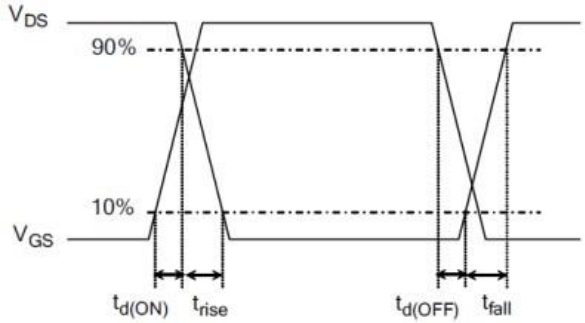
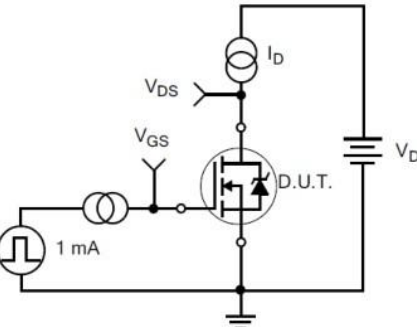
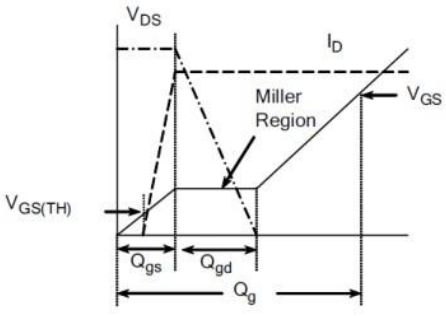
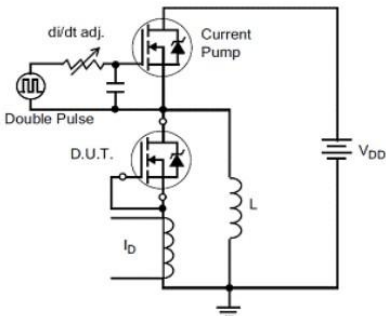
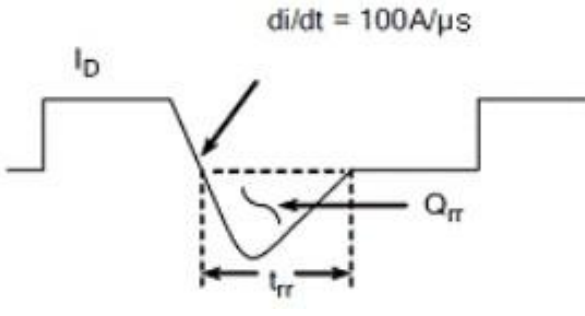
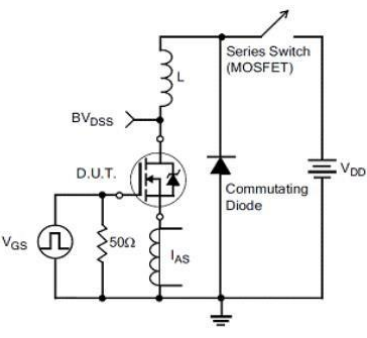
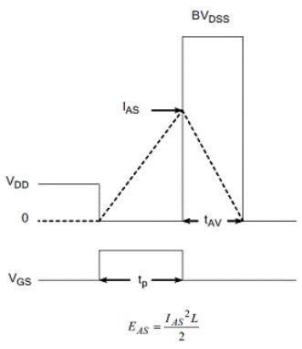


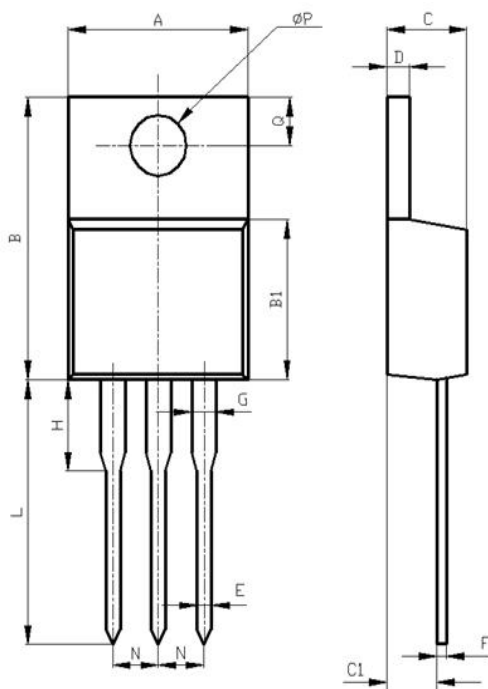
Figure 11 Normalized Maximum Transient Thermal Impedance



Test Circuit and Waveform

<p>Figure 12. Resistive Switching Test Circuit</p>	<p>Figure 13. Resistive Switching Waveforms</p>
 <p>The diagram shows a MOSFET (D.U.T.) in a common-source configuration. The drain is connected to a load resistor R_L and a supply V_{DD}. The gate is connected to a gate resistor R_G and a pulse source. The drain voltage is V_{DS} and the gate voltage is V_{GS}.</p>	 <p>The diagram shows the relationship between V_{DS} and V_{GS} during switching. V_{GS} transitions from 0V to a pulse and back to 0V. V_{DS} transitions from 0V to V_{DD} and back to 0V. Key parameters are marked: $t_{d(ON)}$ (delay to turn on), t_{rise} (rise time), $t_{d(OFF)}$ (delay to turn off), and t_{fall} (fall time). The 90% and 10% voltage levels are indicated for both signals.</p>
<p>Figure 14. Gate Charge Test Circuit</p>	<p>Figure 15. Gate Charge Waveforms</p>
 <p>The diagram shows a MOSFET (D.U.T.) with a 1 mA current source connected to the gate. The drain is connected to a load resistor R_L and a supply V_{DD}. The drain current is I_D. The gate voltage is V_{GS} and the drain voltage is V_{DS}.</p>	 <p>The diagram shows the relationship between V_{DS} and V_{GS} during gate charging. V_{GS} rises from 0V to $V_{GS(TH)}$ and then to a plateau. V_{DS} rises from 0V to V_{DD} during the Miller region. Key parameters are marked: Q_{gs} (gate-source charge), Q_{gd} (gate-drain charge), and Q_g (total gate charge). The Miller region is explicitly labeled.</p>
<p>Figure 16. Diode Reverse Recovery Test Circuit</p>	<p>Figure 17. Diode Reverse Recovery Waveform</p>
 <p>The diagram shows a MOSFET (D.U.T.) in a common-source configuration. The drain is connected to a current pump and a load inductor L. The gate is connected to a double pulse source. The drain current is I_D and the drain voltage is V_{DS}. The diode reverse recovery time t_{rr} is indicated.</p>	 <p>The diagram shows the diode reverse recovery waveform. The current I_D transitions from a positive value to a negative value. The reverse recovery time t_{rr} is the time interval from the start of the reverse current to the point where the current reaches zero. The charge Q_{rr} is the area under the reverse current curve. The di/dt rate is specified as $di/dt = 100A/\mu s$.</p>
<p>Figure 18. Unclamped Inductive Switching Test Circuit</p>	<p>Figure 19. Unclamped Inductive Switching Waveform</p>
 <p>The diagram shows a MOSFET (D.U.T.) in a common-source configuration. The drain is connected to a series switch (MOSFET) and a load inductor L. The gate is connected to a pulse source V_{GS} and a 50Ω resistor. The drain current is I_{AS}. The diode is a commutating diode. The drain voltage is V_{DS} and the supply is V_{DD}. The avalanche voltage BV_{DSS} and avalanche current I_{AS} are indicated.</p>	 <p>The diagram shows the unclamped inductive switching waveform. The drain voltage V_{DS} transitions from V_{DD} to 0V and then to a negative voltage $-V_{AS}$ during the avalanche phase. The avalanche current I_{AS} is constant during this phase. The pulse width is t_p. The equation $E_{AS} = \frac{I_{AS}^2 L}{2}$ is provided.</p>

Package Description



Symbol	Values(mm)	
	MIN	MAX
A	9.60	10.6
B	15.0	16.0
B1	8.90	9.50
C	4.30	4.80
C1	2.30	3.10
D	1.20	1.40
E	0.70	0.90
F	0.30	0.60
G	1.17	1.37
H	2.70	3.80
L	12.6	14.8
N	2.34	2.74
Q	2.40	3.00
ϕP	3.50	3.90

TO-220 Package



迈诺斯科技

IRFB3207PBF

NOTE:

1. Exceeding the maximum ratings of the device in performance may cause damage to the device, even the permanent failure, which may affect the dependability of the machine. Please do not exceed the absolute maximum ratings of the device when circuit designing.
2. When installing the heat sink, please pay attention to the torsional moment and the smoothness of the heat sink.
3. MOSFETs is the device which is sensitive to the static electricity, it is necessary to protect the device from being damaged by the static electricity when using it.
4. Shenzhen Minos reserves the right to make changes in this specification sheet and is subject to change without prior notice.

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