

Dual N-Channel 20V(D-S) Enhancement Mode Mosfet , ESD Protection

GENERAL DESCRIPTION

The ME6980ED is the Dual N-Channel logic enhancement mode power field effect transistors are produced using high cell density, DMOS trench technology. This high density process is especially tailored to minimize on-state resistance. These devices are particularly suited for low voltage application such as cellular phone and notebook computer power management and other battery powered circuits where high-side switching , and low in-line power loss are needed in a very small outline surface mount package.

FEATURES

- $R_{DS(ON)} \leq 14.5m\Omega @ V_{GS}=4.5V$
- $R_{DS(ON)} \leq 15m\Omega @ V_{GS}=4.0V$
- $R_{DS(ON)} \leq 17m\Omega @ V_{GS}=3.1V$
- $R_{DS(ON)} \leq 20m\Omega @ V_{GS}=2.5V$
- Super high density cell design for extremely low $R_{DS(ON)}$
- Exceptional on-resistance and maximum DC current capability

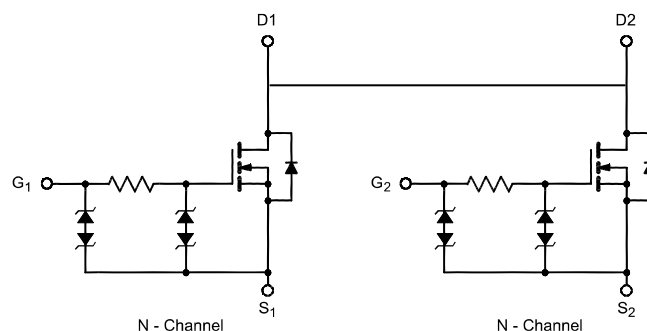
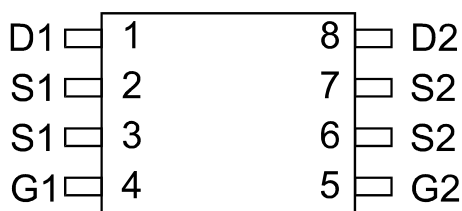
APPLICATIONS

- Power Management in Note book
- Portable Equipment
- Battery Powered System
- Load Switch
- DSC

PIN CONFIGURATION

(TSSOP-8)

Top View



*Typical value by design

Ordering Information: ME6980ED (Pb-free)

ME6980ED-G (Green product-Halogen free)

Absolute Maximum Ratings ($T_A=25^\circ C$ Unless Otherwise Noted)

Parameter		Symbol	Maximum Ratings	Unit
Drain-Source Voltage		V_{DS}	20	V
Gate-Source Voltage		V_{GS}	± 12	V
Continuous Drain Current	$T_A=25^\circ C$	I_D	7.3	A
	$T_A=70^\circ C$		5.9	
Pulsed Drain Current		I_{DM}	29	A
Maximum Power Dissipation	$T_A=25^\circ C$	P_D	1.3	W
	$T_A=70^\circ C$		0.8	
Junction and Storage Temperature Range		T_J, T_{stg}	-55 to 150	$^\circ C$
Thermal Resistance-Junction to Ambient*		$R_{\theta JA}$	100	$^\circ C/W$

* The device mounted on $1in^2$ FR4 board with 2 oz copper

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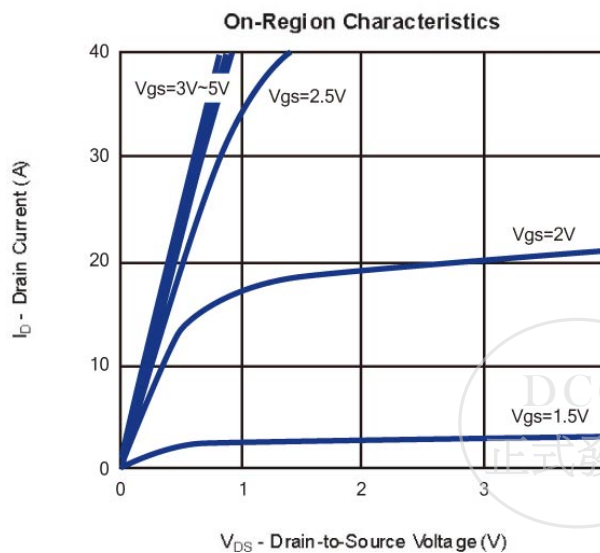
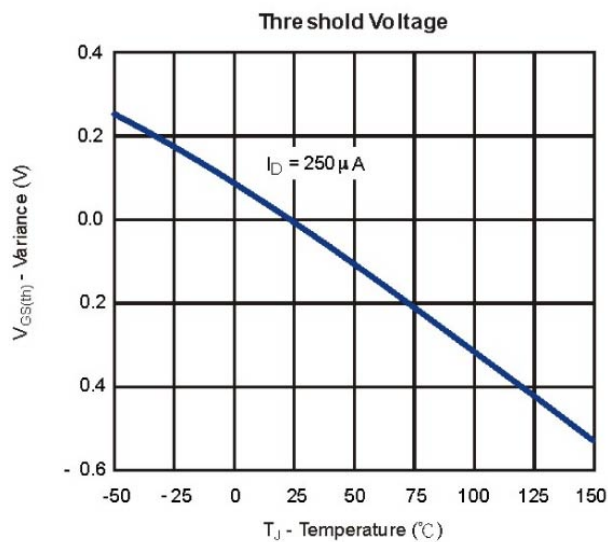
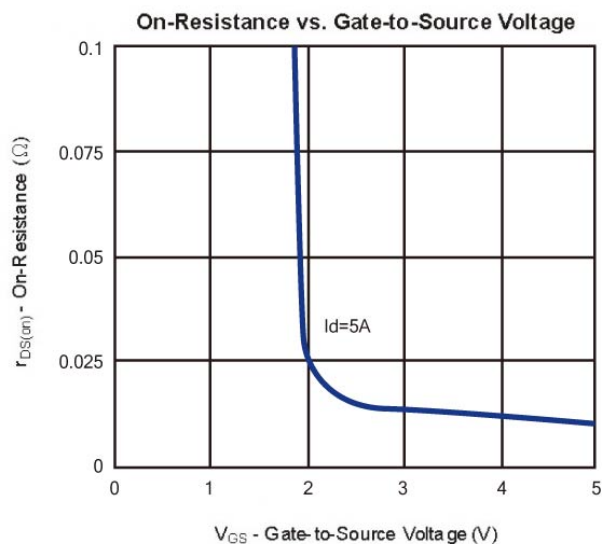
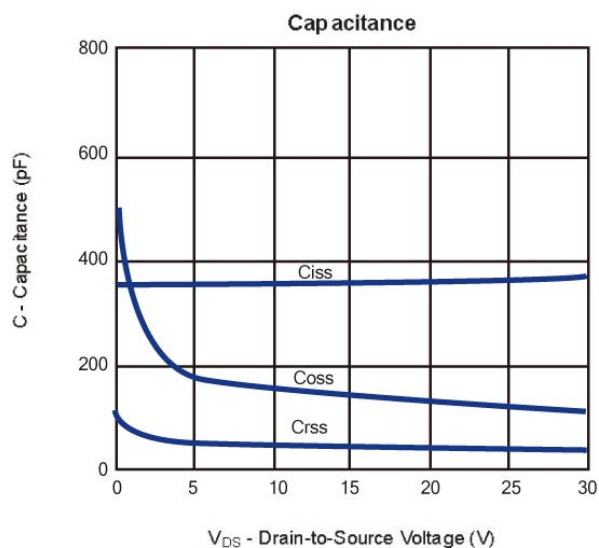
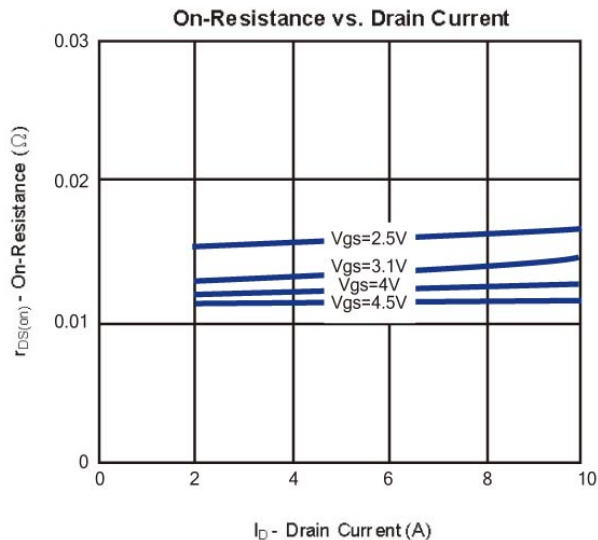
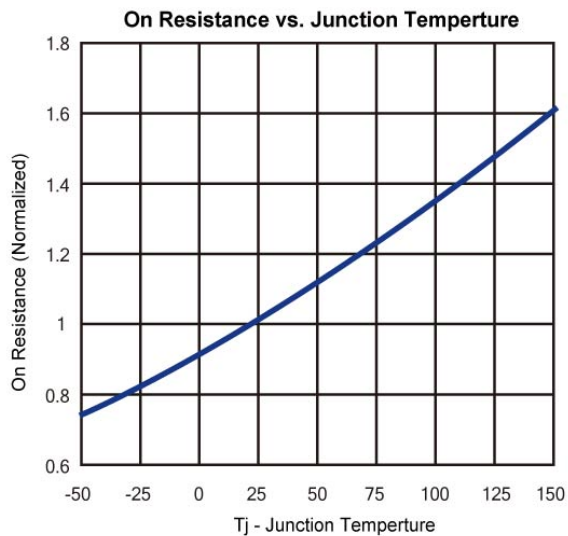
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Electrical Characteristics (TA=25°C Unless Otherwise Specified)

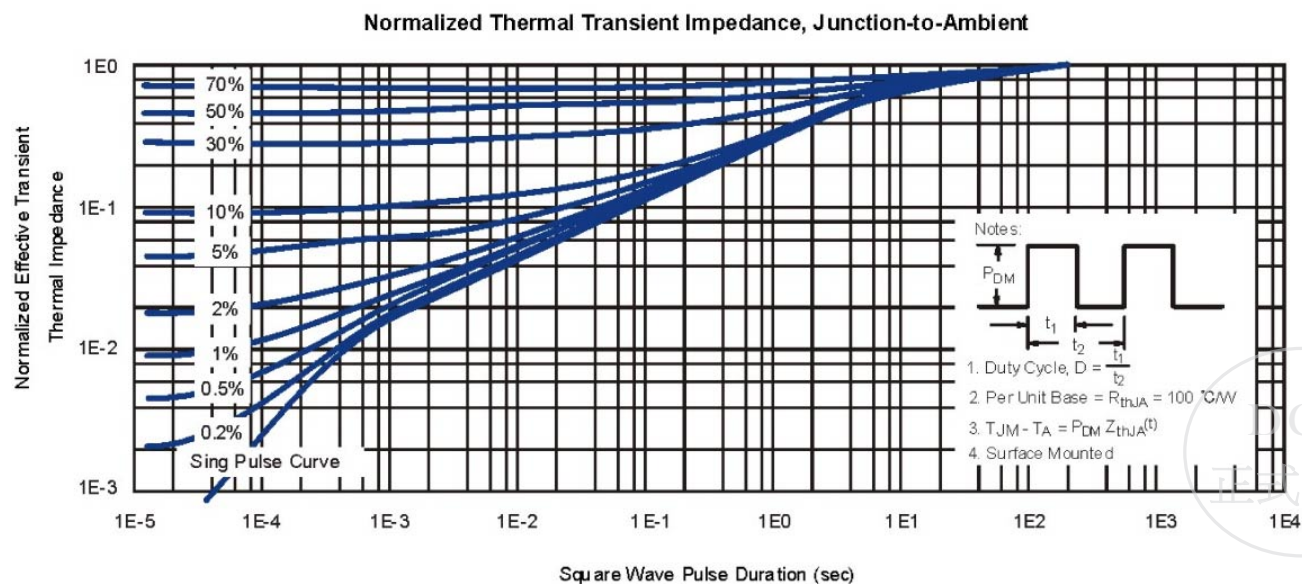
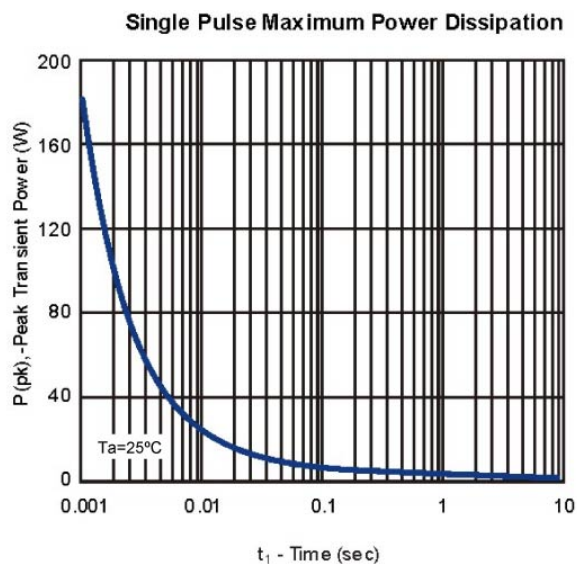
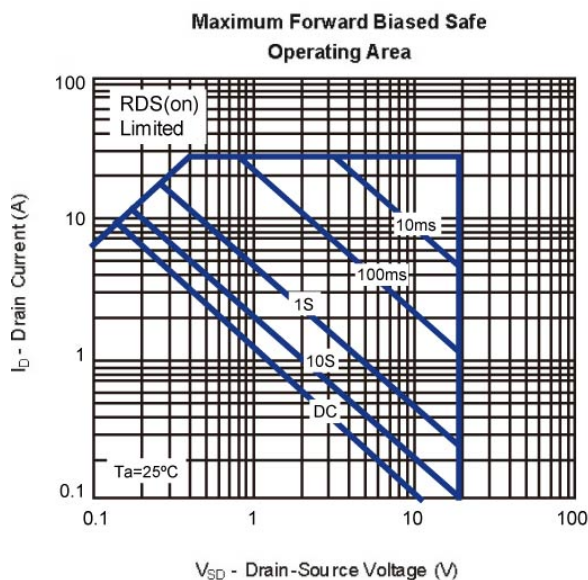
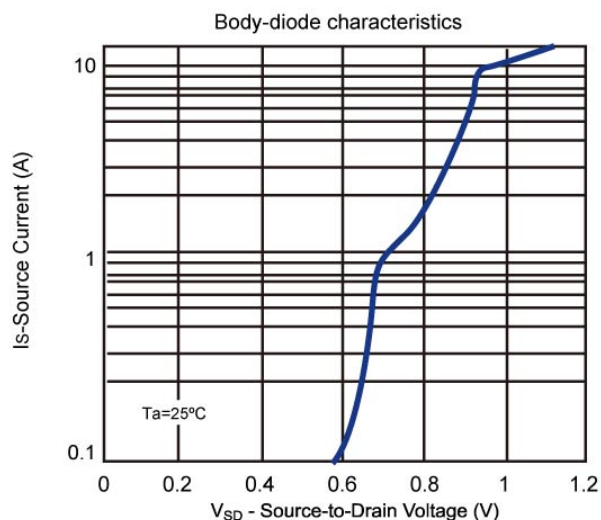
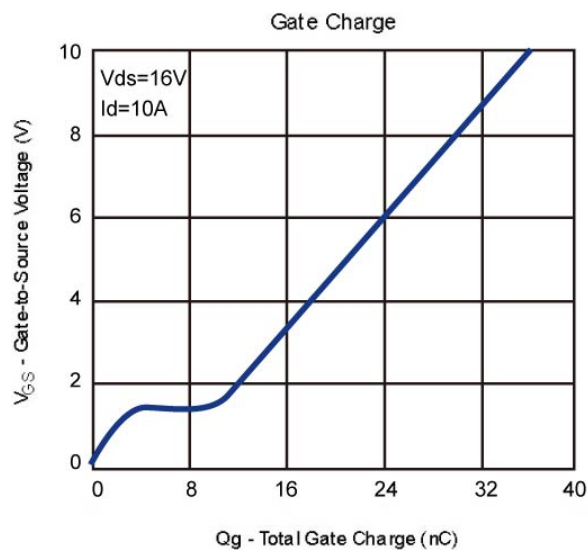
Symbol	Parameter	Limit	Min	Typ	Max	Unit
STATIC						
BV _{DSS}	Drain-Source Breakdown Voltage	V _{GS} =0V, I _D =250 μ A	20			V
V _{GS(th)}	Gate Threshold Voltage	V _{DS} =V _{GS} , I _D =250 μ A	0.6		1.2	V
I _{GSS}	Gate Leakage Current	V _{DS} =0V, V _{GS} = $\pm$ 10V			$\pm$ 10	μ A
I _{DSS}	Zero Gate Voltage Drain Current	V _{DS} =20V, V _{GS} =0V			1	μ A
R _{DS(ON)}	Drain-Source On-State Resistance ^a	V _{GS} =4.5V, I _D =5A		12	14.5	m Ω
		V _{GS} =4V, I _D = 5A		12.5	15	
		V _{GS} =3.1V, I _D = 5A		13.5	17	
		V _{GS} =2.5V, I _D = 5A		16	20	
V _{SD}	Diode Forward Voltage	I _S =10A, V _{GS} =0V		0.9	1.2	V
DYNAMIC						
Q _g	Total Gate Charge	V _{DS} =16V, V _{GS} =10V, I _D =10A		36		nC
Q _g	Total Gate Charge	V _{DS} =16V, V _{GS} =4.5V, I _D =10A		19		
Q _{gs}	Gate-Source Charge			3.2		
Q _{gd}	Gate-Drain Charge			7.4		
C _{iss}	Input Capacitance	V _{DS} =25V, V _{GS} =0V, f=1MHz		365		pF
C _{oss}	Output Capacitance			123		
C _{rss}	Reverse Transfer Capacitance			37		
t _{d(on)}	Turn-On Delay Time	V _{DD} =10V, R _L =2 Ω I _D =5A, V _{GEN} =4V R _G =10 Ω		0.8		μ s
t _r	Turn-On Rise Time			1.1		
t _{d(off)}	Turn-Off Delay Time			4.6		
t _f	Turn-Off Fall Time			2.3		

Notes: a. pulse test: pulse width $\leq$ 300 μ s, duty cycle $\leq$ 2%, Guaranteed by design, not subject to production testing.

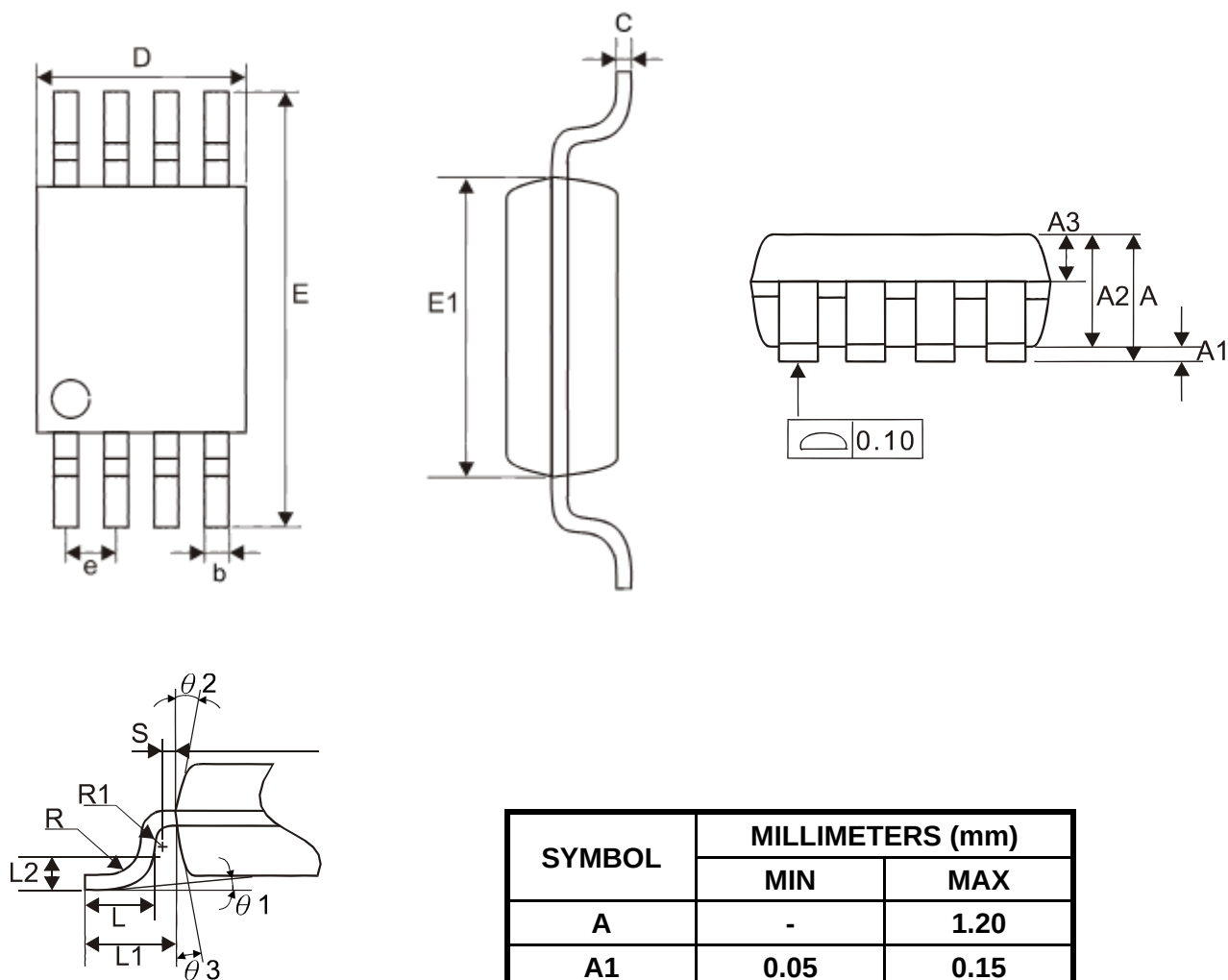
b. Matsuki Electric/ Force mos reserves the right to improve product design, functions and reliability without notice.







TSSOP-8 Package



SYMBOL	MILLIMETERS (mm)	
	MIN	MAX
A	-	1.20
A1	0.05	0.15
A2	0.90	1.05
A3	0.34	0.54
b	0.19	0.30
c	0.09	0.20
D	2.90	3.10
E	6.20	6.60
E1	4.30	4.50
e	0.65BSC	
L	0.45	0.75
L1	1.00REF	
L2	0.25BSC	
R	0.09	-

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