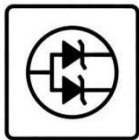


MSKSEMI 美森科

SEMICONDUCTOR



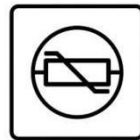
ESD



TVS



TSS



MOV



GDT



PLED

TLV900x-MS

Product specification

GENERAL DESCRIPTION

The TLV9001(single),TLV9002(dual),TLV9004 (quad)are general purpose, low offset, high frequency response and low power operational amplifiers. With an excellent bandwidth of 1M Hz, a slew rate of 1V/ μ s, and a quiescent current of 28 μ A per amplifier at 5Vthe TLV9001/ TLV9002/TLV9004 family can be designed into a wide range of applications.

The TLV900x-MS op-amps are designed to provide optimal performance in low voltage and low power systems. The input common-mode voltage range includes ground , and the maximum input offset voltage are 3mV.

These parts provide rail-to-rail output swing into heavy loads.

The TLV900x-MS families of operational amplifiers are specified at the full temperature range of -40°C to +85°C under single or dual power supplies of 1.8V to 5.5V.

FEATURES

- Input Offset Voltage: 1mV(Typical)
- Low Supply Current: 28 μ A($V_s=5V$)Su
- pply Range: 1.8V to 5.5V
- Gain Bandwidth: 1MHz($V_s=5V$)
- Slew rate: 1V/us($V_s=5V$)
- Rail-to-Rail Input and Output
- Low Cost
- Micro size Packages:
- TLV9001: SOT23-5 SC70-5
- TLV9002: SOP-8 MSOP-8 TSSOP-8
- TLV9004: SOP-14 TSSOP-14

APPLICATIONS

- Battery and Power Supply Control
- Audio Outputs
- Smoke/Gas/Environment Sensors
- Portable Equipment and Mobile Devices
- Sensor Interfaces
- Active Filters
- Medical Equipment

TYPICAL APPLICATION

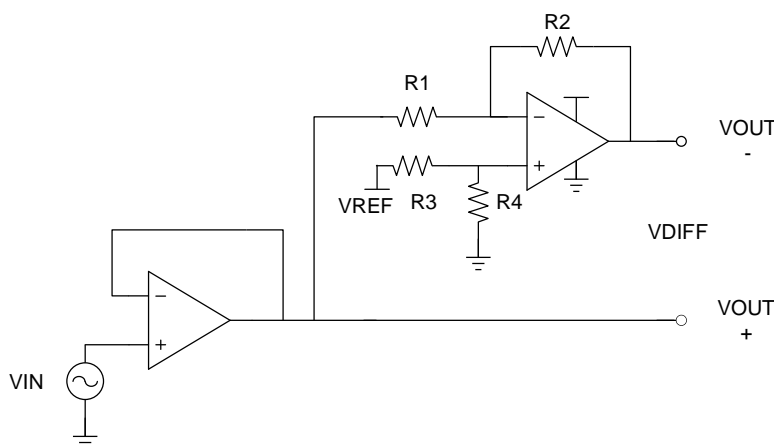


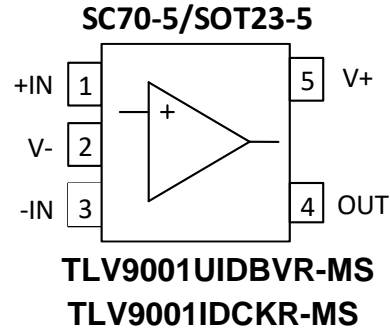
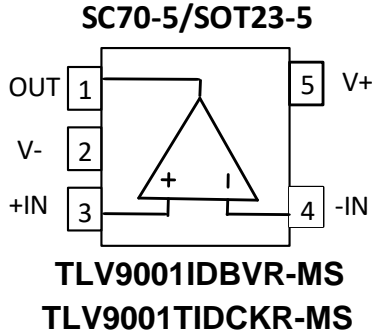
Figure 1. Typical Application

PACKAGE/ORDER INFORMATION

P/N	PKG	QTY	MARKING
TLV9001IDBVR-MS	SOT-23-5	3000PCS	10GF MS
TLV9001TIDCKR-MS	SC-70-5	3000PCS	1 D 6 MS
TLV9001UIDBVR-MS	SOT-23-5	3000PCS	1ODF MS
TLV9001IDCKR-MS	SC-70-5	3000PCS	1 B Z MS
TLV9002IDR-MS	SOIC-8	2500PCS	MSKSEMI 9002IDR MS***
TLV9002IPWR-MS	TSSOP-8	2500PCS	9002 IPWR MS***
TLV9002IDGKR-MS	VSSOP-8	2500PCS	9 0 0 2 I D G K
TLV9004IDR-MS	SOIC-14	2500PCS	MSKSEMI 9004IDR MS***
TLV9004IPWR-MS	TSSOP-14	3000PCS	MSKSEMI 9004IPWR MS***

Pin Configuration and Functions (Top View)

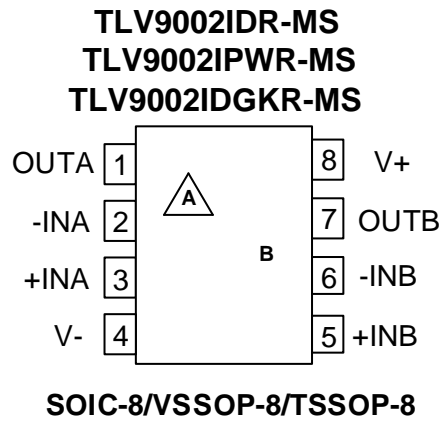
Pin Description



Number		NAME	I/O	DESCRIPTION
TLV9001IDBVR-MS TLV9001TIDCKR-MS	TLV9001IDCKR-MS TLV9001UIDBVR-MS			
3	1	+IN	I	Positive (noninverting) input
4	3	-IN	I	Negative (inverting) input
1	4	OUT	O	Output
2	2	V-	-	Positive (highest) power supply
5	5	V+	-	Negative (lowest) power supply

Pin Configuration and Functions (Top View)

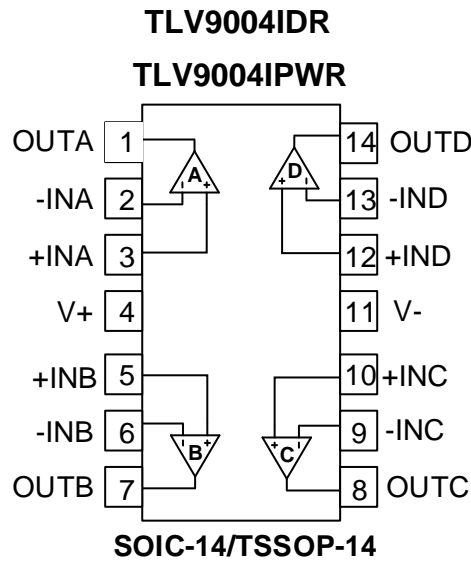
Pin Description



PIN		I/O	DESCRIPTION
NAME	Number		
+INA	3	I	Noninverting input, channel A
+INB	5	I	Noninverting input, channel B
-INA	2	I	Inverting input, channel A
-INB	6	I	Inverting input, channel B
OUTA	1	O	Output, channel A
OUTB	7	O	Output, channel B
V-	4	-	Negative (lowest) power supply
V+	8	-	Positive (highest) power supply

Pin Configuration and Functions (Top View)

Pin Description



PIN		I/O	DESCRIPTION
NAME	Number		
+INA	3	I	Noninverting input, channel A
+INB	5	I	Noninverting input, channel B
+INC	10	I	Noninverting input, channel C
+IND	12	I	Noninverting input, channel D
-INA	2	I	Inverting input, channel A
-INB	6	I	Inverting input, channel B
-INC	9	I	Inverting input, channel C
-IND	13	I	Inverting input, channel D
OUTA	1	O	Output, channel A
OUTB	7	O	Output, channel B
OUTC	8	O	Output, channel C
OUTD	14	O	Output, channel D
V-	4	-	Negative (lowest) power supply
V+	11	-	Positive (highest) power supply

SPECIFICATIONS

Absolute Maximum Ratings⁽¹⁾

		MIN	MAX	UNIT
Voltage	Supply Voltage		6	V
	Signal Input Terminals Voltage ⁽²⁾	(V-) - 0.5	(V+) + 0.5	V
	Signal Input Terminals Voltage ⁽³⁾	(V-) - 0.5	(V+) + 0.5	V
Current	Signal Input Terminals Current ⁽²⁾	-10	10	mA
	Signal output Terminals Current ⁽³⁾	-200	200	mA
	Output Short-Circuit ⁽⁴⁾	Continuous		
θ_{JA}	Operating Temperature Range	-40	85	°C
	Storage Temperature Range	-65	150	°C
	Junction Temperature	-40	150	°C

(1) Stresses above these ratings may cause permanent damage. Exposure to absolute maximum conditions for extended periods may degrade device reliability. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those specified is not implied.

(2) Input terminals are diode clamped to the power-supply rails. Input signals that can swing more than 0.5V beyond the supply rails should be current limited to 10mA or less.

(3) Output terminals are diode-clamped to the power-supply rails. Output signals that can swing more than 0.5V beyond the supply rails should be current-limited to ± 200 mA or less.

(4) Short-circuit to ground, one amplifier per package.

ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human-Body Model (HBM)	± 2000	V
		Charged-Device Model (CDM)	± 500	V
		Machine Model	100	V

Recommended Operating Conditions

		MIN	MAX	UNIT
Supply voltage, $V_S = (V+) - (V-)$	Single-supply	1.8	5.5	V
	Dual-supply	± 0.9	± 2.75	V

ELECTRICAL CHARACTERISTICS ($V_S = +5V$)

At $T_A = 25^\circ\text{C}$, $V_{CM} = V_{OUT} = V_S / 2$, unless otherwise noted.

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNIT
OFFSET VOLTAGE					
V_{OS}	Input Offset Voltage	-3	± 1	3	mV
dV_{OS}/dT	Input Offset Voltage Average Drift	$T_A = -40^\circ\text{C}$ to 85°C		1.8	$\mu\text{V}/^\circ\text{C}$

INPUT CURRENT

I_B	Input Bias Current			5		pA
I_{OS}	Input Offset Current			1		pA

NOISE

V_N	Input Voltage Noise	$f=0.1\text{Hz to }10\text{Hz}$		20		μV_{PP}
e_n	Input Voltage Noise Density	$f=1\text{kHz}$		65		$\text{nV}/\sqrt{\text{Hz}}$

INPUT VOLTAGE

V_{CM}	Common-Mode Voltage Range		$V_{S-}-0.1$		$V_{S+}+0.1$	V
CMRR	Common-Mode Rejection Ratio	$V_{CM}=0.1\text{V to }4\text{V}$	70	80		dB

FREQUENCY RESPONSE

GBW	Gain-Bandwidth Product			1		MHz
SR	Slew Rate	$G = +1,$ $V_{IN}=2\text{V Step}$		1		V/us
t_s	Settling Time to 0.1%	$G = +1,$ $V_{IN}=2\text{V Step}$		2.5		us

OUTPUT

A_V	Open-Loop Voltage Gain	$V_{OUT}=0.1\text{V to }4.9\text{V}$ $R_L=100\text{k}\Omega$	80	100		dB
$V_{OUT-SWING}$	Output Swing from Rail	$R_L=100\text{k}\Omega$			5	mV
I_{SC}	Output Short-Circuit Current	Source current		45		mA
		Sink current		70		mA
$C_L^{(1)}$	Capacitive Load Drive	$G = +1,$ $V_{IN}=0.2\text{V Step}$			1000	pF

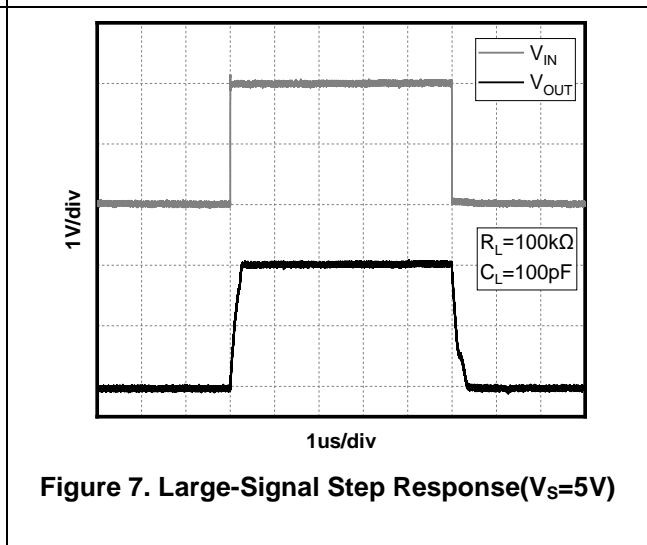
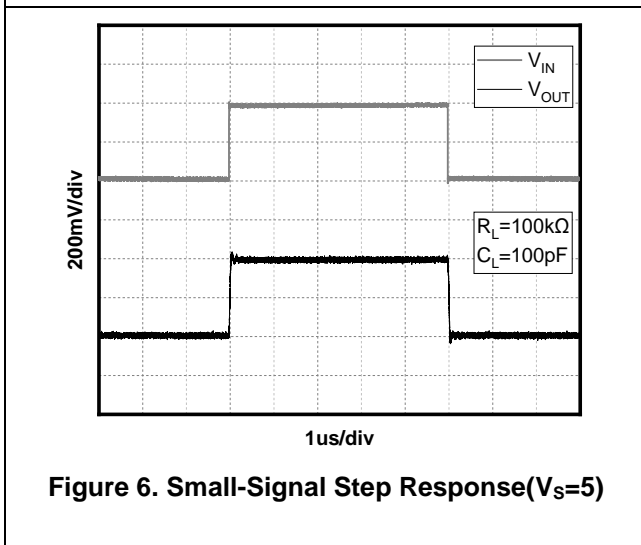
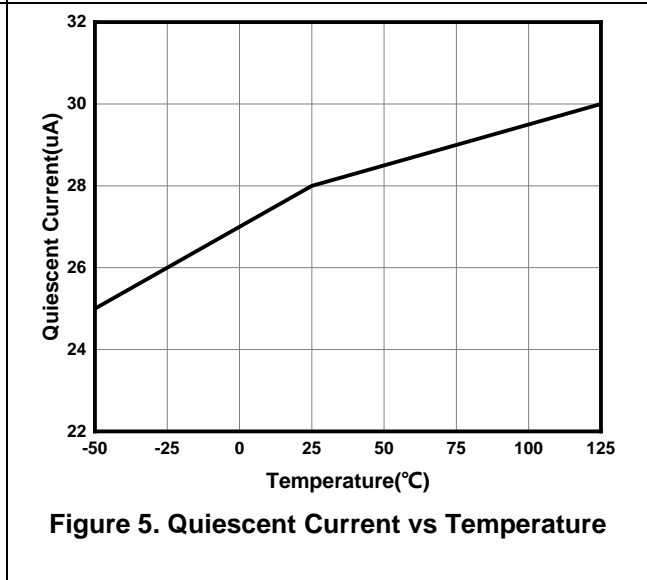
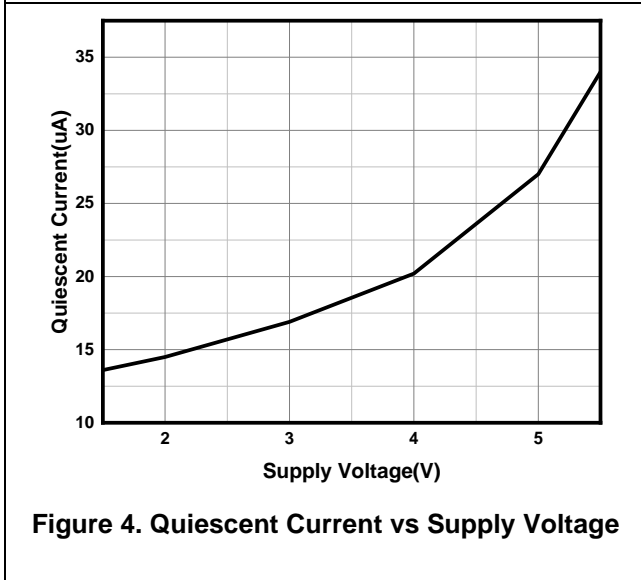
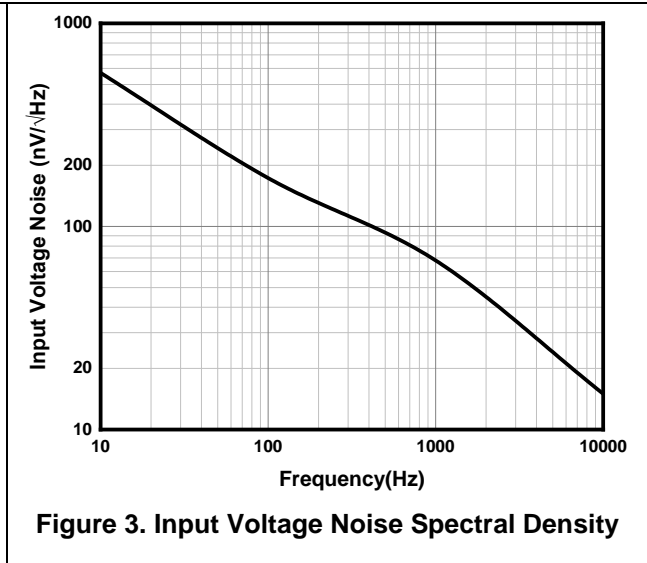
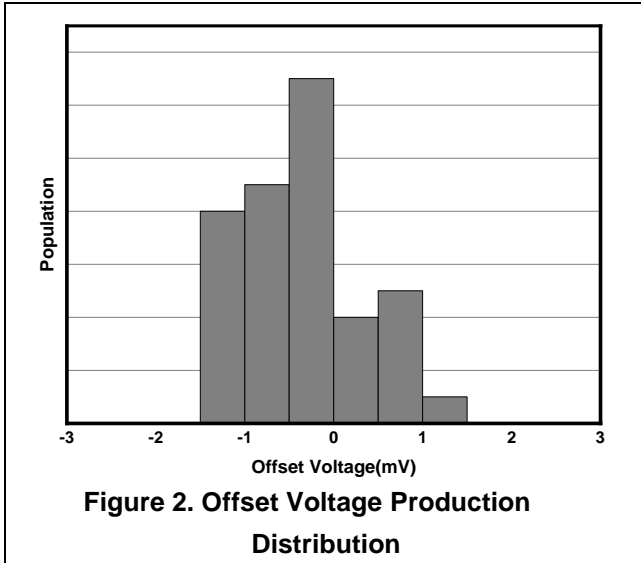
POWER SUPPLY

PSRR	Power-Supply Rejection Ratio	$V_S=1.8\text{V to }5.5\text{V}$	80	90		dB
V_S	Operating Voltage Range		1.8		5.5	V
I_Q	Quiescent Current/Amplifier	$I_O=0\text{A}$		28	40	uA

(1) Capacitive load drive means that above a given maximum value, the output waveform will oscillate under the step response.

TYPICAL CHARACTERISTICS

At $T_A = 25^\circ\text{C}$, $V_S = +5\text{V}$, $G=+1$, $V_{IN}=V_{OUT}= V_S / 2$, unless otherwise noted.



TYPICAL CHARACTERISTICS

At $T_A = 25^\circ\text{C}$, $V_S = +5\text{V}$, $G=+1$, $V_{IN}=V_{OUT}= V_S / 2$, unless otherwise noted.

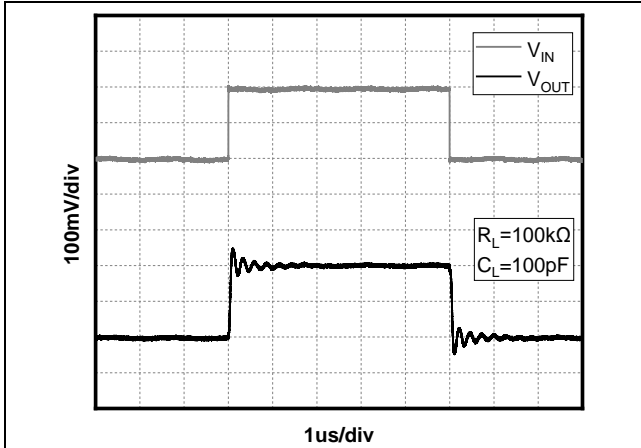


Figure 8. Small-Signal Step Response($V_S=1.5\text{V}$)

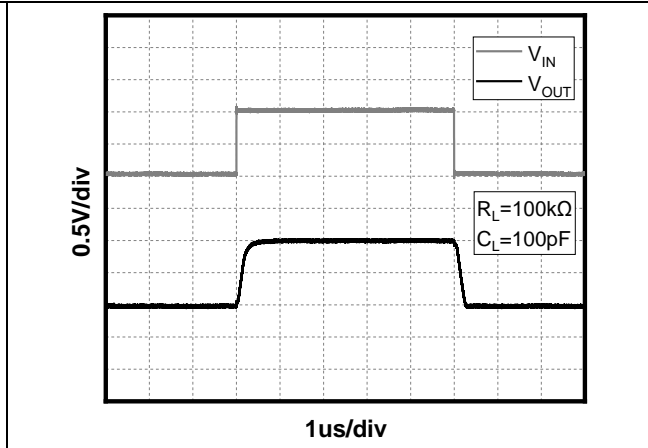


Figure 9. Large-Signal Step Response($V_S=1.5\text{V}$)

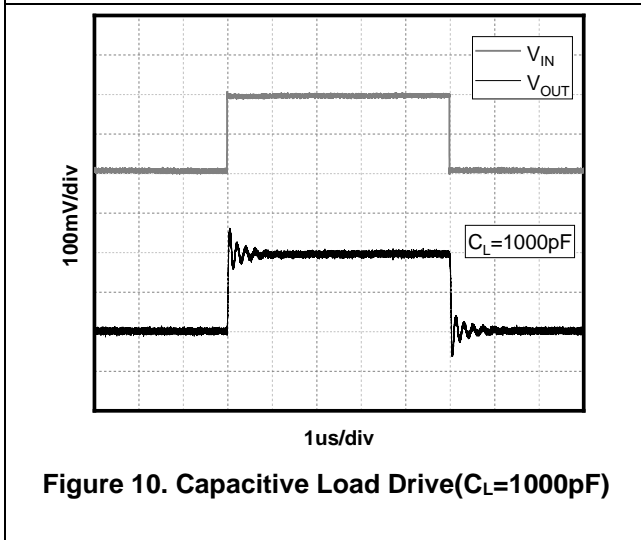


Figure 10. Capacitive Load Drive($C_L=1000\text{pF}$)

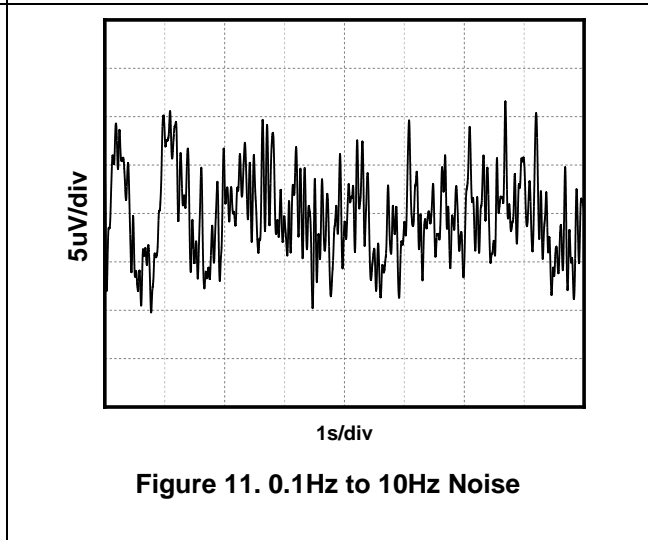


Figure 11. 0.1Hz to 10Hz Noise

Detailed Description

Overview

The TLV900x-MS devices are a low power, unity-gain stable, rail-to-rail operational amplifier that operate in a single-supply voltage range of 1.8V to 5.5V ($\pm 0.9V$ to $\pm 2.75V$). A high supply voltage of 6V (absolute maximum) can permanently damage the amplifier. Rail-to-rail input and output wobbles significantly increase the dynamic range, especially in low-supply applications. Good layout practices require that a 0.1 μF capacitor be used where it is tightly threaded through the power supply pin.

Phase Reversal Protection

The TLV900x-MS devices have internal phase-reversal protection. Many op amp exhibit phase reversal when the input is driven beyond the linear common-mode range. This condition is most often encountered in noninverting circuits when the input is driven beyond the specified common-mode voltage range, causing the output to reverse into the opposite rail.

The input of the TLV900x-MS prevents phase reversal with excessive common mode voltage. Instead, the appropriate rail limits the output voltage.

Typical Applications

1 Voltage Follower

As shown in Figure 12, the voltage gain is 1. With this circuit, the output voltage V_{OUT} is configured to be equal to the input voltage V_{IN} . Due to the high input impedance and low output impedance, the circuit can also stabilize the output voltage, the output voltage expression is

$$V_{OUT} = V_{IN} \quad (1)$$

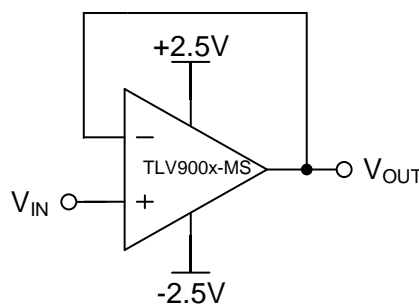


Figure 12. Voltage Follower

2 Inverting Proportional Amplifier

As shown in Figure 13, for a reverse-phase proportional amplifier, the input voltage V_{IN} is amplified by a voltage gain that depends on the ratio of R_1 to R_2 . The output voltage V_{OUT} is inversely with the input voltage V_{IN} . The input impedance of the circuit is equal to R_1 , and the output voltage expression is

$$V_{OUT} = -\frac{R_2}{R_1} V_{IN} \quad (2)$$

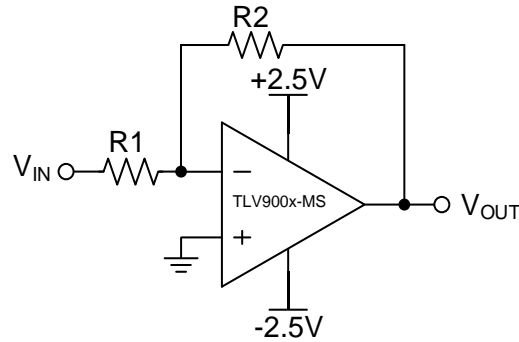


Figure 13. Inverting Proportional Amplifier

3 Noninverting Proportional Amplifier

As shown in Figure 14, for a noninverting amplifier, the input voltage V_{IN} is amplified by a voltage gain that depends on the ratio of $R1$ to $R2$. The output voltage V_{OUT} is in phase with the input voltage V_{IN} . In fact, this circuit has a high input impedance because its input side is the same as the input side of the operational amplifier. The output voltage expression is

$$V_{OUT} = \left(1 + \frac{R2}{R1}\right) V_{IN} \quad (3)$$

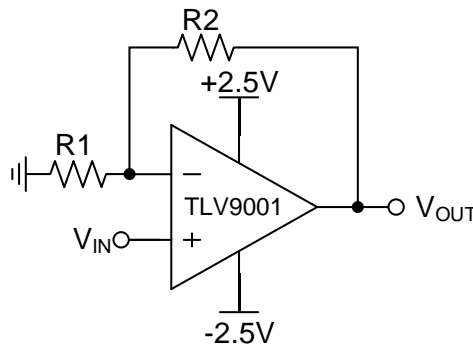


Figure 14. Noninverting Proportional Amplifier

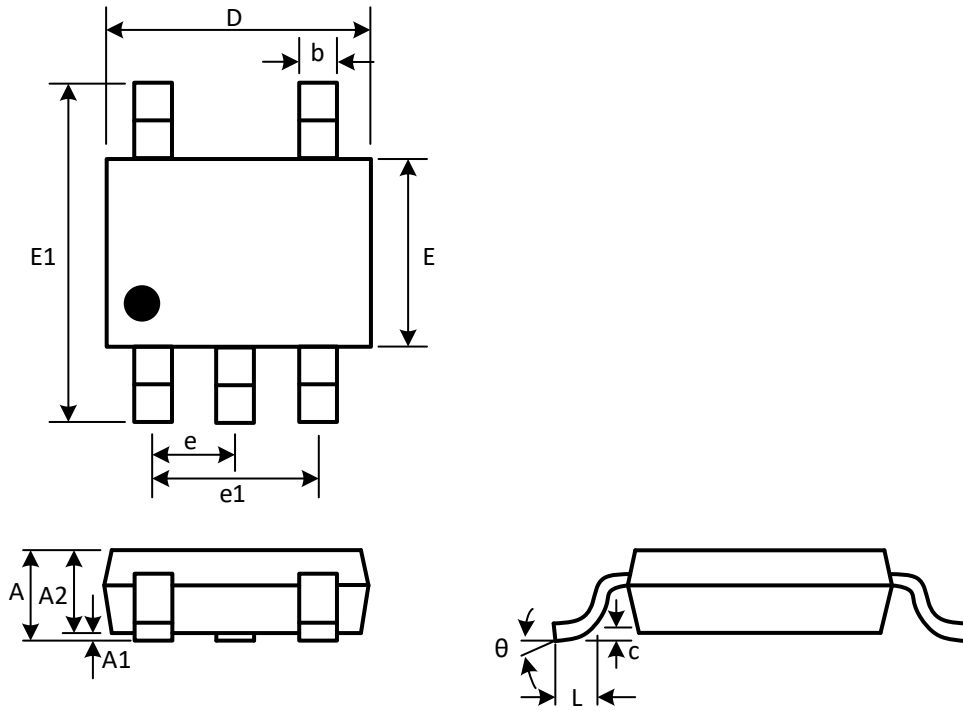
Layout Guidelines

Attention to good layout practices is always recommended. Keep traces short. When possible, use a PCB ground plane with surface-mount components placed as close to the device pins as possible. Place a 0.1µF capacitor closely across the supply pins.

These guidelines should be applied throughout the analog circuit to improve performance and provide benefits such as reducing the EMI susceptibility.

PACKAGE DESCRIPTION

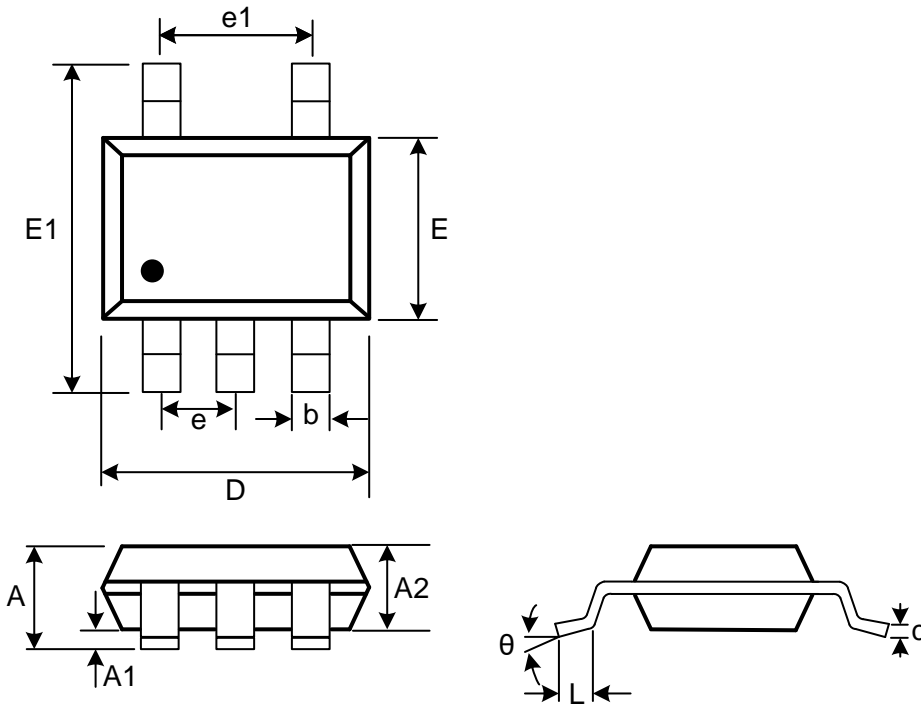
SOT23-5



(Unit: mm)

Symbol	Min	Max
A	1.050	1.250
A1	0.000	0.100
A2	1.050	1.150
b	0.300	0.500
c	0.100	0.200
D	2.820	3.020
e	0.950(BSC)	
e1	1.800	2.000
E	1.500	1.700
E1	2.650	2.950
L	0.300	0.600
θ	0°	8°

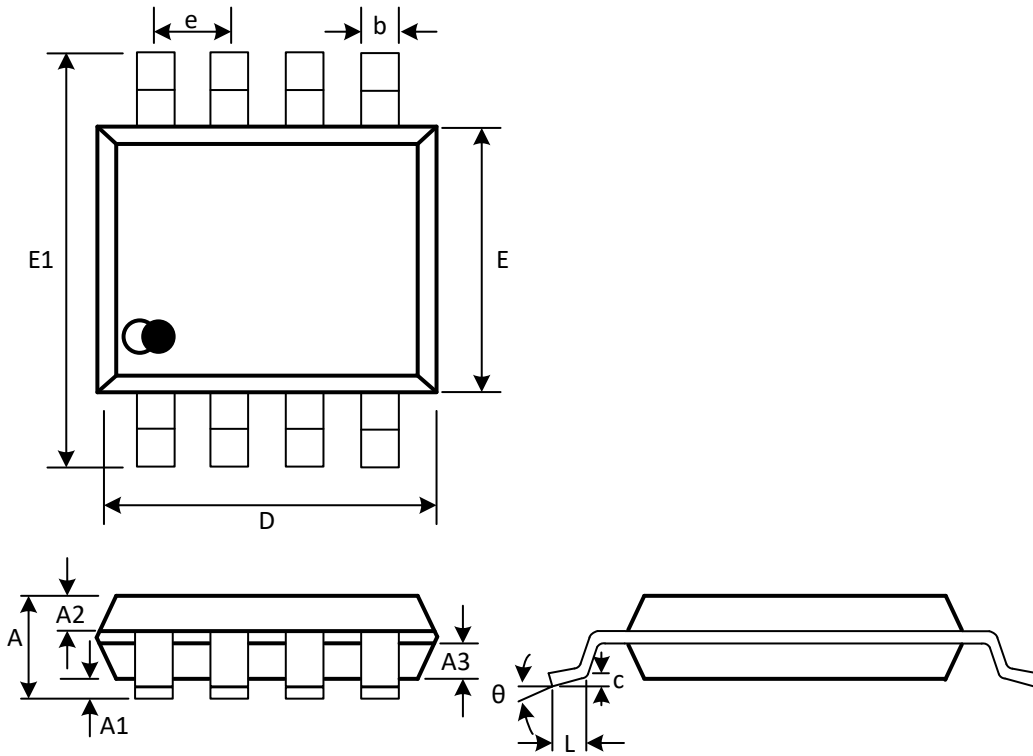
SC70-5 (SOT353)



(Unit: mm)

Symbol	Min	Max
A	0.8	1.1
A1	0	0.1
b	0.15	0.3
c	0.15	
D	1.85	2.15
e	0.65 (BSC)	
e1	1.3 (BSC)	
E	1.1	1.4
E1	1.8	2.4
L	0.26	0.46
θ	0°	8°

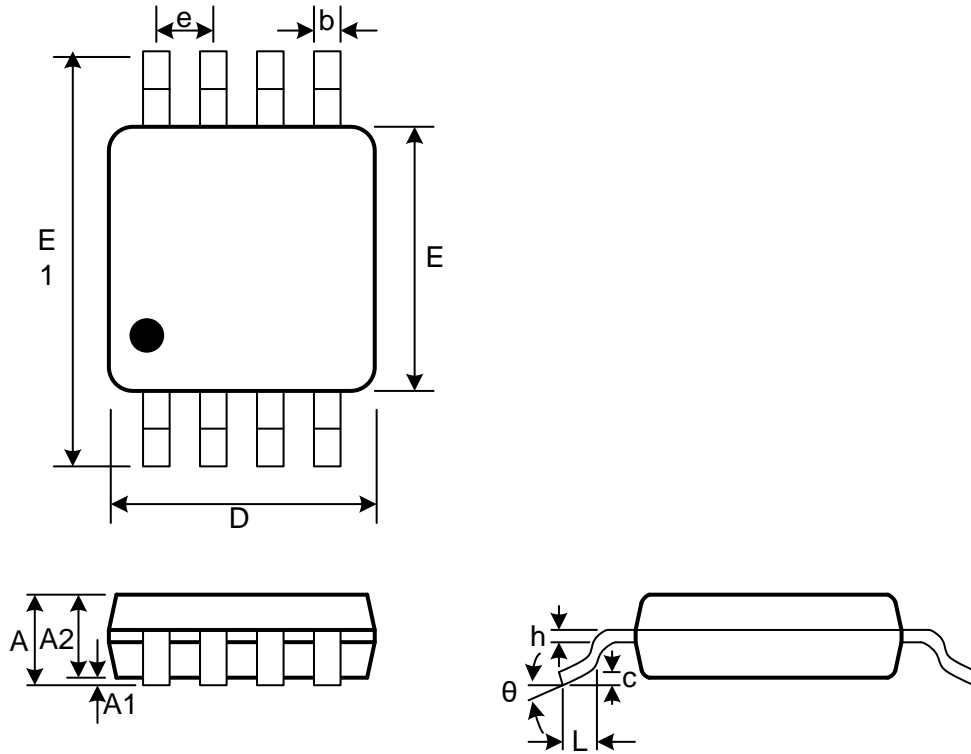
SOP-8



(Unit: mm)

Symbol	Min	Max
A	1.300	1.600
A1	0.050	0.200
A2	0.550	0.650
A3	0.550	0.650
b	0.356	0.456
c	0.203	0.233
D	4.800	5.000
e	1.270(BSC)	
E	3.800	4.000
E1	5.800	6.200
L	0.400	0.800
θ	0°	8°

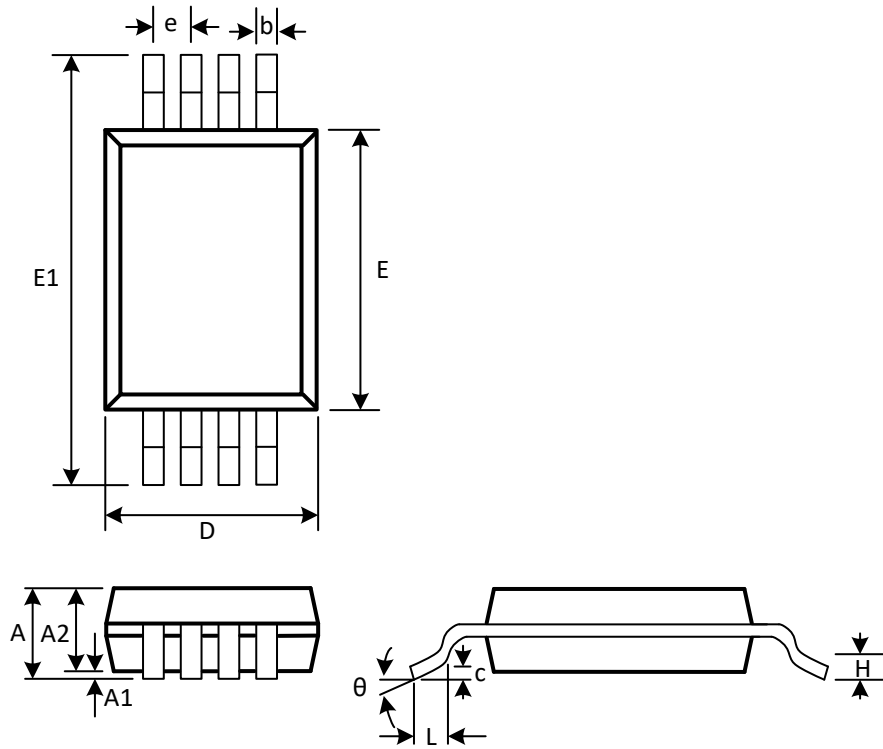
VSSOP8



(Unit: mm)

Symbol	Min	Max
A		1.100
A1	0.050	0.150
A2		0.950
b	0.250	0.380
c	0.250	
D	2.900	3.100
e	0.650(BSC)	
E	2.900	3.100
E1	4.750	5.050
h	0.130	0.230
L	0.400	0.700
θ	0°	8°

TSSOP-8

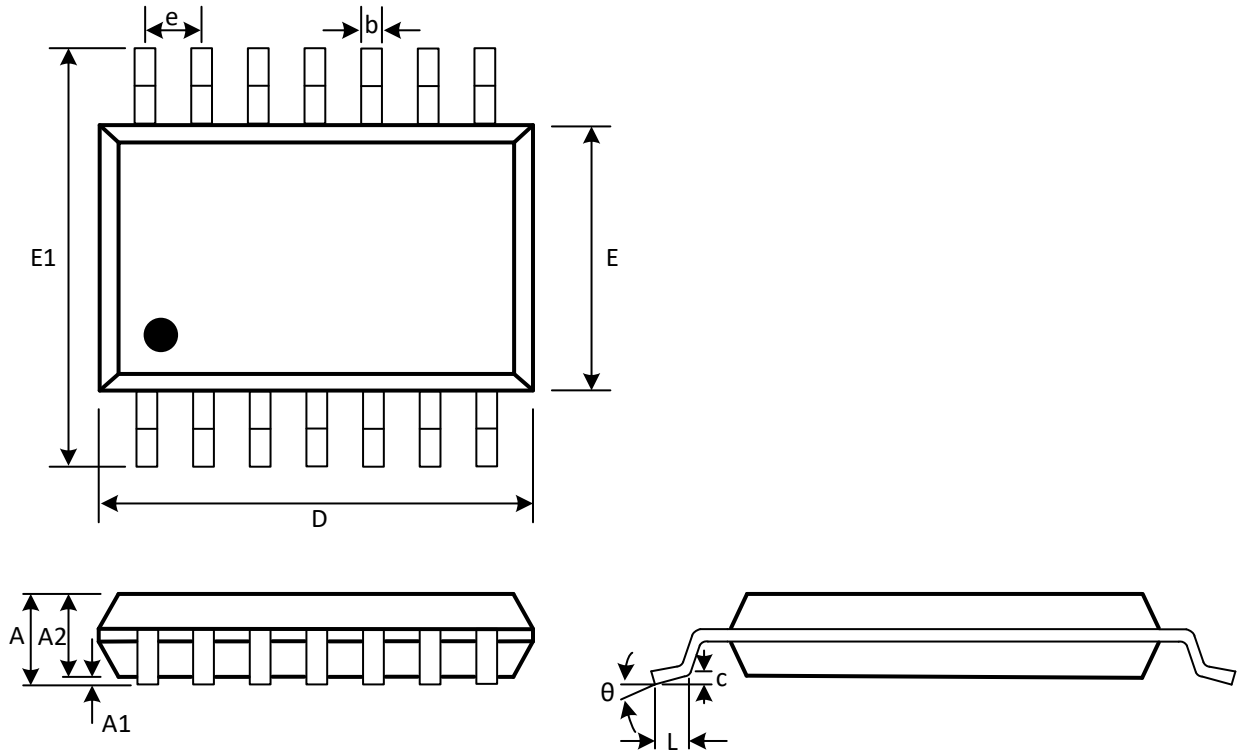


(Unit: mm)

Symbol	Min	Max
A		1.100
A1	0.050	0.150
A2	0.800	1.000
b	0.190	0.300
c	0.090	0.200
D	2.900	3.100
e	0.650(BSC)	
E	4.300	4.500
E1	6.250	6.550
H	0.250	
L	0.500	0.700
θ	1°	7°

PACKAGE DESCRIPTION

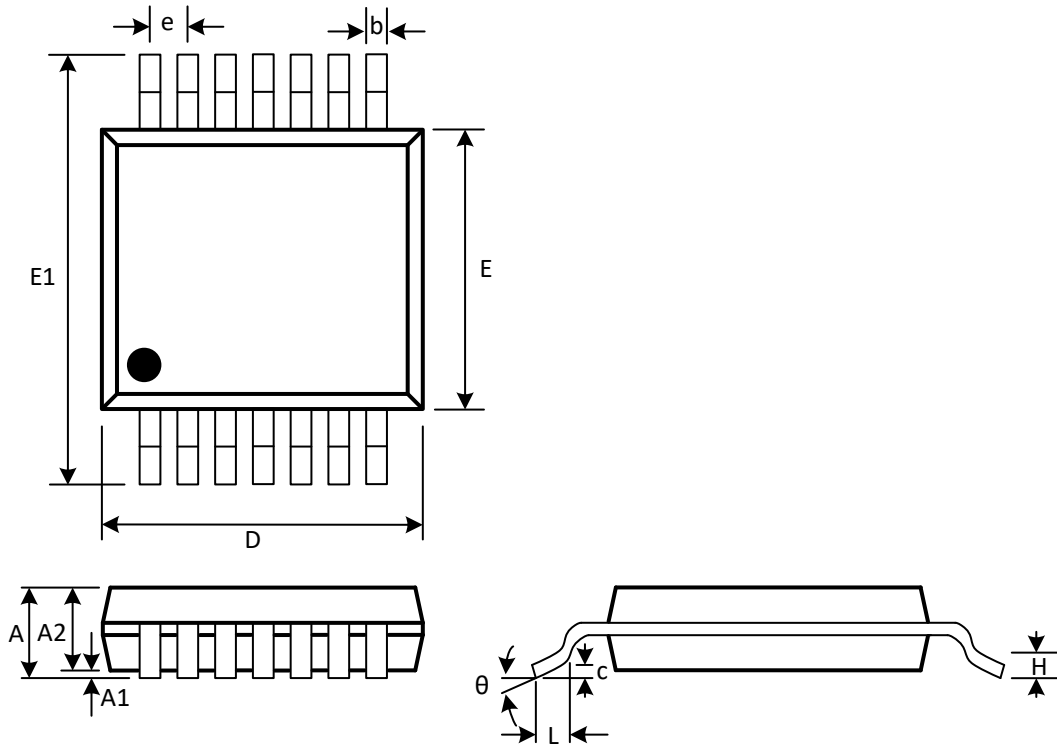
SOIC-14(SOP-14)



(Unit: mm)

Symbol	Min	Max
A	1.350	1.750
A1	0.100	0.250
A2	1.350	1.550
b	0.310	0.510
c	0.100	0.250
D	8.450	8.850
e	1.270(BSC)	
E1	5.800	6.200
E	3.800	4.000
L	0.400	1.270
θ	0°	8°

TSSOP-14



(Unit: mm)

Symbol	Min	Max
A		1.200
A1	0.050	0.150
A2	0.800	1.050
b	0.190	0.300
c	0.090	0.200
D	4.860	5.100
e	0.650(BSC)	
E	4.300	4.500
E1	6.250	6.550
L	0.500	0.700
	0.250(TYP)	
θ	1°	7°

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