1. DESCRIPTION

The XLCD74HC4515 are high-speed silicon gate devices consisting of a 4-bit strobed latch and a 4-to 16-line decoder. The selected output is enabled by a low on the enable input ($\overline{E}$). A high on $\overline{E}$ inhibits selection of any output. Demultiplexing is accomplished by using the E input as the data input and the select inputs (A0- A3) as addresses. This E input also serves as a chip select when these devices are cascaded.

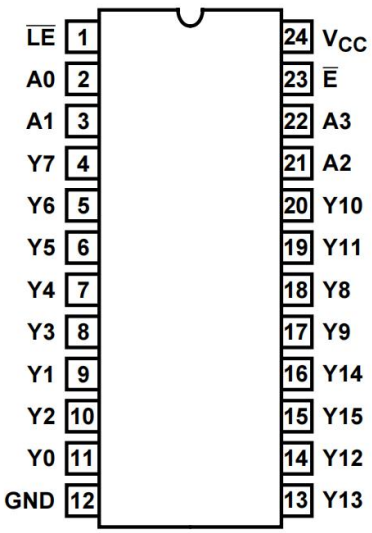
When Latch Enable ($\overline{LE}$) is high the output follows changes in the inputs (see truth table). When $\overline{LE}$ is low the output is isolated from changes in the input and remains at the level (low for the 4515) it had before the latches were enabled. These devices, enhanced versions of the equivalent CMOS types, can drive 10 LSTTL loads.

2. FEATURES

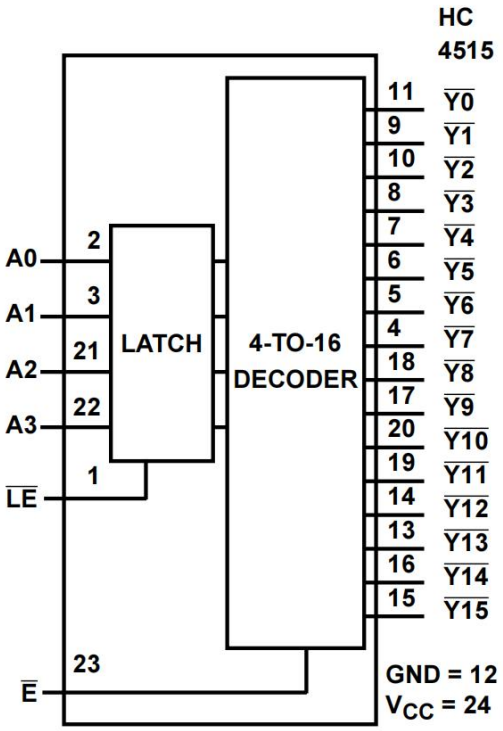
- Multifunction Capability
  - Binary to 1-of-16 Decoder
  - 1-to-16 Line Demultiplexer
- Fanout (Over Temperature Range)
  - Standard Outputs . . . . . 10 LSTTL Loads
  - Bus Driver Outputs . . . . . 15 LSTTL Loads
- Wide Operating Temperature Range . . . -40°C to 85°C
- Balanced Propagation Delay and Transition Times
- Significant Power Reduction Compared to LSTTL Logic ICs
- HC Types
  - 2V to 6V Operation
  - High Noise Immunity: N_{IL} = 30%, N_{IH} = 30% of V_{CC} at V_{CC} = 5V

3. PINOUT

XLCD74HC4515M96(SOP)
TOP VIEW



4. FUNCTIONAL DIAGRAM



DECODE TRUTH TABLE (LE = 1)

ENABLE	DECODER INPUTS				ADDRESSED OUTPUT 4515 = LOGIC 0(HIGH)
	A3	A2	A1	A0	
0	0	0	0	0	Y0
0	0	0	0	1	Y1
0	0	0	1	0	Y2
0	0	0	1	1	Y3
0	0	1	0	0	Y4
0	0	1	0	1	Y5
0	0	1	1	0	Y6
0	0	1	1	1	Y7
0	1	0	0	0	Y8
0	1	0	0	1	Y9
0	1	0	1	0	Y10
0	1	0	1	1	Y11
0	1	1	0	0	Y12
0	1	1	0	1	Y13
0	1	1	1	0	Y14
0	1	1	1	1	Y15
1	X	X	X	X	All Outputs = 1, 4515

X = Don't Care; Logic 1 = High; Logic 0 = Low

5. ABSOLUTE MAXIMUM RATINGS

DC Supply Voltage, V_{CC} . . . . . -0.5V to 7V

DC Input Diode Current, I_{IK}

For V_I < -0.5V or V_I > V_{CC} + 0.5V. . . . . .±20mA

DC Output Diode Current, I_{OK}

For V_O < -0.5V or V_O > V_{CC} + 0.5V . . . . . .±20mA

DC Drain Current, per Output, I_O

For -0.5V < V_O < V_{CC} + 0.5V. . . . . .±25mA

DC Output Source or Sink Current per Output Pin, I_O

For V_O > -0.5V or V_O < V_{CC} + 0.5V . . . . . .±25mA

DC V_{CC} or Ground Current, I_{CC} . . . . . .±50m

6. THERMAL INFORMATION

Thermal Resistance (Typical) . . . . . .θ_{JA} (°C/W)

SOP Package (Note 2). 46

Maximum Junction Temperature . . . . . 150°C

Maximum Storage Temperature Range . . . . . .-65°C to 150°C

Maximum Lead Temperature (Soldering 10s) . . . . . 300°C

7. OPERATING CONDITIONS

Temperature Range (TA) . . . . . -40°C to 85°C

Supply Voltage Range, V_{CC}

HC Types . . . . . .2V to 6V

DC Input or Output Voltage, V_I , V_O . . . . . 0V to VCC

Input Rise and Fall Time

2V . . . . . 1000ns (Max)

4.5V. . . . . 500ns (Max)

6V . . . . . 400ns (Max)

CAUTION: Stresses above those listed in “Absolute Maximum Ratings” may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

NOTES:

1. The package thermal impedance is calculated in accordance with JESD 51-7.

8. DC ELECTRICAL SPECIFICATIONS

PARAMETER	SYMBOL	TEST CONDITIONS		V_{CC} (V)	25°C			-40°C TO 85°C		UNITS
		V_I(V)	I_O(mA)		MIN	TYP	MAX	MIN	MAX	
HC TYPES										
High Level Input Voltage	V_{IH}	-	-	2	1.5	-	-	1.5	-	V
				4.5	3.15	-	-	3.15	-	V
				6	4.2	-	-	4.2	-	V
Low Level Input Voltage	V_{IL}	-	-	2	-	-	0.5	-	0.5	V
				4.5	-	-	1.35	-	1.35	V
				6	-	-	1.8	-	1.8	V
High Level Output Voltage CMOS Loads	V_{OH}	V_{IH}or V_{IL}	-0.02	2	1.9	-	-	1.9	-	V
			-0.02	4.5	4.4	-	-	4.4	-	V
			-0.02	6	5.9	-	-	5.9	-	V
High Level Output Voltage TTL Loads			-	-	-	-	-	-	-	V
			-4	4.5	3.98	-	-	3.84	-	V
			-5.2	6	5.48	-	-	5.34	-	V
Low Level Output Voltage CMOS Loads	V_{OL}	V_{IH}or V_{IL}	0.02	2	-	-	0.1	-	0.1	V
			0.02	4.5	-	-	0.1	-	0.1	V
			0.02	6	-	-	0.1	-	0.1	V
Low Level Output Voltage TTL Loads			-	-	-	-	-	-	-	V
			4	4.5	-	-	0.26	-	0.33	V
			5.2	6	-	-	0.26	-	0.33	V
Input Leakage Current	I_I	V_{CC} or GND	-	6	-	-	±0.1	-	±1	μA
Quiescent Device Current	I_{CC}	V_{CC} or GND	0	6	-	-	8	-	80	μA

9. PREREQIOSOTE FPR SWITCHING SPECIFICATIONS

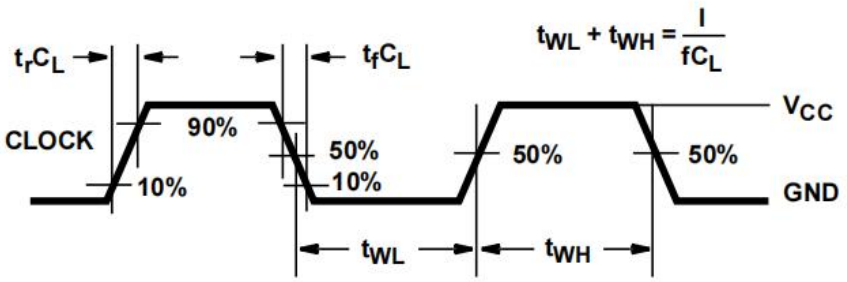
PARAMETER	SYMBOL	TEST CONDITIONS	V_{CC} (V)	25°C			-40°C TO 85°C		UNITS
				MIN	TYP	MAX	MIN	MAX	
HC TYPES									
LE Pulse Width	t_W	-	2	75	-	-	95	-	ns
			4.5	30	-	-	19	-	ns
			6	35	-	-	16	-	ns
Select to LE Set-Up Time	t_{SU}	-	2	100	-	-	125	-	ns
			4.5	20	-	-	25	-	ns
			6	17	-	-	21	-	ns
Select to LE Hold Time	t_H	-	2	0	-	-	0	-	ns
			4.5	0	-	-	0	-	ns
			6	0	-	-	0	-	ns

10. SWITCHING SPECIFICATIONS C_L = 50pF, Input t_r, t_f = 6ns

PARAMETER	SYMBOL	TEST CONDITIONS	VCC (V)	25°C			-40°C TO 85°C		UNITS
				MIN	TYP	MAX	MIN	MAX	
HC TYPES									
Propagation Delay Select to Outputs	t_{PHL}, t_{PLH}	C_L = 50pF	2	-	-	275	-	345	ns
			4.5	-	-	55	-	69	ns
		C_L = 15pF	5	-	23	-	-	-	ns
		C_L = 50pF	6	-	-	47	-	59	ns
LE to Outputs	t_{PHL}, t_{PLH}	C_L = 50pF	2	-	-	225	-	280	ns
			4.5	-	-	45	-	56	ns
		C_L = 15pF	5	-	19	-	-	-	ns
		C_L = 50pF	6	-	-	38	-	48	ns
E to Outputs	t_{PHL}, t_{PLH}	C_L = 50pF	2	-	-	175	-	220	ns
			4.5	-	-	35	-	44	ns
		C_L = 15pF	5	-	14	-	-	-	ns
		C_L = 50pF	6	-	-	30	-	37	ns
Output Transition Time	t_{THL}, t_{TLH}	C_L = 50pF	2	-	-	75	-	95	ns
			4.5	-	-	15	-	19	ns
			6	-	-	13	-	16	ns
Input Capacitance	C_{IN}	C_L = 50pF	-	10	-	10	-	10	pF
Power Dissipation Capacitance (Notes 2, 3)	C_{PD}	-	5	-	70	-	-	-	pF

NOTES:
2. C_{PD} is used to determine the dynamic power consumption, per package.
3. $P_D = V_{CC}^2 f_i (C_{PD} + C_L)$ where f_i = Input Frequency, C_L = Output Load Capacitance, V_{CC} = Supply Voltage.

11. TEST CIRCUITS AND WAVEFORMS



NOTE: Outputs should be switching from 10% VCC to 90% VCC in accordance with device truth table. For fMAX, input duty cycle = 50%.

FIGURE 1. HC CLOCK PULSE RISE AND FALL TIMES AND PULSE WIDTH

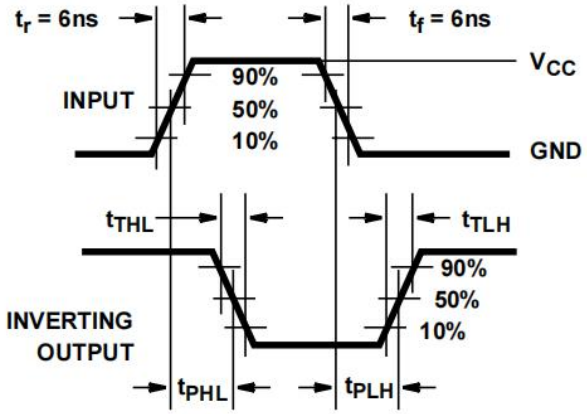


FIGURE 2. HC TRANSITION TIMES AND PROPAGATION DELAY TIMES, COMBINATION LOGIC

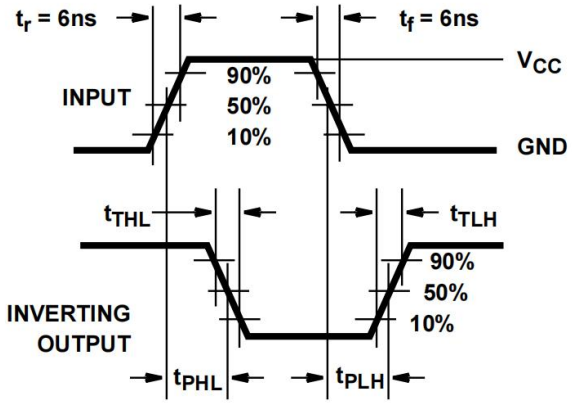


FIGURE 3. HC TRANSITION TIMES AND PROPAGATION DELAY TIMES, COMBINATION LOGIC

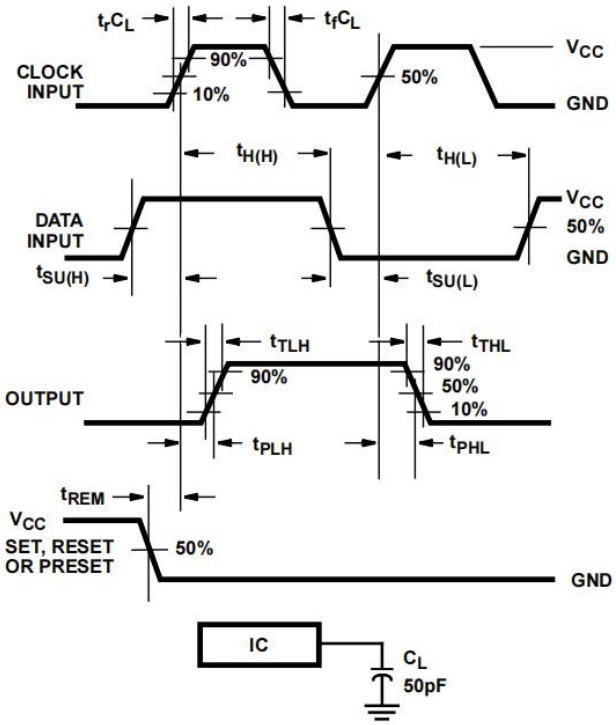


FIGURE 4. HC SETUP TIMES, HOLD TIMES, REMOVAL TIME, AND PROPAGATION DELAY TIMES FOR EDGE TRIGGERED SEQUENTIAL LOGIC CIRCUITS

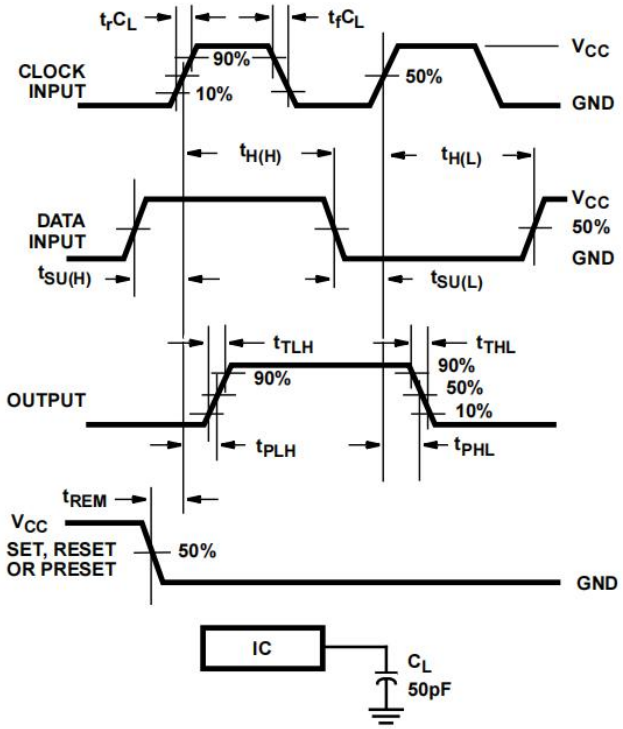


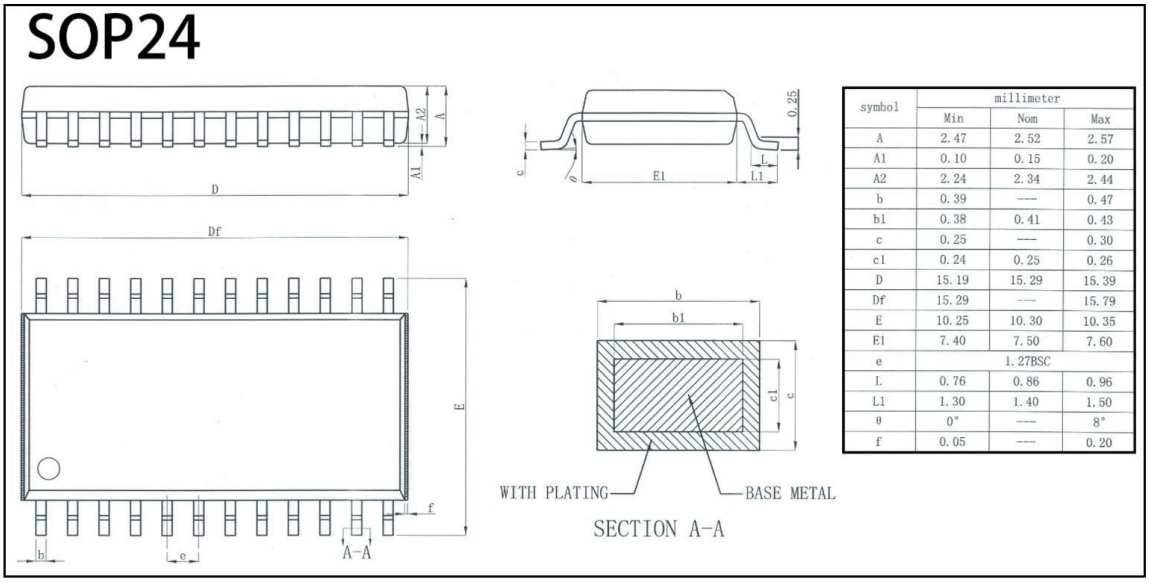
FIGURE 5. HC SETUP TIMES, HOLD TIMES, REMOVAL TIME, AND PROPAGATION DELAY TIMES FOR EDGE TRIGGERED SEQUENTIAL LOGIC CIRCUITS

12. ORDERING INFORMATION

Ordering Information

Part Number	Device Making	Package type	Body size (mm)	Temperate (℃)	MSL	Transpo Rt	Package Quantit
XLCD74HC4515M96	XL4515D	SOP24	15.29 *7.50	-40 to +85	MSL3	T&R	2000

13. DIMENSIONAL DRAWINGS



symbol	millimeter		
	Min	Nom	Max
A	2.47	2.52	2.57
A1	0.10	0.15	0.20
A2	2.24	2.34	2.44
b	0.39	---	0.47
b1	0.38	0.41	0.43
c	0.25	---	0.30
c1	0.24	0.25	0.26
D	15.19	15.29	15.39
Df	15.29	---	15.79
E	10.25	10.30	10.35
E1	7.40	7.50	7.60
e	1.27BSC		
L	0.76	0.86	0.96
L1	1.30	1.40	1.50
θ	0°	---	8°
f	0.05	---	0.20