JW5293/JW5293P

3A, 6V, 1.5MHz

Synchronous Step-Down Converter

DESCRIPTION

The JW5293 and JW5293P are monolithic buck switching regulators based on constant on-time (COT) control for fast transient response. Operating with an input range of 2.7V-6.0V, the JW5293 and JW5293P deliver 3A of continuous output current with integrated P-Channel and N-Channel MOSFETs. The internal synchronous power switches provide high efficiency. At light loads, JW5293 and JW5293P operate in low frequency to maintain high efficiency.

The JW5293 and JW5293P guarantee robustness with hiccup output short-circuit protection, start-up current run-away protection and input under voltage lockout, and thermal protection.

The JW5293 and JW5293P are available in 6-pin SOT563 package, which provides a compact solution with minimal external components.

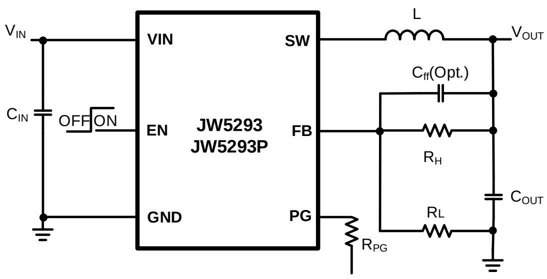
FEATURES

- 2.7V to 6.0V Operating Input Range
- Up to 3A Output Current
- Up to 95% Peak Efficiency
- Very Low Rdson
- High Efficiency at Light Load
- 1% FB Accuracy
- Internal Soft-Start
- 1.5MHz Switching Frequency
- Input Under Voltage Lockout
- Optional Power Good (PG) Function
- Output Discharge
- Pre-bias Soft Start
- Current Run-Away Protection
- Short Circuit Protection
- Thermal Protection
- Available in SOT563 Package

APPLICATIONS

- 5V or 3.3V Point of Load Conversion
- Set Top Boxes
- Telecom/Networking Systems
- Storage Equipment
- GPU/DDR Power Supply

TYPICAL APPLICATION



ORDER INFORMATION

DEVICE[1]	PACKAGE	TOP MARKING[2]	ENVIRONMENTAL[3]
JW5293SOTI#TR	SOT563	JWW☐ YW☐☐	Green
JW5293PSOTI#TR	SOT563	JAG☐ YW☐☐	Green

Notes:

1) JW☐ ☐#TR
- Tape and Reel (If TR is not shown, it means Tube)
- Package Code
- Part No.

2) Line1: J ☐☐☐
- Lot number
- Product code
- JoulWatt LOGO

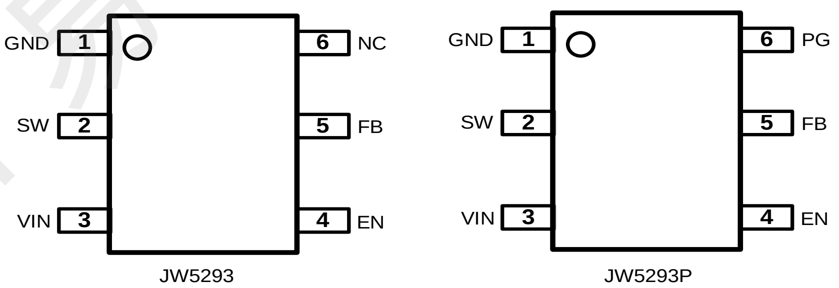
Line2: YW ☐☐
- Lot number
- Week code
- Year code

3) All JoulWatt products are packaged with Pb-free and Halogen-free materials and compliant to RoHS standards.

DEVICE[1]	Function	Package
JW5293SOTI#TR	-	SOT563
JW5293PSOTI#TR	PG	SOT563

PIN CONFIGURATION

TOP VIEW



ABSOLUTE MAXIMUM RATING[1)]

VIN, EN, FB, PG Pins ....-0.3V to 7.0 V
SW Pin………………………………………………………...…-0.3V (-2V for 10ns) to 7V (8.5V for 10ns)
Junction Temperature.[2)] 150ºC
Lead Temperature 260ºC
Storage Temperature .... -65ºC to +150ºC
ESD Susceptibility (Human Body Model) 2kV

RECOMMENDED OPERATING CONDITIONS[3)]

Input Voltage V_{IN} ....2.7V to 6.0V
Output Voltage V_{OUT}...0.6V to VIN
Operating Junction Temperature…..-40ºC to 125ºC

THERMAL PERFORMANCE[4)] θ_{JA} θ_{Jc}

SOT563..145…...45ºC/W

Note:

1) Exceeding these ratings may damage the device. These stress ratings do not imply function operation of the device at any other conditions beyond those indicated under RECOMMENDED OPERATING CONDITIONS.
2) The JW5293 and JW5293P include thermal protection that is intended to protect the device in overload conditions. Continuous operation over the specified absolute maximum operating junction temperature may damage the device.
3) The device is not guaranteed to function outside of its operating conditions.
4) Measured on JESD51-7, 4-layer PCB.

ELECTRICAL CHARACTERISTICS

VIN=5V, T_A=25℃, unless otherwise stated.

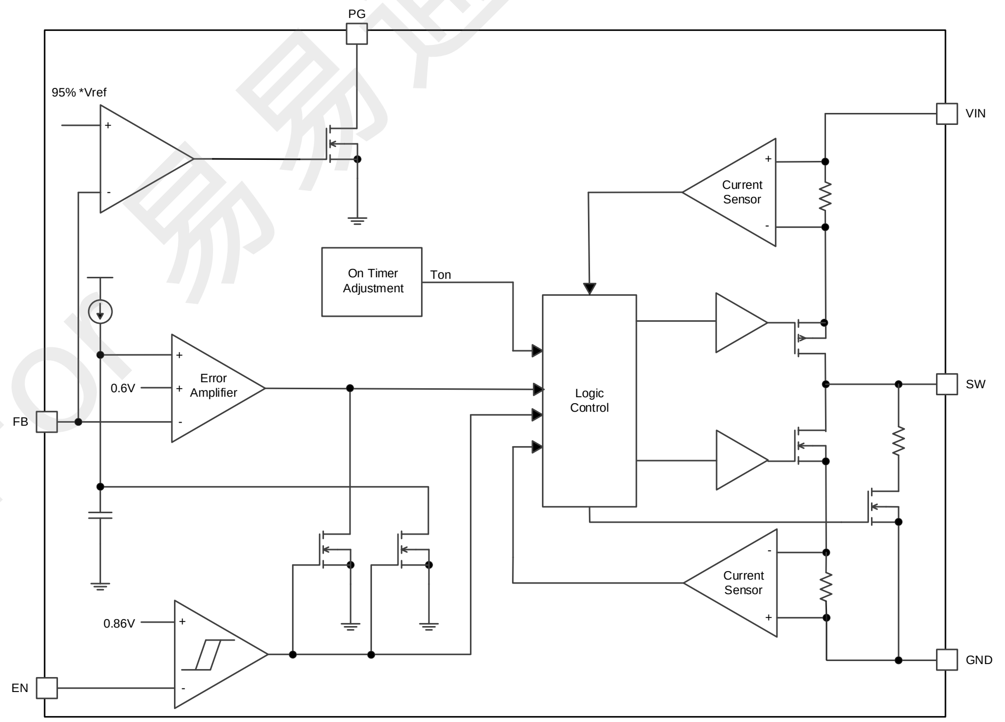
Item	Symbol	Condition	Min.	Typ.	Max.	Units
V_{IN} Under Voltage Lockout Threshold	V_{IN_UVLO}	V_{IN} rising		2.3	2.5	V
V_{IN} Under Voltage Lockout Hysteresis	$V_{IN\_UVLO\_HYST}$	V_{IN} falling		200		mV
EN Rising Threshold	V_{EN_H}	V_{EN} rising, FB=0.3V		0.86	1.2	V
EN Falling Threshold	V_{EN_L}	V_{EN} falling, FB=0.3V	0.4	0.6		V
Shutdown Current	I_{SHDN}	V_{IN}=6.0V, V_{EN}=0V		0.1	1	μA
Quiescent Current	I_Q	V_{EN}=5V, I_{OUT}=0A, V_{FB}=V_{REF}*105%		55	85	μA
Regulated Feedback Voltage	V_{FB}	2.7V<V_{IN}<6.0V	0.594	0.6	0.606	V
		T_j=-40 ºC~125 ºC	0.588	0.6	0.612	V
FB Leakage Current	I_{FB}	V_{FB}=0.7V			100	nA
PFET On Resistance	R_{DSON_P}			46		mΩ
NFET On Resistance	R_{DSON_N}			26		mΩ
PFET Leakage Current	I_{LEAK_P}	V_{IN}=6.0V, V_{EN}=0V, V_{SW}=0V			1	uA
NFET Leakage Current	I_{LEAK_N}	V_{IN}=6.0V, V_{EN}=0V, V_{SW}=6.0V			1	uA
PFET Current Limit	I_{LIM_TOP}		3.8	5	6.2	A
NFET Current Limit	I_{LIM_BOT}		3	4	5	A
Switch Frequency	F_{SW}	CCM	1.2	1.5	1.8	MHz
Minimum On Time[5)]	T_{ON_MIN}			80		ns
Minimum Off Time[5)]	T_{OFF_MIN}			120		ns
Maximum Duty Cycle[5)]	D_{MAX}			100		%
Soft-Start Period	T_{SS}	10% to 90% V_{ref}		0.63		ms
Output Discharge Resistor	R_{DIS}			40		Ω
Power Good Threshold	V_{PG_H}	V_{FB} rising, referenced to V_{FB} nominal (JW5293P)	90%	95%	99%	
	V_{PG_L}	V_{FB} falling, referenced to V_{FB} nominal (JW5293P)	85%	90%	95%	
Power Good Delay Time	T_{PG_Delay}	(JW5293P)		40		us
Low-Level Output Voltage at PG Pin	V_{PG_OL}	I_{PG}= 1 mA (JW5293P)			0.4	V
Thermal Shutdown Threshold[5)]	T_{SHDN}			160		℃
Thermal Shutdown Hysteresis	T_{HYST}			20		℃

Note: (5) Guaranteed by design

PIN DESCRIPTION

JW5293 Pin	JW5293P Pin	Name	Description
1	1	GND	Ground pin.
2	2	SW	SW is the switching node that supplies power to the output. Connect the output LC filter from SW to the output load.
3	3	VIN	Input voltage pin. VIN supplies power to the IC. Connect a 2.7V to 6.0V supply to VIN and bypass VIN to GND with a suitably large capacitor to eliminate noise on the input to the IC.
4	4	EN	Drive EN pin high to turn on the regulator and low to turn off the regulator.
5	5	FB	Output feedback pin. FB senses the output voltage and is regulated by the control loop to 0.6V. Connect a resistive divider at FB.
	6	PG	Open drain output. Connect a 10KΩ resistor from PG to VIN. If it's not used, leave the pin floating.
6		NC	

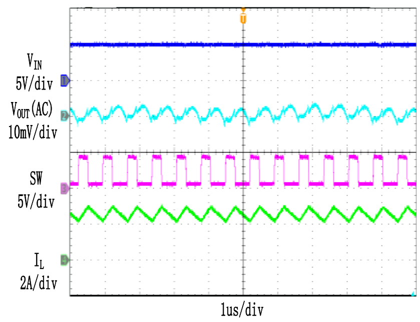
BLOCK DIAGRAM



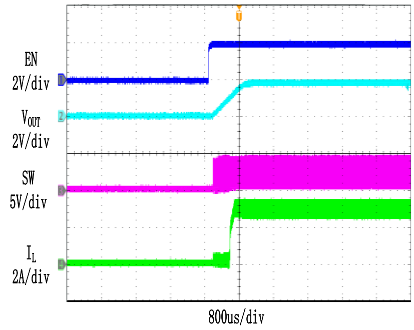
TYPICAL PERFORMANCE CHARACTERISTICS(JW5293/JW5293P)

V_{IN} =5V, V_{OUT} = 1.8V, C_{OUT} = 22μF, T_A = +25°C, unless otherwise noted

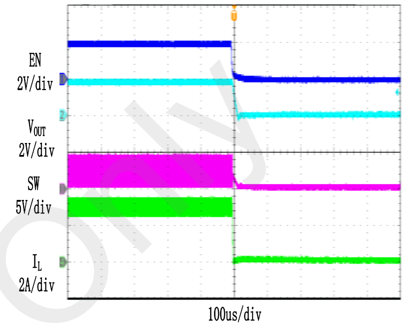
Steady State Test
V_{IN}=5V, V_{OUT}=1.8V
I_{OUT}=3A



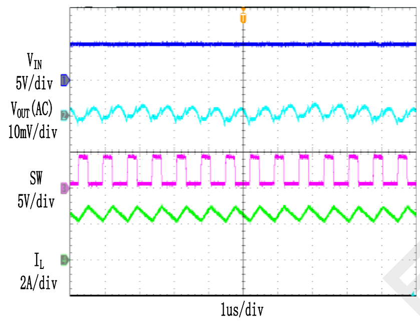
Startup through Enable
V_{IN}=5V, V_{OUT}=1.8V
I_{OUT}=3A (Eload)



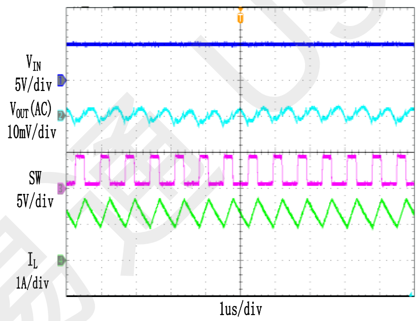
Shutdown through Enable
V_{IN}=5V, V_{OUT}=1.8V
I_{OUT}=3A (Eload)



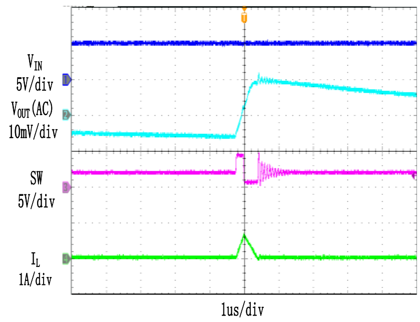
Heavy Load Operation
3A LOAD



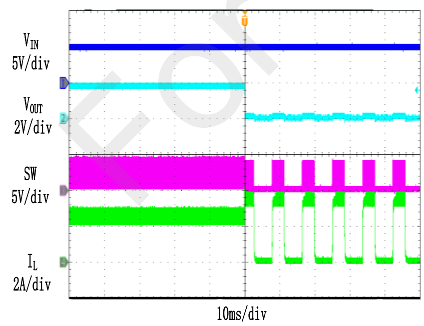
Medium Load Operation
1.5A LOAD



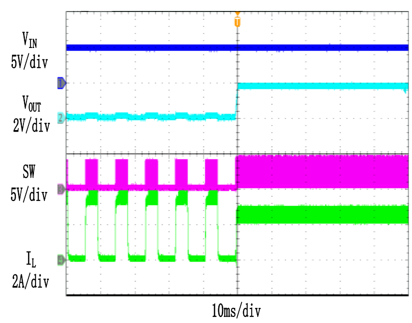
Light Load Operation
0A LOAD



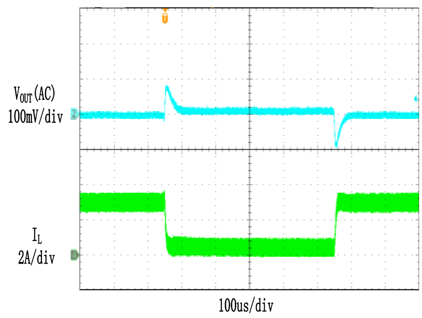
Short Circuit Protection
V_{IN}=5V, V_{OUT}=1.8V
I_{OUT}=3A - Short



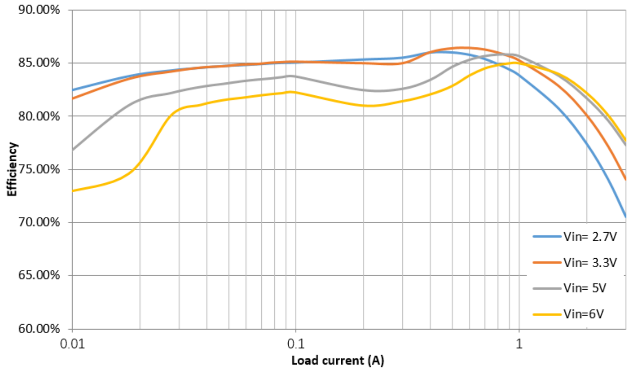
Short Circuit Recovery
V_{IN}=5V, V_{OUT}=1.8V
I_{OUT}=Short-3A



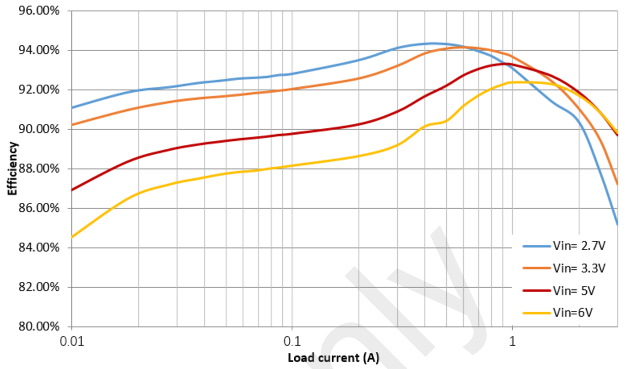
Load Transient
C_{ff}=NC
0.3A LOAD → 3A LOAD → 0.3A LOAD



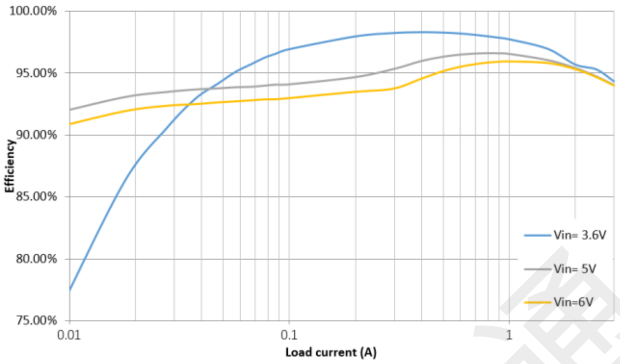
TYPICAL PERFORMANCE CHARACTERISTICS(JW5293/JW5293P)



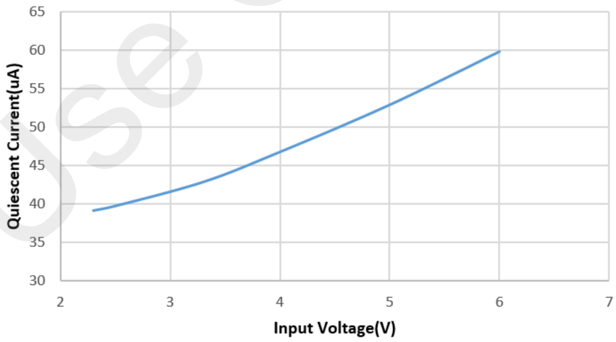
Efficiency vs Load Current
(V_{OUT}=0.6V)



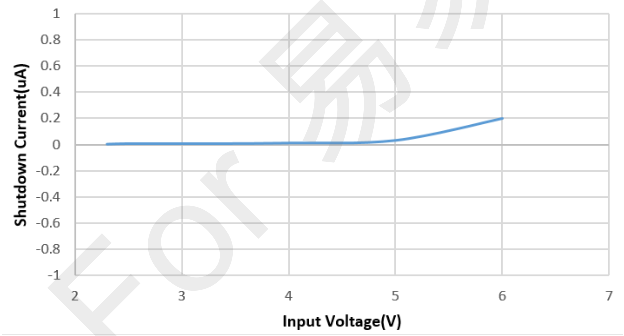
Efficiency vs Load Current
(V_{OUT}=1.8V)



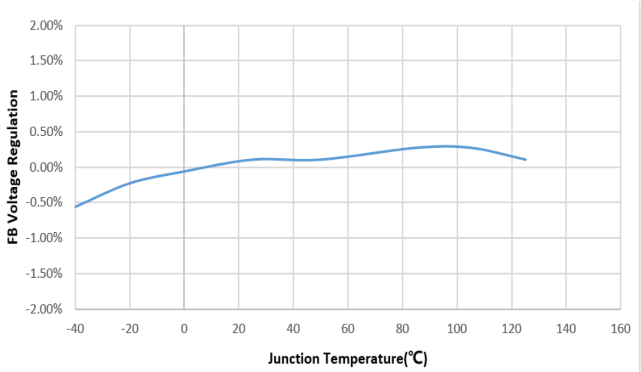
Efficiency vs Load Current
(V_{OUT}=3.3V)



Quiescent Current vs Input Voltage

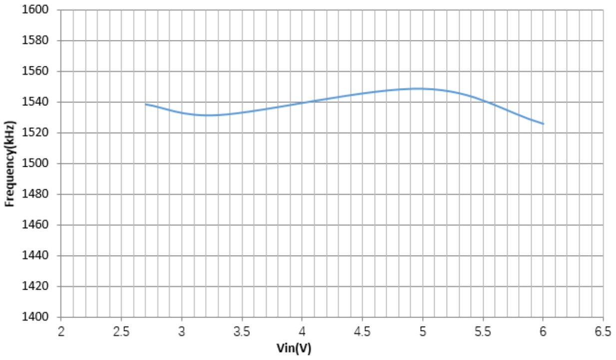


Shutdown Current vs Input Voltage

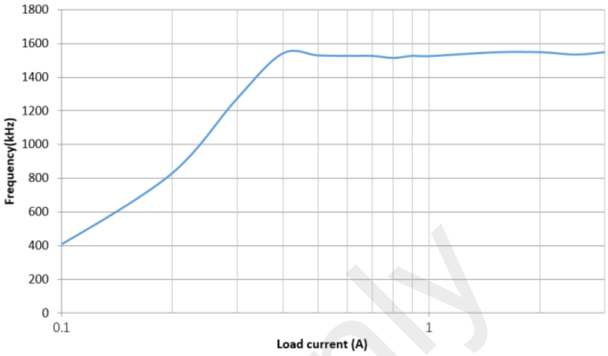


FB Voltage Regulation vs Junction Temperature

TYPICAL PERFORMANCE CHARACTERISTICS(JW5293/JW5293P)



Switching Frequency vs Input Voltage
(V_{OUT}=1.8V, I_{OUT}=1.5A)



Switching Frequency vs Load Current
(V_{OUT}=1.8V, V_{IN}=5V)

FUNCTIONAL DESCRIPTION

The JW5293 and JW5293P are constant on-time control, synchronous, step-down regulators. They regulate input voltages from 2.7V~6.0V down to an output voltage as low as 0.6V, and are capable of supplying up to 3A of load current.

Constant On-time Control

The JW5293 and JW5293P utilize constant on-time control to regulate the output voltage. The output voltage is measured at the FB pin through a resistive voltage divider and the error is amplified by the internal transconductance error amplifier.

Output of the internal error amplifier is compared with the switch current measured internally to control the output current limit.

Soft-Start and Pre-bias Soft Start

Soft-start is designed in the JW5293 and JW5293P to prevent the converter output voltage from overshooting during startup and short-circuit recovery. An internal current source is designed to charge the internal soft-start capacitor and generates a soft-start (SS) voltage. When it is less than internal reference voltage (V_{REF}, typ. 0.6V), SS voltage overrides V_{REF} and the error amplifier uses SS voltage as the reference. When SS exceeds V_{REF}, V_{REF} regains control. The typical soft start time (10% to 90%) T_{SS} is about 630us.

If the output capacitor is pre-biased at startup, the device initiates switching and starts ramping up only after the internal reference voltage exceeds the sensed output voltage at FB. This scheme ensures that the converters ramp up smoothly into regulation point.

PFM Mode

The JW5293 and JW5293P operate in PFM mode at light load. In PFM mode, switch frequency is continuously controlled in proportion to the load current, i.e. switch frequency decreases when load current drops to boost power efficiency at light load by reducing switch-loss, while switch frequency increases when load current rises, minimizing output voltage ripples.

Shut-Down Mode

The JW5293 and JW5293P operate in shut-down mode when voltage at EN pin is driven below 0.4V. In shut-down mode, the entire regulator is off and the supply current consumed by the IC drops below 1uA.

Output Voltage Discharge

The JW5293 and JW5293P enable the output voltage discharge mode. This causes both the high side MOSFET and the low side MOSFET to latch off. A discharge FET connected between SW and GND is turned on to discharges the output VOUT when the Vin pin voltage below the UVLO or the EN pin voltage is below the turn-on threshold. The typical switch on resistance of this FET is about 40Ω.

Power Switches

P-channel and N-channel MOSFET switches are integrated on the JW5293 and JW5293P to down convert the input voltage to the regulated output voltage.

Short Circuit Protection

When output is shorted to ground, the switching frequency is reduced to prevent the inductor current from increasing beyond PFET current limit. If short circuit condition holds for more than 1024 cycles, both PFET and NFET are forced off and can be enabled again after 5ms. This procedure is repeated as long as short circuit condition is not removed.

Power Good

JW5293P have built in power good (PG) function to indicator whether the output voltage has reached its appropriate level or not. The PG pin goes high impedance once the output is above 95% of the nominal voltage, and is driven low once the output voltage falls below typically 90% of the nominal voltage. The PG signal can be used for startup sequencing for multiple rails. The PG pin is an open drain output. JW5293P features PG=Low when the device is turned-off due to EN=Low, UVLO and thermal shutdown.

Thermal Protection

When the temperature of the IC rises above 160°C, it is forced into thermal shut-down. Only when core temperature drops below 140°C can the regulator become active again.

APPLICATION INFORMATION

Output Voltage Set

The output voltage is determined by the resistor divider connected at the FB pin, and the voltage ratio is:

$$V_{FB} = V_{OUT} \cdot \frac{R_L}{R_L + R_H}$$

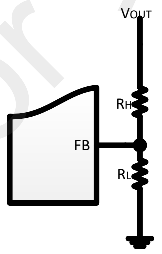
where V_{FB} is the feedback voltage and V_{OUT} is the output voltage.

Choose R_L around 10kΩ, and then R_H can be calculated by:

$$R_H = R_L \cdot \left(\frac{V_{OUT}}{0.6} - 1 \right)$$

To ensure stability, R_L is not allowed to exceed 50kΩ. The following table lists the recommended values.

V_{OUT} (V)	R_L(kΩ)	R_H(kΩ)
0.8	12	4
1	30	20
1.2	10	10
1.8	10	20
3.3	11	49.9



Input Capacitor

The input capacitor is used to supply the AC input current to the step-down converter and maintaining the DC input voltage. Estimate the RMS current in the input capacitor with:

$$I_{CIN} = I_{LOAD} \cdot \sqrt{\frac{V_{OUT}}{V_{IN}} \cdot \left(1 - \frac{V_{OUT}}{V_{IN}} \right)}$$

where I_{LOAD} is the load current, V_{OUT} is the output voltage, V_{IN} is the input voltage.

The input capacitor can be calculated by the following equation when the input ripple voltage is determined.

$$C_{IN} = \frac{I_{LOAD}}{f_S \cdot \Delta V_{IN}} \cdot \frac{V_{OUT}}{V_{IN}} \cdot \left(1 - \frac{V_{OUT}}{V_{IN}} \right)$$

where C_{IN} is the input capacitance value, fs is the switching frequency, ΔV_{IN} is the input ripple voltage.

The input capacitor can be electrolytic, tantalum or ceramic. To minimizing the potential noise, a small X5R or X7R ceramic capacitor, i.e. 0.1μF, should be placed as close to the IC as possible when using electrolytic capacitors.

A 22uF ceramic capacitor is recommended in typical application.

Output Capacitor

The output capacitor is required to maintain the DC output voltage, and the capacitance value determines the output ripple voltage. The output voltage ripple can be calculated by:

$$\Delta V_{OUT} = \frac{V_{OUT}}{f_S \cdot L} \cdot \left(1 - \frac{V_{OUT}}{V_{IN}} \right) \cdot \left(R_{ESR} + \frac{1}{8 \cdot fs \cdot C_{OUT}} \right)$$

where C_{OUT} is the output capacitance value and R_{ESR} is the equivalent series resistance value of the output capacitor.

The output capacitor can be low ESR electrolytic, tantalum or ceramic, which lower ESR capacitors get lower output ripple voltage.

The output capacitors also affect the system stability and transient response, and 22uF ~

22uFx2 ceramic capacitors are recommended in typical application.

Inductor Selection

The inductor is used to supply constant current to the output load, and the value determines the ripple current which affect the efficiency and the output voltage ripple. The ripple current is typically allowed to be 30% of the maximum output current limit (3A), thus the inductance value can be calculated by:

$$L = \frac{V_{OUT}}{f_S \times \Delta I_L} \times \left(1 - \frac{V_{OUT}}{V_{IN}}\right)$$

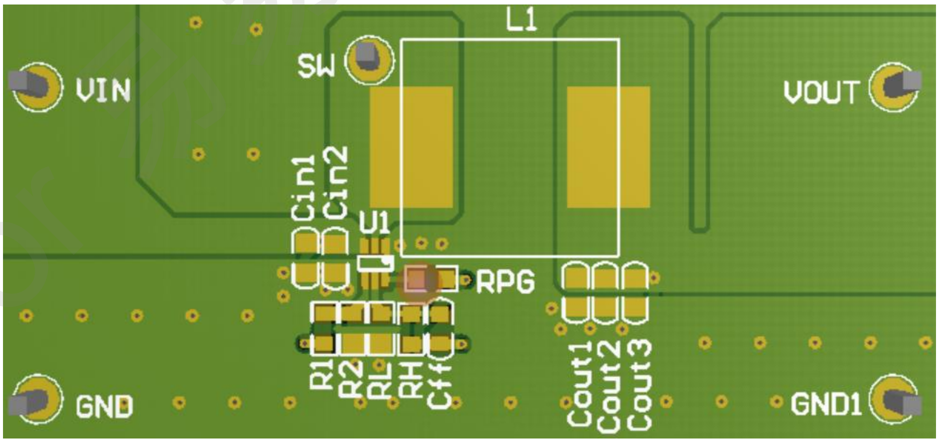
where V_{IN} is the input voltage, V_{OUT} is the output voltage, f_S is the switching frequency, and $\triangle I_L$ is the peak-to-peak inductor ripple current.

PCB Layout Guidelines

For minimum noise problem and best operating performance, the PCB is preferred to following the guidelines as reference.

1. Place the input decoupling capacitor as close to JW5293 series (V_{IN} pin and GND) as possible to eliminate noise at the input pin. The loop area formed by input capacitor and GND must be minimized.
2. Put the feedback trace as short as possible, and far away from the inductor and noisy power traces like SW node.
3. The ground plane on the PCB should be as large as possible for better heat dissipation.
4. Keep the switching node SW short to prevent excessive capacitive coupling.
5. Make V_{IN}, V_{OUT} and ground bus connections as wide as possible. This reduces any voltage drops on the input or output paths of the converter and maximizes efficiency.

SOT563:



PCB Layout Recommendation

REFERENCE DESIGN

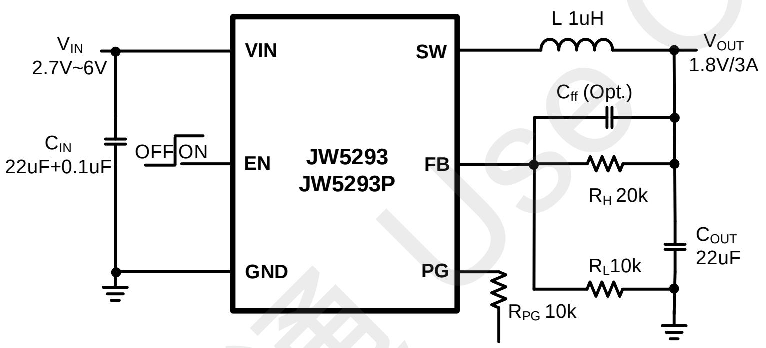
Note: Information in the following reference design sections is not part of JoulWatt component specification. Customers are responsible for determining suitability of components chosen for their purposes and should validate their design implementation to make sure the proper system functionality.

Reference 1:

V_{IN}: 2.7V~6V

V_{OUT}: 1.8V

I_{LOAD}: 0~3A



External Components Suggestion (V_{IN}=5V):

V_{OUT} (V)	R_L (kΩ)	R_H (kΩ)	C_{ff} (pF)	L (μH)	C_{OUT_NOM}(μF)	C_{OUT_EFF} (μF)
0.8	12	4	NC	0.68	44	33
1	30	20	NC	0.68	44	30
1.2	10	10	NC	1	22	15
1.8	10	20	NC	1	22	10
3.3	11	49.9	NC	1.5	22	10

Notes:

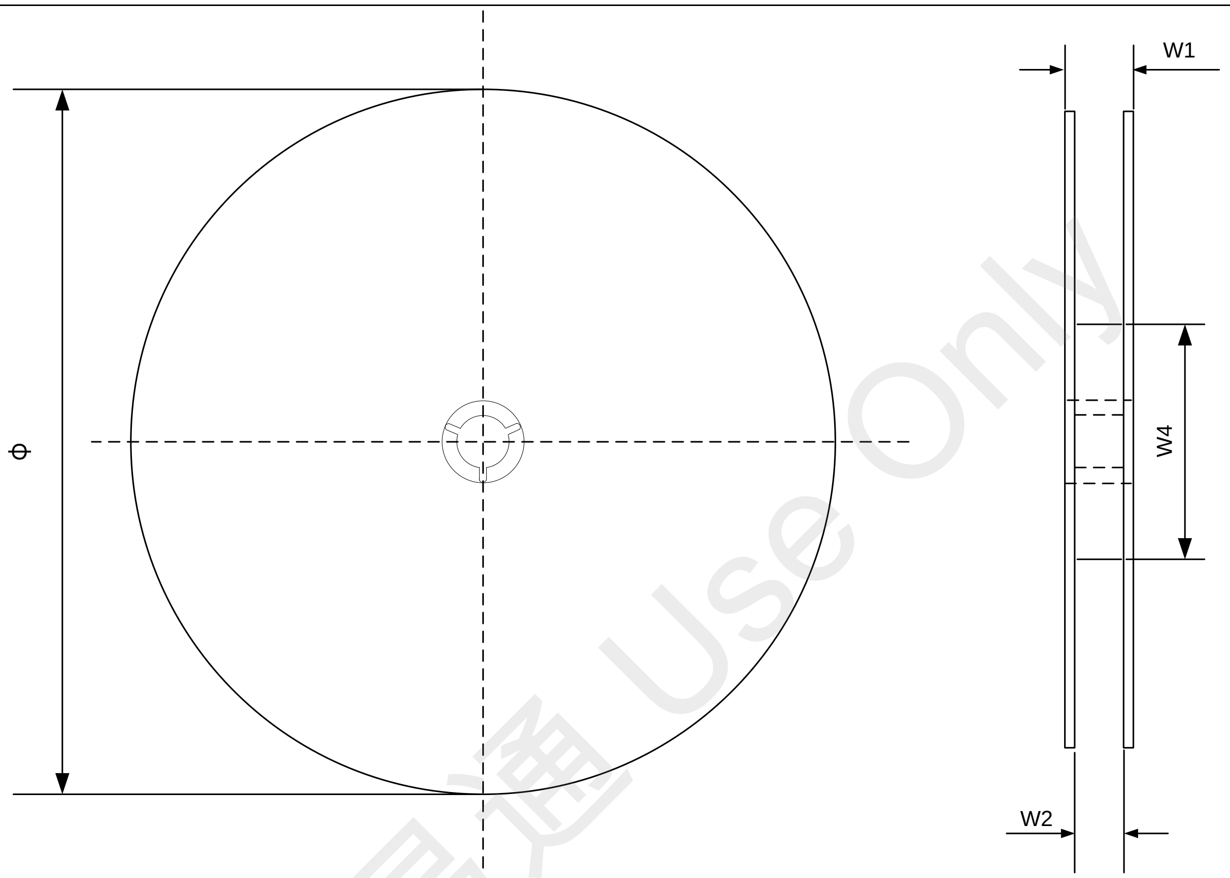
1) In order to improve dynamic performance, a feedforward capacitor (C_{ff}) can be considered to be in parallel with R_H.

2) Capacitor tolerance and bias voltage de-rating should be considered. The effective capacitance can vary by +20% and -80%. Please refer to the datasheet of the capacitor.

3) C_{OUT_NOM} is the minimum nominal capacitance value of C_{OUT} (output capacitance). C_{OUT_EFF} is the minimum effective capacitance value of C_{OUT}.

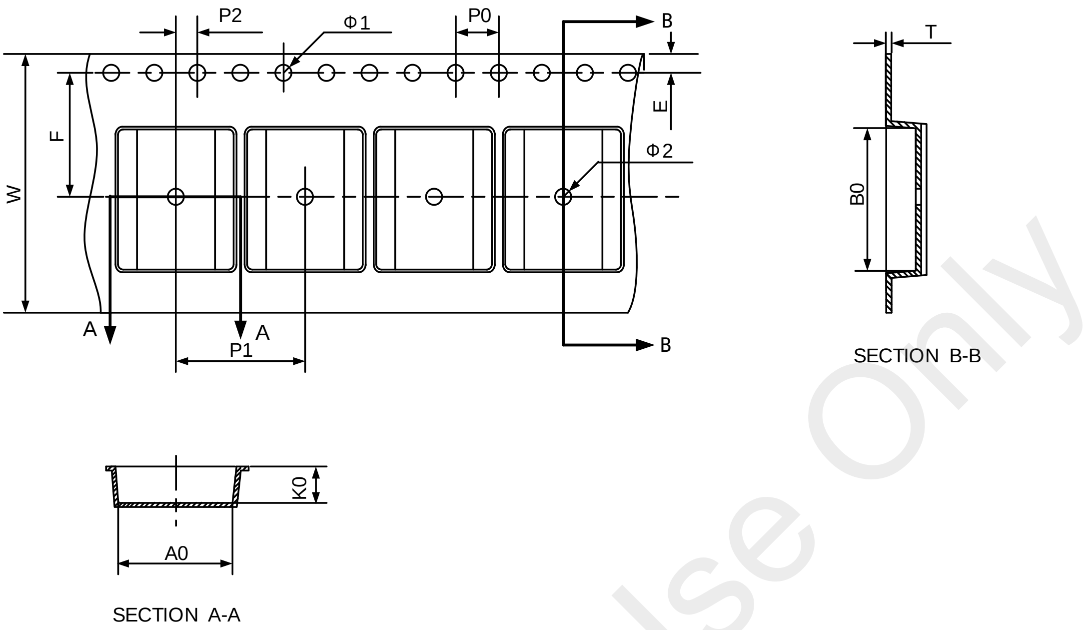
TAPE AND REEL INFORMATION

Reel UNIT: mm



Package	Diameter Φ	Thickness W1	Width W2	W4
SOT563	178±2	12.30±2	9.5±2	58±4

Carrier Tape UNIT: mm



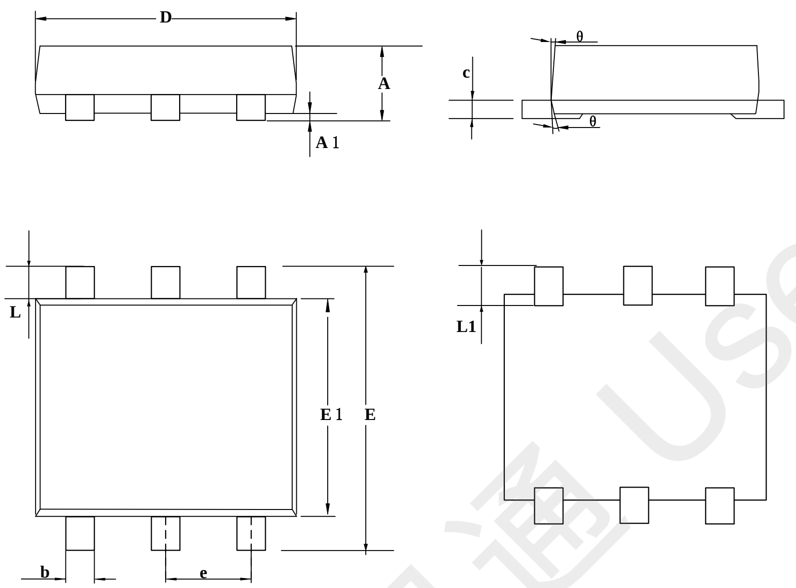
Note：

1) The carrier type is black, and colorless transparent.
2) Carrier camber is within 1mm in 100mm.
3) 10 pocket hole pitch cumulative tolerance:±0.20.
4) All dimensions are in mm.

Package	Tape dimensions（mm）										
	P0	P2	P1	A0	B0	W	T	K0	Φ1	Φ2	E	F
SOT563	4.0±0.1	2.0±0.1	4.0±0.1	1.78±0.3	1.78±0.3	8.0±0.3	0.20±0.2	0.69±0.2	1.50min	0.50±0.10	1.75±0.1	5.50±0.10

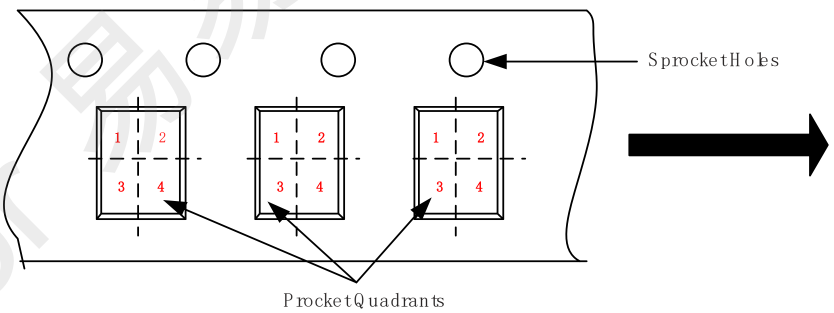
PAKCAGE OUTLINE

SOT563 UNIT: mm



SYMBOL	MILLIMETER		
	MIN	NOM	MAX
A	0.525	—	0.60
A1	0.00	—	0.05
b	0.17	0.22	0.27
c	0.09	—	0.18
D	1.50	1.60	1.70
E	1.50	1.60	1.70
E1	1.10	1.20	1.30
e	0.45	0.50	0.55
L	0.10	0.20	0.30
L1	0.20	0.30	0.4
θ	9°REF		

QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



Package Type	Pin1 Quadrant
SOT563	3

IMPORTANT NOTICE

- **Joulwatt Technology Co.,Ltd reserves the right to make modifications, enhancements, improvements, corrections or other changes without further notice to this document and any product described herein.**
- **Any unauthorized redistribution or copy of this document for any purpose is strictly forbidden.**
- **Joulwatt Technology Co.,Ltd does not warrant or accept any liability whatsoever in respect of any products purchased through unauthorized sales channel.**
- **JOULWATT TECHNOLOGY CO.,LTD PROVIDES TECHNICAL AND RELIABILITY DATA (INCLUDING DATASHEETS), DESIGN RESOURCES (INCLUDING REFERENCE DESIGNS), APPLICATION OR OTHER DESIGN ADVICE, SAFETY INFORMATION AND OTHER RESOURCES, AND DISCLAIMS ALL WARRANTIES, EXPRESS AND IMPLIED, INCLUDING WITHOUT LIMITATION ANY IMPLIED WARRANTIES OF MERCHANTABILITY, FITNESS FOR A PARTICULAR PURPOSE OR NON-INFRINGEMENT OF THIRD PARTY INTELLECTUAL PROPERTY RIGHTS.**