YAMAHA

YGV642

VC1H

■ Overview

- YGV642 (also called VC1H) is a pattern graphics controller with integrated VRAM functionality requiring only a few inexpensive external components to build nicely animated GUI display subsystems.
- Conventional graphics controllers require complex and large display control program development efforts, whereas YGV642 simply use a 12-byte parameter to control each graphic pattern attributes—its position, scaling, alpha-values, colors—to do away with most of such efforts. Moreover the host controller does not have to be powerful one to effectively animate GUIs with this device.
- YGV642 supports on-the-fly decompression of sprites and font data which are compressed in Yamaha proprietary algorithm and stored in the SPI flash memory. Less memory is needed for the same graphics quality with this feature.
- YGV642 now supports flash memories with SPI bus and comes in smaller package.

All these features allow this device to be built into the compact LCD display subsystems in car instrument dashboards or any electric appliances, at an affordable cost with a minimum number of additional components.

YAMAHA CORPORATION

YGV642 Catalog
CATALOG No. LSI-4GV642A00
2012.8

■ Features

■ Display Controller

- Display Monitors Supported
  - TFT LCD Panels (with digital RGB) or other display devices with compatible interface
- Screen Resolutions Supported
  - Programmable to NTSC, PAL, QVGA, WQVGA, VGA, WVGA, SVGA, and other resolutions
- Integrated LCD Timing Controller
- Display Plane Layering Architecture
  - Graphic primitives: Sprites (pattern graphics), Lines, and Text
  - Hardware clipping with rectangular windows
  - Up to 341 Layers (layered display planes)
  - Each Layer contains Sprite, or Lines, or Text
  - Alpha blending controls on pixel-by-pixel level
  - Contrast, brightness controls of layered image
  - Macro command sequencer for animating GUI

■ Graphics Primitives

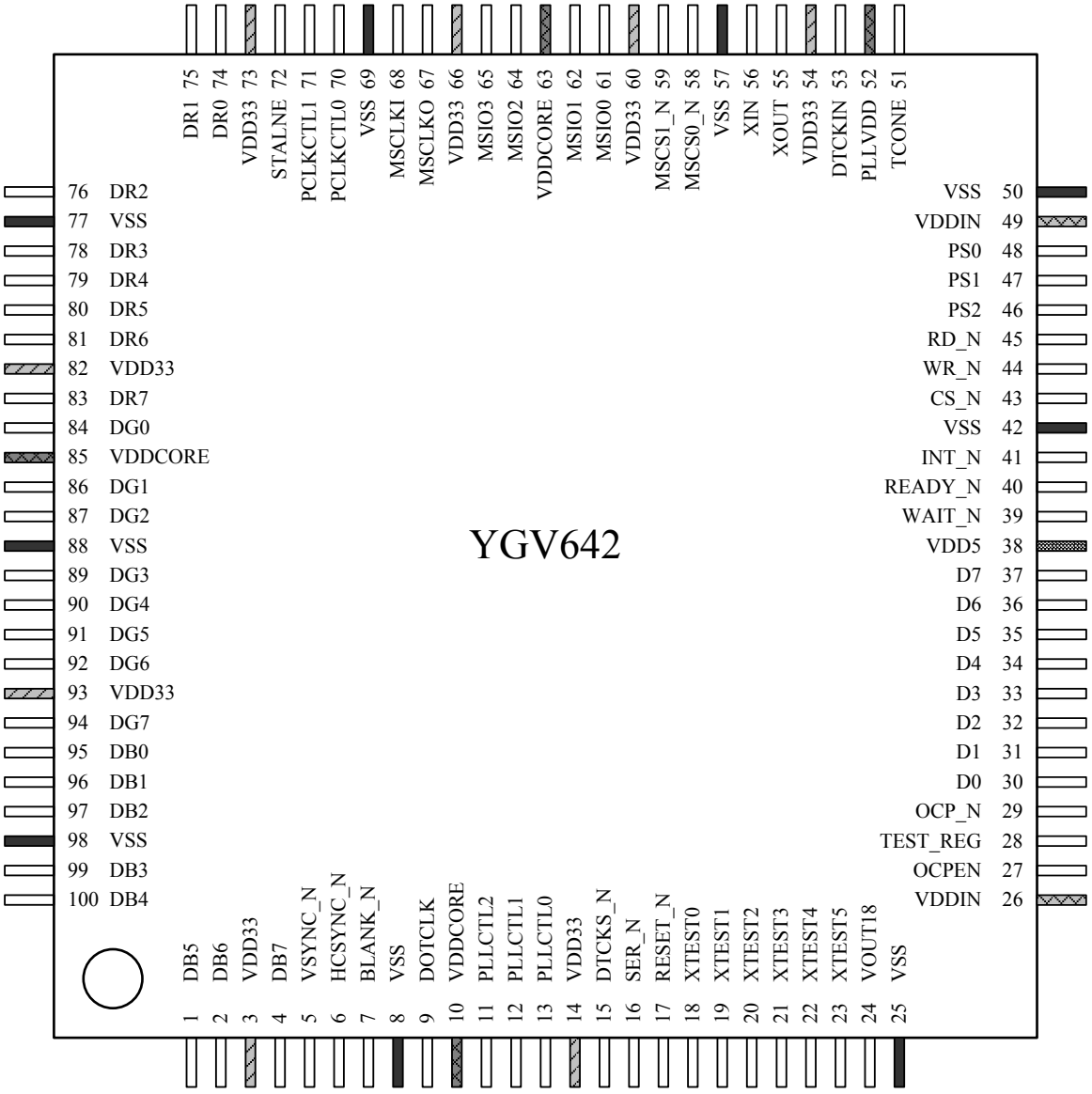
- Sprite
  - Up to 341 Sprites per screen (up to 64 Sprites per scan line)
  - Supports sizes from 8 pixels × 8 pixels to 512 pixels × 512 pixels (horizontal and vertical sizes can be chosen independently in 8 pixel units)
  - Supports color palettes of 2, 16, 64, or 256 colors out of 16M colors; or 262 144 colors with 18-bit RGB; or 16 777 216 colors with 24-bit RGB for photo quality images
  - Image scaling with a 0 to 3.984375 scaling factor (in 0.015625 increments)
  - Anti-aliased Sprite outlines using 4 bpp or 8 bpp Alpha Tables
  - Up to 1024 total palette colors in combinations of 2-color palettes, 16-color palettes, 64-color palettes, and 256-color palettes
- Text
  - Up to 1864 fonts per screen (up to 64 fonts per scan line)
  - Font size from 1 pixel × 1 pixel to 64 pixels × 64 pixels (horizontal and vertical sizes can be chosen independently in 1 pixel units)
  - Independent font selections for each text strings
  - Supports proportional font
  - Inter-character spacing control with kerning
  - Supports half-width font
  - Supports 4 bpp anti-aliasing font
  - Supports font rendering for vertically written texts
- Lines
  - Up to 510 lines per screen
  - Line width from 1 pixel to 16 pixels (in one-pixel increments)
  - Colors selected from 32 768 colors (in RGB555 format) or specified with indices to a palette (16 777 216 colors)
  - Hardware line renderer draws directly from the start- and end-point coordinates (no need to construct lines with pixel patterns)

- ✧ Flat or round cap for start- and end-point of the line
- ✧ Supports anti-aliased line rendering

■ Other Features

- ➢ Host Controller Interface
  - ✧ Serial connection or 8-bit parallel connection
  - ✧ Indirect accesses through a single access port (to built-in registers and tables and to the pattern memory)
- ➢ Pattern Memory Interface
  - ✧ Up to 512 Mbit (64 MB) memory
  - ✧ Supports SPI flash memory: Single, Dual, and Quad I/O modes
- ➢ Other Specifications
  - ✧ Lead-free 100-pin SQFP (YGV642-SZ)
  - ✧ Supply voltage: 3.3 V (with built-in regulator for core power supply (1.8 V))
  - ✧ Host controller interface signaling level: between 3.3 V and 5 V
  - ✧ Operating temperature range from −40 °C to +105 °C

■ Pin Assignment



< 100 pin SQFP Top View >

Figure 1 Pin Assignment.

■ Pin Descriptions

Table 1 Pin Attributes

Category	No.	Pin Name	I/O	Power	Description	Attribute	Drive	Note
Host Controller Interface	30	D0	I/O	VDD5	Data bus ・MSB: D7, LSB: D0	†	4 mA	1 2
	31	D1						
	32	D2						
	33	D3						
	34	D4						
	35	D5						
	36	D6						
	37	D7						
	48	PS0	I	VDD5	Access port select	†		1
	47	PS1						
	46	PS2						
	43	CS_N	I	VDD5	Chip select	†		3
		(SCS_N)			Serial interface chip select			
	45	RD_N	I	VDD5	Data read strobe	†		3
		(SDIN)			Serial interface data input			
	44	WR_N	I	VDD5	Data write strobe	†		3
		(SCLK)			Serial interface clock			
	39	WAIT_N	OT	VDD5	Bus wait	†	4 mA	3 4 5
		(SDOUT)			Serial interface data output			2 3
	40	READY_N	OT	VDD5	Bus ready	†	4 mA	4 5
	41	INT_N	OD	VDD5	Interrupt request	†	4 mA	5
	16	SER_N	I	VDD33	Host controller interface select			6
Pattern Memory Interface	58	MSCS0_N	O	VDD33	Chip select		8 mA	
	59	MSCS1_N	O	VDD33	Chip select		8 mA	7
	67	MSCLKO	O	VDD33	Clock output		16 mA	8
	68	MSCLKI	I	VDD33	Clock input			8 9
	61	MSIO0	I/O	VDD33	Pattern Memory data input and output ・MSB: MSIO3, LSB: MSIO0		8 mA	2
	62	MSIO1						
	64	MSIO2						
	65	MSIO3						

Category	No.	Pin Name	I/O	Power	Description	Attribute	Drive	Note
Monitor Interface	74	DR0	O	VDD33	Digital video Red output ・MSB: DR7, LSB: DR0		4 mA	10
	75	DR1						
	76	DR2						
	78	DR3						
	79	DR4						
	80	DR5						
	81	DR6						
	83	DR7						
	84	DG0	O	VDD33	Digital video Green output ・MSB: DG7, LSB: DG0		4 mA	10
	86	DG1						
	87	DG2						
	89	DG3						
	90	DG4						
	91	DG5						
	92	DG6						
	94	DG7						
	95	DB0	O	VDD33	Digital video Blue output ・MSB: DB7, LSB: DB0		4 mA	10
	96	DB1						
	97	DB2						
	99	DB3						
	100	DB4						
	1	DB5						
	2	DB6						
	4	DB7						
	5	VSYNC_N	OT	VDD33	Vertical sync output		4 mA	3
		(POL)			Polarity reverse output			11
	6	HCSYNC_N	OT	VDD33	Horizontal sync signal or composite sync signal output		4 mA	3 11
		(CLKV)			Vertical clock output			
	7	BLANK_N	OT	VDD33	Blanking signal output		4 mA	3
		(STARTV)			Vertical start signal output			11
	9	DOTCLK	O	VDD33	Dot clock output		4 mA	
	(12)	(STARTH)	I/O	VDD33	Horizontal start signal output		4 mA	3 11
	(11)	(LOADH)	I/O	VDD33	Horizontal load signal output		4 mA	3 11
	(13)	(OUTENV)	I/O	VDD33	Gate driver output enable		4 mA	3 11
	51	TCONE	I	VDD33	Timing controller function select (internally pulled down)			12 13
Clock	56	XIN	I	VDD33	Reference clock input			14
	55	XOUT	O	VDD33	For resonator device connection			14
	53	DTCKIN	I	VDD33	Dot clock input			15
	15	DTCKS_N	I	VDD33	Dot clock select			12
	13	PLLCTL0 (OUTENV)	I/O	VDD33	PLL controls			3 12
	12	PLLCTL1 (STARTH)						
	11	PLLCTL2 (LOADH)						
	70	PCLKCTL0	I	VDD33	PLL controls (for initial values on reset) (internally pulled down)			12 13
	71	PCLKCTL1 (STALNM)						3 12 13

Category	No.	Pin Name	I/O	Power	Description	Attribute	Drive	Note
System	17	RESET_N	I$	VDD33	Hardware reset input	‡		
	18	XTEST0	OT	VDD33	Test pin		4 mA	3
		(WP_SDOUT)			Pattern Memory program serial data output			16
	19	XTEST1	I	VDD33	Test pin	‡		3
		(WP_SCS_N)			Pattern Memory program serial chip select			17
	20	XTEST2			Test pin			
		(WP_SDIN)			Pattern Memory program serial data input			
	21	XTEST3			Test pin			
		(WP_SCLK)			Pattern Memory program serial clock			
	22	XTEST4	I	VDD33	Test pin			17
	23	XTEST5						
	(71)	(STALNM)	I	VDD33	Pattern Memory width select (for stand-alone mode) (internally pulled down)			3 12 13
	72	STALNE	I	VDD33	Stand-alone mode selection (internally pulled down)			12 13
	3	VDD33	−	−	Digital power supply			18
	14	VDD33						
	54	VDD33						
	60	VDD33						
	66	VDD33						
	73	VDD33						
	82	VDD33						
	93	VDD33						
	38	VDD5	−	−	Host controller interface power supply ・Supports from 3.3 V to 5 V as the controller interface signaling voltage			19
	8	VSS	−	−	Digital ground			18
	25	VSS						20
	42	VSS						
	50	VSS						
	57	VSS						
	69	VSS						
	77	VSS						
	88	VSS						
	98	VSS						
	52	PLLVDD	−	−	PLL power supply			20
	27	OCPEN	I	VDD5	Overcurrent protect enable/disable/reset	†		
	28	TEST_REG	I	VDD5	Overcurrent protect test pin	†		21
	29	OCP_N	O	VDD5	Overcurrent detect indication		4 mA	
	10	VDDCORE	−	VDDIN	Core supply decoupling capacitor connection			22
	63	VDDCORE						
	85	VDDCORE						
	24	VOUT18	−	VDDIN	1.8 V digital power supply			20
	26	VDDIN	−	−	3.3 V supply for core supply regulator (1.8 V)			18
	49	VDDIN						

* Symbols in I/O column

- ・I: Input
- ・I/O: Input and Output
- ・I$: Input with Schmitt trigger input
- ・O: Output
- ・OT: 3-state output
- ・OD: Open-drain output

* Symbols in Attribute column
  - †: "5 V Tolerant"
    These pins withstand the application of up to 5 V signals beyond the power rail.
    This means that 5 V can be applied when the device power pin is at 0 V.
  - ‡: "Tolerant"
    These pins withstand, and not draw current even when the applied signal is beyond the power rail.
    This is slightly different from the "5 V Tolerant" attribute in that the extent beyond the power rail must be 3.6 V or less. This means that only up to 3.6 V (the maximum operating voltage supply) can be applied when the device is unpowered (at 0 V supply voltage).

[Note 1]
Parallel bus interface is used when SER_N = H.
Fix these pins to "H" or "L" level when SER_N = L.

[Note 2]
Pull up these pins with a resistor.

[Note 3]
Multi function pins.

[Note 4]
Use READY_N and WAIT_N pins as appropriate to the used controller interface timing.

[Note 5]
Pull up these pins with a resistor when used.
(No pull-up resistor is required when these pins are not used.)

[Note 6]
The voltage must be settled to a valid logic level while RESET_N = L on device power-up.
- SER_N = L: serial interface
- SER_N = H: parallel interface

[Note 7]
Leave this pin unconnected (N.C.) when not used.

[Note 8]

Circuit Board Layout Notes:

- Place SPI flash memories as close to YGV642 as possible.
- Place a series 30−100 ohm damping resistor on MSCLKO signal near MSCLKO pin.
- Values of MSCLKO series resistor for the MSCLKI connection and for the SPI flash memory connections must be the same.
- Lengths of MSCLKO signal trace for the MSCLKI connection and for the SPI flash memory connections must be the same.

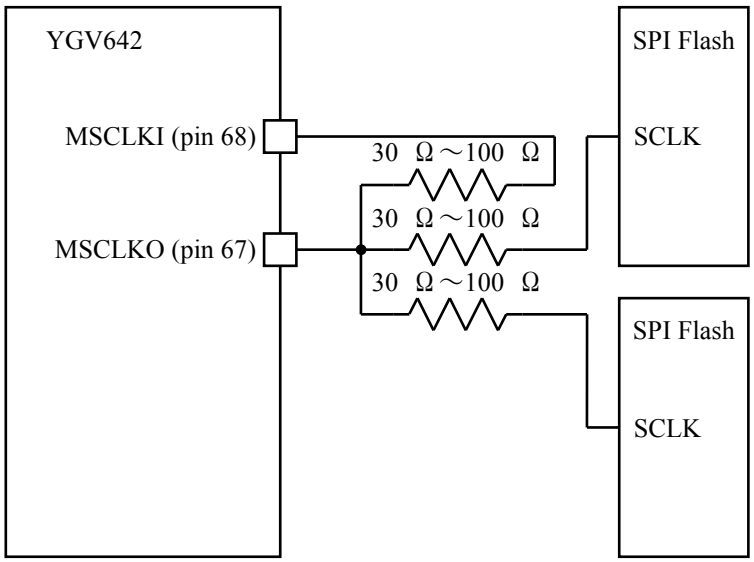


Figure 2 Series Damping Resistors on MSCLKO signal.

[Note 9]

Connect this pin to MSCLKO pin.

[Note 10]

Leave DR1-0, DG1-0, and DB1-0 pins unconnected (N.C.) when using 6 bit data for each RGB video output.

[Note 11]

These pins are in the high-impedance state on device reset until R#1Ch: SYEN becomes "1". Check your LCD specifications to see if pull-down or pull-up resistors are needed on these connections.

[Note 12]

The voltage must be settled to a valid logic level while RESET_N = L on device power-up.

[Note 13]

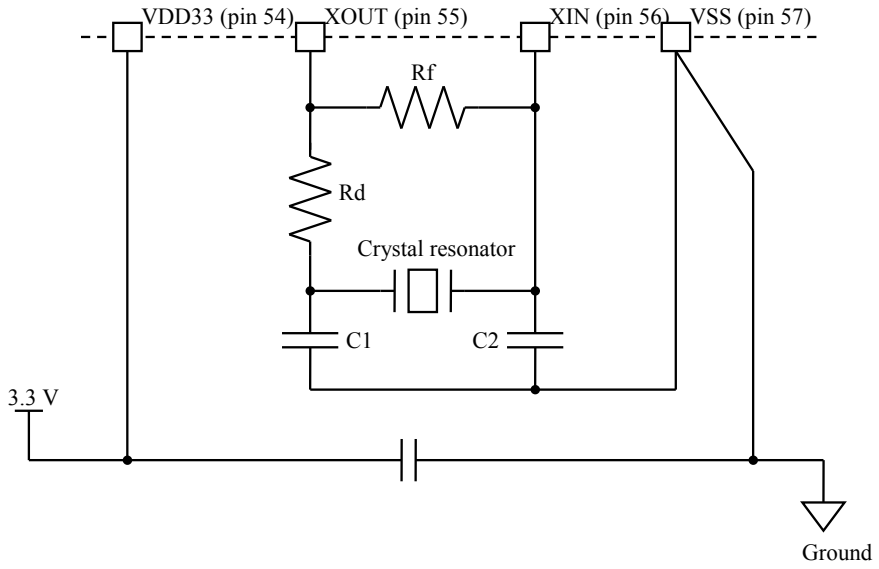
Tie this pin directly to ground to signal logic low although a pull-down resistor is integrated. Tie this pin directly to VDD33 to signal logic high.

[Note 14]

Clocks can be supplied either by connecting a crystal resonator between XIN and XOUT pins to use the on-chip oscillator or by feeding external clock to XIN pin. When external clock is fed, XOUT pin must be left open.

- Supported frequency range of the crystal on XIN and XOUT: 6 MHz to 20 MHz
- Supported frequency range of external clock input to XIN: 6 MHz to 40 MHz

The schematic below shows an external component network when a crystal is used for the clock supply.



C1, C2: Load capacitance, Rf: Feedback resistor, Rd: Damping resistor

Figure 3 External Network for XIN / XOUT.

For the reliable operation of the crystal oscillator circuit, we recommend you to take the following design considerations.

1) Place and connect all the components (such as this device, crystal resonator, etc.) as close to each other as possible with short signal traces.
2) The ground node of the external network must be directly connected to VSS (pin 57) pin.
3) Locate other signal traces as far away as possible from this one, particularly those in which a large current can flow.
4) Use decoupling capacitors between VDD33 (pin 54) and VSS (pin 57).
5) Design wide ground traces around the external network to prevent interference from other signals and connect it to VSS (pin 57).

YGV642 electrical characteristics are specified on the assumption that either a crystal resonator (XIN/XOUT) or an external crystal oscillator (XIN) is used. Whenever possible, therefore use one of these crystal-based clock generators and design so that the frequency tolerance comes within ±100 ppm including its temperature induced variations.

When a ceramic resonator is used, note the following:

1. Find and use a ceramic resonator with jitter performance comparable to those of crystal resonators.
2. Ceramic resonator's frequency tolerance and temperature coefficient are generally larger than those of crystal resonators.

Larger frequency tolerance of components such as ceramic resonators are not considered in the YGV642 design; therefore, use a ceramic resonator with a slightly lower nominal frequency than the designed value so that the system clock frequency remain within the specification even at the upper end of the variation.

[Note 15]
Fix this pin either to logic high or low when DTCKS_N = H.

[Note 16]
Pull up this pin with a resistor when designing an application board that runs both normal operations and Pattern Memory program operations. Leave this pin open when it runs only normal operations.

[Note 17]
For normal operations, XTEST5-1 pins must be tied to "HHHHH", or XTEST5-4 pins be tied to "HL" for Pattern Memory program operations. Other setting may damage this device and devices connected to this one.
Pull up XTEST4-1 pins with a resistor when designing an application board that runs both normal operations and Pattern Memory program operations; pull up XTEST5-1 pins toVDD33 without a resistor when it runs only normal operations.

[Note 18]
Use high-frequency ceramic capacitors across VDD33 and VSS pins and across VDDIN and VSS pins, and place them very near to the IC to minimize wiring inductance.

[Note 19]
Put decoupling capacitors across VDD5 and VSS pins.

[Note 20]
- Connect PLLVDD pin to VOUT18 pin.
- Put a decoupling capacitor across PLLVDD and VSS (pin 50).
  - Place the capacitor as close to PLLVDD pin as possible.
- Put a 1 μF or more ceramic capacitor across VOUT18 and ground.
  - Place the capacitor as close to VOUT18 pin as possible.

[Note 21]
Connect this pin to ground directly, without a resistor.

[Note 22]
- Put a 1 μF or more ceramic capacitor across VDDCORE and ground.
  - Place the capacitor as close to VDDCORE pin as possible.

● Multi-Function Pins

· Host Controller Interface

Table 2 Host Controller Interface

Pin Name	Serial Interface (SER_N = L)	Parallel Interface (SER_N = H)
D7-0	Tie these pins to H or L level	D7-0
PS2-0	Tie these pins to H or L level	PS2-0
CS_N	SCS_N	CS_N
RD_N	SDIN	RD_N
WR_N	SCLK	WR_N
WAIT_N	SDOUT	WAIT_N
READY_N	- (open)	READY_N
INT_N	INT_N	←

· Timing Controller

Table 3 Timing Controller

Pin Name	Timing Controller Disabled (TCONE = L)	Timing Controller Enabled (TCONE = H)
DR7-0	DR7-0	←
DG7-0	DG7-0	←
DB7-0	DB7-0	←
DOTCLK	DOTCLK	←
HCSYNC_N	HCSYNC_N	CLKV
VSYNC_N	VSYNC_N	POL
BLANK_N	BLANK_N	STARTV
PLLCTL2	PLLCTL2	LOADH
PLLCTL1	PLLCTL1	STARTH
PLLCTL0	PLLCTL0	OUTENV

· Pattern Memory Program Serial Interface

Table 4 Pattern Memory Program Serial Interface

Pin Name	For Pattern Memory Program Operations (XTEST5-4 = HL)	For Normal Operations (XTEST5-4 = HH)
XTEST3	WP_SCLK	XTEST3
XTEST2	WP_SDIN	XTEST2
XTEST1	WP_SCS_N	XTEST1
XTEST0	WP_SDOUT	XTEST0

· Stand-Alone Mode

Table 5 Stand-Alone Mode

Pin Name	Normal Mode Pin Function (STALNE = L)	Stand-Alone Mode Pin Function (STALNE = H)
PCLKCTL1	PCLKCTL1	STALNM
PCLKCTL0	PCLKCTL0	Ignored

■ Block Diagram

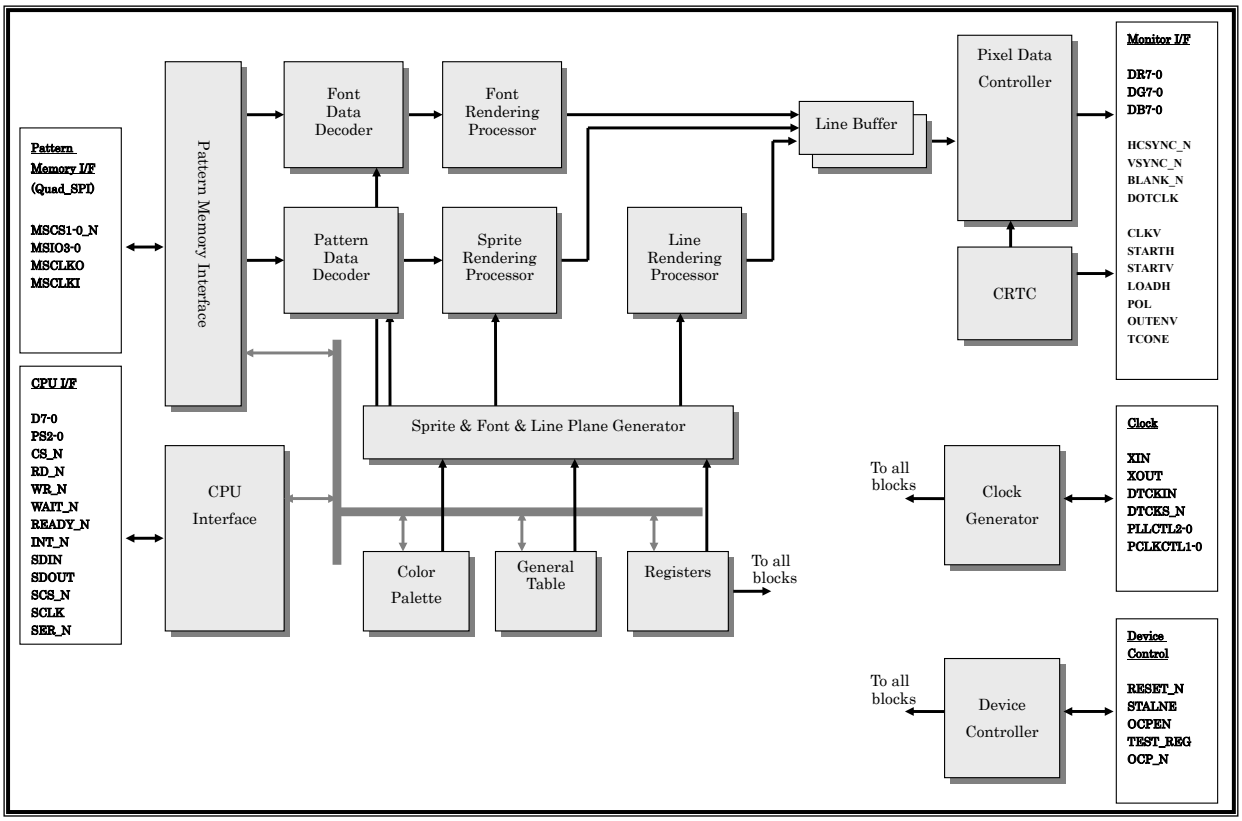


Figure 4 Block Diagram.

■ Electrical Characteristics

● Absolute Maximum Ratings

Table 6 Absolute Maximum Ratings

Parameter	Symbol	Ratings	Unit	Note
Supply voltage (VDD5)	V_{DD5}	−0.5 to +7.0	V	1
Supply voltage (VDD33, VDDIN)	V_{DD33}	−0.5 to +4.6	V	1
PLL supply voltage (PLLVDD)	V_{PLVD}	−0.5 to +2.5	V	1
Input pin voltage (for pins supplied from VDD5)	V_I	−0.5 to +7.0	V	1
Input pin voltage (for RESET_N)	V_I	−0.5 to VDD33+4.6 (≤ 5.5 Max.)	V	1
Input pin voltage (for pins supplied from VDD33 except RESET_N)	V_I	−0.5 to VDD33+0.5 (≤ 4.6 Max.)	V	1
Output pin voltage ("Tolerant" output (including I/O) pins supplied from VDD5)	V_O	−0.5 to +5.5	V	1
Output pin voltage (for pins supplied from VDD5 except the pins above)	V_O	−0.5 to VDD5+0.5 (≤ 5.5 Max.)	V	1
Output pin voltage (for pins supplied from VDD33 including I/O pins)	V_O	−0.5 to VDD33+0.5 (≤ 4.6 Max.)	V	1
Input pin current	I_I	−20 to +20	mA	
Output pin current	I_O	−20 to +20	mA	
Storage temperature	T_{STG}	−50 to +125	°C	

[Note 1] Values are specified using VSS (ground) = 0 V as the reference.

● Recommended Operating Conditions

Table 7 Recommended Operating Conditions

Parameter	Symbol	Min.	Typ.	Max.	Unit	Note
Supply voltage (VDD33, VDDIN)	V_{DD33}	3.0	3.3	3.6	V	1
PLL supply voltage (PLLVDD)	V_{PLVD}	1.65	1.8	1.95	V	1, 2
Controller I/F supply voltage (VDD5)	V_{DD5}	3.0	5.0	5.25	V	1
Operating ambient temperature	T_{OP}	−40		105	°C	3

[Note 1] Values are specified using VSS (ground) = 0 V as the reference.

[Note 2] Connect VOUT18 pin to PLLVDD pin. (no external 1.8 V power supply required)

[Note 3] The maximum operating ambient temperature of 105 °C is specified for the following conditions:

- 4-layer board with over 300 % copper coverage.

* These conditions also assume this device is the only one mounted on the board.

● Power Consumption

Table 8 Power Consumption

Parameter	Conditions	Symbol	Min.	Typ.	Max.	Unit	Note
Total power consumption	C_L = 20pF V_{IL} = ground $V_{IH} = V_{DD33}$	P_D			TBD	mW	1
Current drawn from each supplies							
- VDD33, VDDIN		I_{VDD}			TBD	mA	1, 2
- VDD5		I_{VDD5}			TBD	mA	1

[Note 1] The total power consumption and drawn current values assume recommended operating conditions.

[Note 2] The current drawn from PLLVDD is included in this value.

● DC Characteristics

Table 9 Input Voltages

Parameter	Symbol	Min.	Typ.	Max.	Unit	Note
Low level input voltage						
XIN pin	V_{IL}	−0.3		$V_{DD33} \times 0.3$	V	1
Input pins and I/O pins (except XIN pin) using 3.3 V rail (VDD33, VDDIN)	V_{IL}	−0.3		0.8	V	1
Input pins and I/O pins using 5 V rail (VDD5) when VDD5 is from 3.0 V to 3.6 V	V_{IL}	−0.3		$V_{DD5} \times 0.2$	V	1
Input pins and I/O pins using 5 V rail (VDD5) when VDD5 is from 3.6 V to 5.25 V	V_{IL}	−0.3		0.8	V	1
High level input voltage						
XIN pin	V_{IH}	$V_{DD33} \times 0.7$		$V_{DD33} + 0.3$	V	1
RESET_N pin	V_{IH}	2.0		5.5	V	1, 2
Input pins and I/O pins (except XIN and RESET_N pins) using 3.3 V rail (VDD33, VDDIN)	V_{IH}	2.0		$V_{DD33} + 0.3$	V	1
Input pins and I/O pins using 5 V rail (VDD5) when VDD5 is from 3.0 V to 3.6 V	V_{IH}	$V_{DD5} \times 0.8$		5.5	V	1
Input pins and I/O pins using 5 V rail (VDD5) when VDD5 is from 3.6 V to 5.25 V	V_{IH}	2.0		5.5	V	1

[Note 1] Values are specified using VSS (ground) = 0 V as the reference.

[Note 2] Up to 5.5 V can be applied to RESET_N pin when V_{DD33} is powered, or up to 4.6 V, when V_{DD33} is unpowered.

Table 10 Output Voltages

Parameter	Conditions	Symbol	Min.	Typ.	Max.	Unit	Note
Low level output voltage							
Output pins and I/O pins (except XOUT pin) using 3.3 V rail (VDD33, VDDIN)	I_{OL} = 100μA	V_{OL}	0		0.2	V	1
	I_{OL} = 2mA	V_{OL}	0		0.4	V	1
Output pins and I/O pins using 5 V rail (VDD5)	I_{OL} = 100μA	V_{OL}	0		0.2	V	1
	I_{OL} = 4mA	V_{OL}	0		0.4	V	1
High level output voltage							
Output pins and I/O pins (except XOUT pin) using 3.3 V rail (VDD33, VDDIN)	I_{OH} = −100μA	V_{OH}	$V_{DD33} - 0.2$		V_{DD33}	V	1
	I_{OL} = −2mA	V_{OH}	2.4		V_{DD33}	V	1
Output pins and I/O pins using 5 V rail (VDD5)	I_{OH} = −100μA	V_{OH}	$V_{DD5} - 0.2$		V_{DD5}	V	1
	I_{OL} = −4mA	V_{OH}	$V_{DD5} \times 0.8$		V_{DD5}	V	1

[Note 1] Values are specified using VSS (ground) = 0 V as the reference.

Table 11 Leakage Current

Parameter	Symbol	Min.	Typ.	Max.	Unit	Note
Input leakage current	I_{LI}	−10		+10	μA	
Output leakage current	I_{LO}	−25		+25	μA	

Table 12 Pin Capacitance

Parameter	Symbol	Min.	Typ.	Max.	Unit	Note
Input pin capacitance	C_I			10	pF	
Output pin capacitance	C_O			10	pF	
Input and Output pin capacitance	C_{IO}			10	pF	

● AC Characteristics

Measurement Conditions:

Input voltage	0 V / V_{DD33} or 0 V / V_{DD5}
Input ramp time	1 ns (The ramp time is defined as the time interval from when the input voltage reaches at V_{DD33} × 0.2 (or V_{DD5} × 0.2) till when it reaches at V_{DD33} × 0.8 (or V_{DD5} × 0.8.))
Timing reference signal levels	Input V_{IL} / V_{IH}
	Output V_{DD33} / 2 V or V_{DD5} / 2 V
Output load capacitance	20 pF

· Clock Input

Table 13 Clock Input

No.	Parameter	Symbol	Min.	Typ.	Max.	Unit	Note
1	XIN: Clock Frequency	f_{XIN}	6		40	MHz	1
	XIN: Clock Cycle Time	t_{XIN}	25		166	ns	1
2	DTCKIN: Clock Frequency	f_{DTCKIN}			40	MHz	
	DTCKIN: Clock Cycle Time	t_{DTCKIN}	25			ns	
3	XIN, DTCKIN: Clock High Level Pulse Width	t_{whCLK}	7.5			ns	
4	XIN, DTCKIN: Clock Low Level Pulse Width	t_{wlCLK}	7.5			ns	
5	SYCLK: Clock Frequency	f_{SYCLK}	50		80	MHz	2
			50		100		2, 3
	SYCLK: Clock Cycle Time	t_{SYCLK}	12.5		20	ns	2
			10		20		2, 3
6	PLL Out: Clock Frequency	f_{PLLO}	200		320	MHz	2
	PLL Out: Clock Cycle Time	t_{PLLO}	3.125		5	ns	2
7	DCLK: Clock Frequency	f_{DCLK}			40	MHz	4
	DCLK: Clock Cycle Time	t_{DCLK}	25			ns	4

[Note 1] A clock frequency ranging from 6 MHz to 40 MHz can be fed to XIN pin. The on-chip oscillator supports from 6 MHz to 20 MHz crystals on XIN and XOUT pins.

[Note 2] SYCLK indicates the internal system clock (PLL Out divided by 4).

[Note 3] Values for system reset in a preset mode (PCLKCTL1-0 = LH, HL, or HH).

[Note 4] DCLK indicates the internal dot clock.

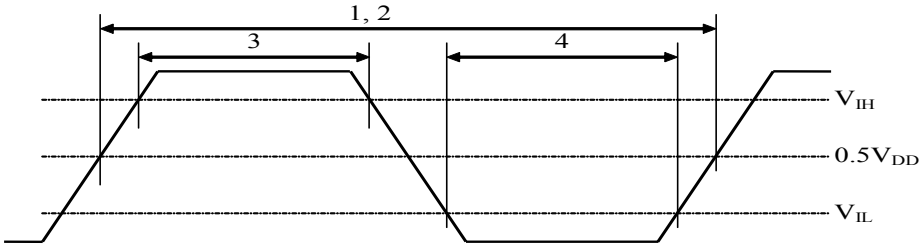


Figure 5 Clock Input.

· Power Supply and Reset Timing Requirements

Table 14 Power Supply and Reset Timing Requirements

No.	Parameter	Symbol	Min.	Typ.	Max.	Unit	Note
1	RESET_N: Assert time	t_{wRES}	10			µs	1
2	RESET_N: Controller Access Hold-Off Time After De-assertion	t_{wAW}	1 to 3.4			ms	
3	RESET_N: Setup Time	t_{sRES}	0			ns	2
4	VDD33, VDDIN: Turn-on Time Difference	t_{vSKWR}			1	s	3
5	VDD33, VDDIN: Turn-off Time Difference	t_{vSKWF}			1	s	4
6	Supply Voltage Ramp Time	t_{vRISE}			200	ms	
7	VDD5: Turn-on Time Difference to VDD33, VDDIN	t_{vSKWR5}	−1			s	5
8	VDD5: Turn-off Time Difference to VDD33, VDDIN	t_{vSKWF5}	−1			s	5
9	VOUT18: Ramp Time	t_{vCORE}			300	µs	6
10	OCPEN: Reset Input Time	t_{wOCPE}	10			µs	
11	OCPEN: Error Input Time	t_{wOCPR}	0.4		10	ms	

[Note 1] RESET_N signal must be asserted for the duration of the time indicated after all the supply voltages exceed 3.0 V, and the VDD18 rise beyond 1.7 V while receiving a stable clock signal on XIN.

[Note 2] RESET_N signal must be asserted the time indicated before first supply voltage reaches its operating level.

[Note 3] It is recommended to turn on both VDD33 and VDDIN at the same time. Uses with one second or more time-difference can affect device reliability.

[Note 4] It is recommended to turn off both VDD33 and VDDIN at the same time. Uses with one second or more time-difference can affect device reliability.

[Note 5] 5 V supply can remain powered when 3 V supplies (VDD33, VDDIN) are turned off.

[Note 6] Four 1 µF capacitors are connected to VOUT18 and VDDCORE pins.

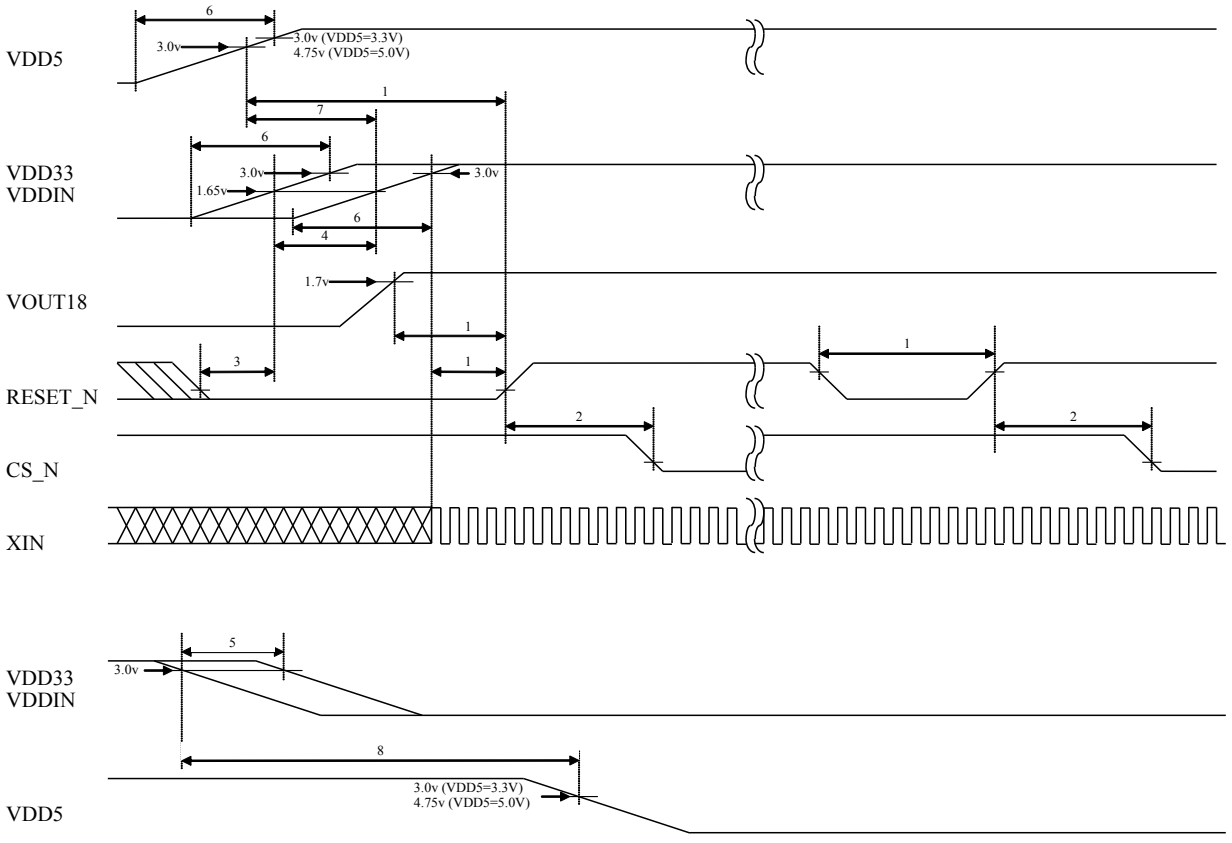


Figure 6 Power Supply and Reset Timing Requirements (1).

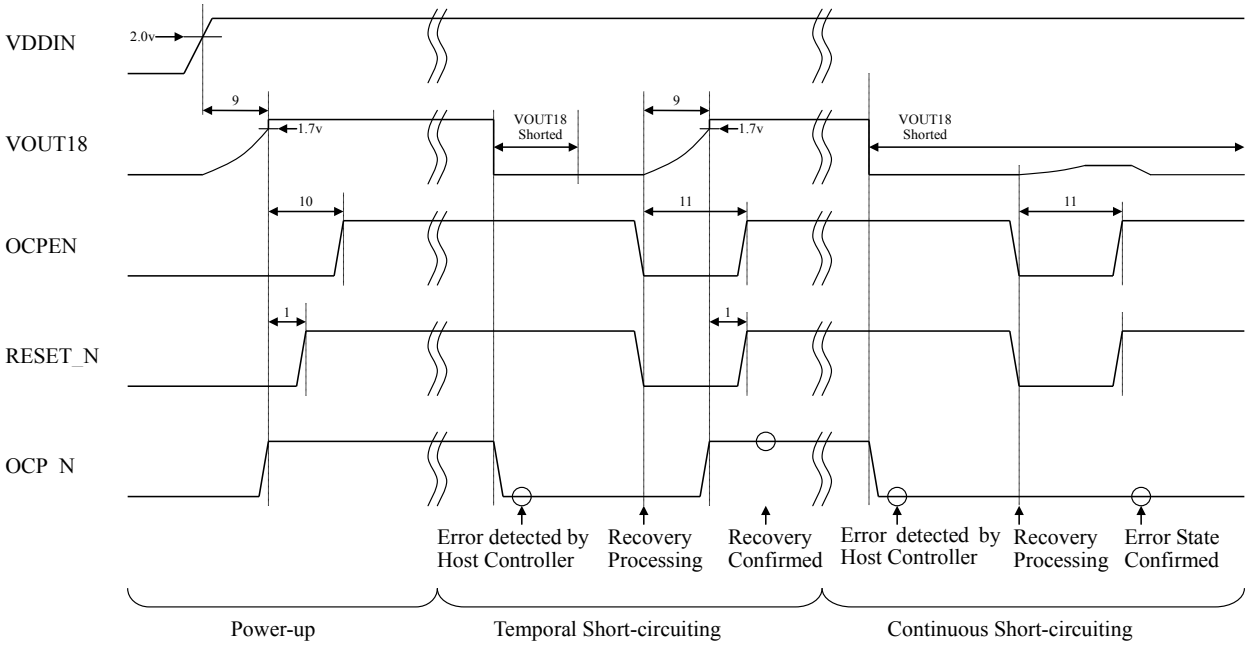


Figure 7 Power Supply and Reset Timing Requirements (2).

· Host Controller Interface

i) Parallel Interface

Table 15 Host Controller Interface (Parallel)

No.	Parameter	Symbol	Min.	Typ.	Max.	Unit	Note
1	PS2-0: Input Data Setup Time	t_{sA}	4			ns	1
2	PS2-0: Input Data Hold Time	t_{hA}	0			ns	1
3	CS_N: Input Data Setup Time	t_{sCS}	0			ns	2
4	CS_N: Input Data Hold Time	t_{hCS}	0			ns	2
5	D7-0: Output Data Turn On Time	t_{onD}	0			ns	
6	D7-0: Output Data Turn Off Time	t_{offD}			30	ns	
7	D7-0: Output Data Valid Delay Time	t_{odD}			0	ns	
8	D7-0: Output Data Hold Time	t_{ohD}	0			ns	
9	WAIT_N, READY_N: Output Data Turn On Time	t_{onWAIT}	0			ns	
10	WAIT_N, READY_N: Output Data Valid Delay Time	t_{dWAIT}			25	ns	
11	WAIT_N, READY_N: Output Data Turn Off Time	$t_{offWAIT}$			30	ns	
12	D7-0: Input Data Setup Time	t_{sD}	t_{SYCLK} + 15			ns	
13	D7-0: Input Data Hold Time	t_{hD}	2			ns	
14	WR_N: Hold Time	t_{hWR}	0			ns	
15	READY_N: Output Data Hold Time	t_{hREADY}	0		30	ns	
16	Command Pulse Active Time	t_{aCMD}	2 × t_{SYCLK}			ns	3
17	Command Pulse Inhibit Time	t_{iCMD}	4 × t_{SYCLK}			ns	3
18	Command Cycle Time	t_{cCMD}	6 × t_{SYCLK}			ns	3

[Note 1] These values assume that WR_N or RD_N is the access strobe signal. Substitute CS_N for WR_N or RD_N in the diagrams and interpret these values accordingly if CS_N is the access strobe signal.

[Note 2] Satisfying these conditions establishes that WR_N or RD_N is the access strobe signal. Otherwise CS_N is the access strobe signal.

[Note 3] Command Pulse is a low-active pulse, which is the result of a logical OR operation between WR_N and CS_N signals or RD_N and CS_N signals.

➢ Host Controller Read Cycle

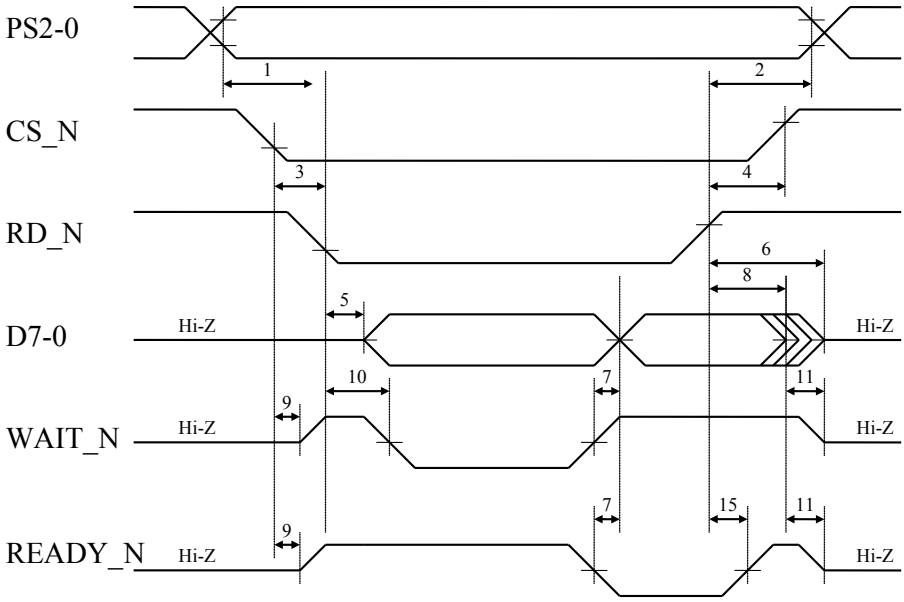


Figure 8 Host Controller Access Timing (Parallel Interface / Read Cycle).

➢ Host Controller Write Cycle

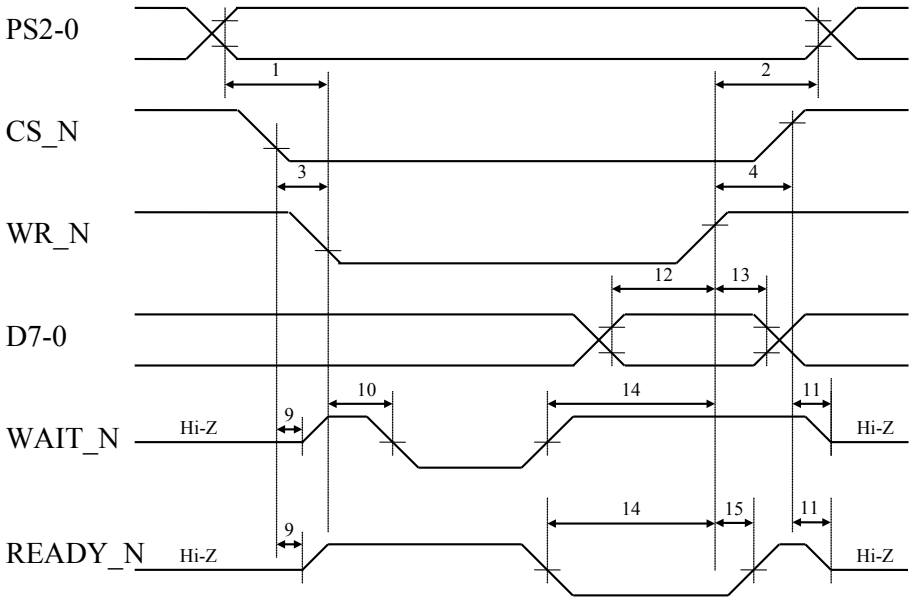


Figure 9 Host Controller Access Timing (Parallel Interface / Write Cycle).

➢ Access Cycle

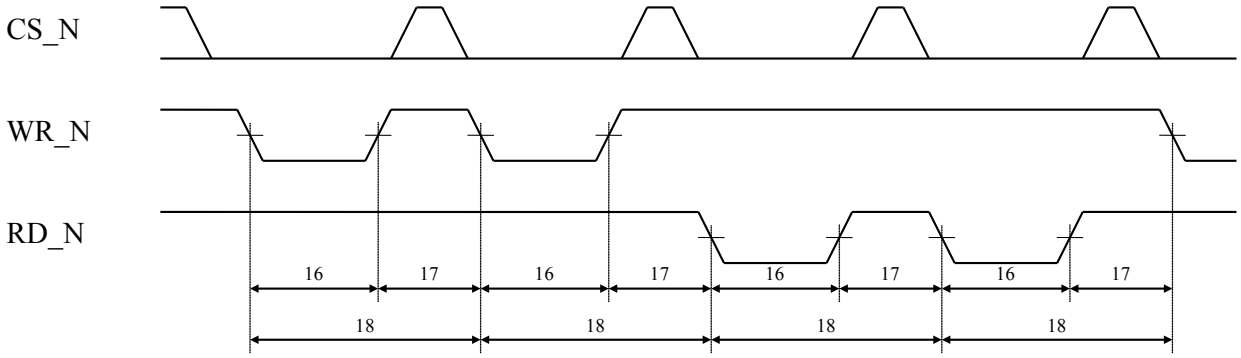


Figure 10 Host Controller Access Timing (Parallel Interface / Access Cycle).

ii) Serial Interface

Table 16 Host Controller Interface (Serial)

No.	Parameter	Symbol	Min.	Typ.	Max.	Unit	Note
1	SCLK: Clock Cycle Time	t_{wSCLK}	125			ns	
			$4 \times t_{XIN}$				1
2	SCLK: Clock High Level Pulse Width	t_{whSCLK}	62.5			ns	
			$2 \times t_{XIN}$				1
3	SCLK: Clock Low Level Pulse Width	t_{wlSCLK}	62.5			ns	
			$2 \times t_{XIN}$				1
4	SCS_N: Input Data Setup Time	t_{sSCS}	25			ns	
			$1.5 \times t_{XIN}$				1
5	SCS_N: Input Data Hold Time	t_{hSCS}	25			ns	
			$1.5 \times t_{XIN}$				1
6	SDIN: Input Data Setup Time	t_{sSDI}	25			ns	
			$1.5 \times t_{XIN}$				1
7	SDIN: Input Data Hold Time	t_{hSDI}	25			ns	
			$1.5 \times t_{XIN}$				1
8	SDOUT: Output Data Delay Time	t_{dSDO}			30	ns	
9	SDOUT: Output Data Turn Off Time	t_{offSDO}			20	ns	
10	SCS_N: Pulse Inhibit Time	t_{iSCS}	400			ns	
			$4 \times t_{XIN}$				1

[Note 1] The alternative value must be used for consideration during the initialization period of YGV642. The clock signal to XIN pin is used as a system clock for during the initialization.

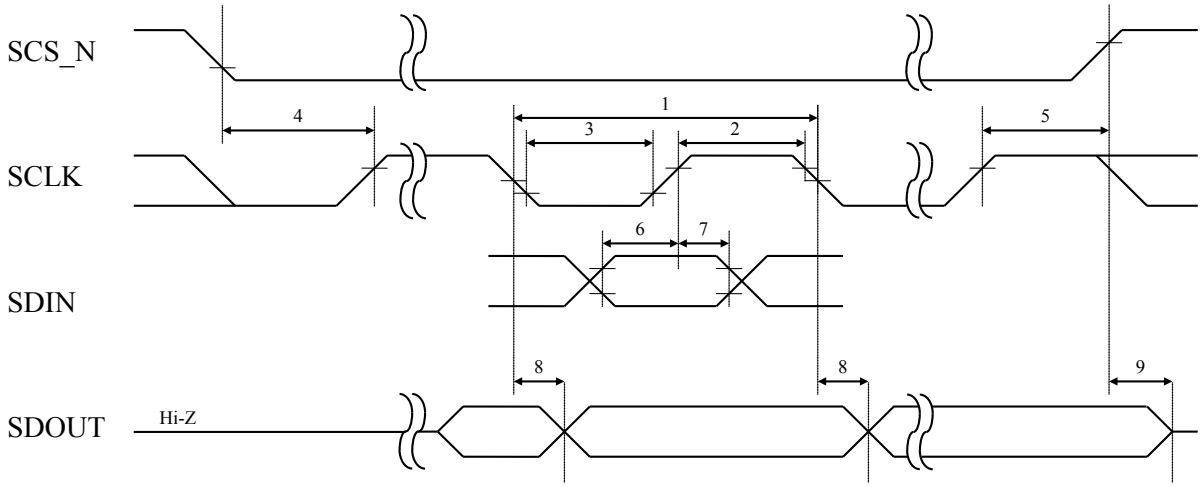


Figure 11 Host Controller Access Timing (Serial Interface) (1).

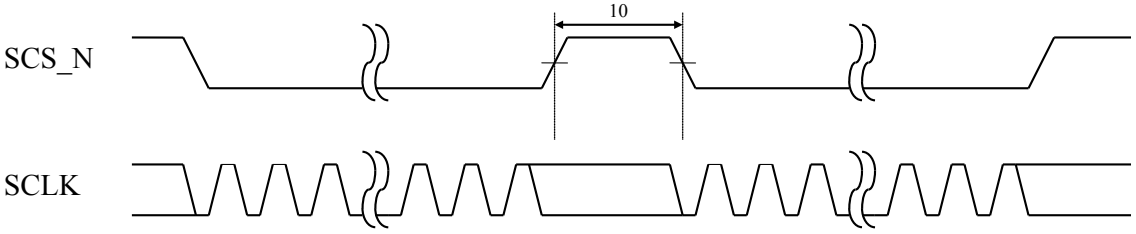


Figure 12 Host Controller Access Timing (Serial Interface) (2).

iii) Pattern Memory Programming

Table 17 Pattern Memory Programming

No.	Parameter	Symbol	Min.	Typ.	Max.	Unit	Note
1	WP_SCLK: Clock Period	$t_{wWPSCLK}$	125			ns	
			$4 \times t_{XIN}$				1
2	WP_SCLK: Clock High Duration	$t_{whWPSCLK}$	62.5			ns	
			$2 \times t_{XIN}$				1
3	WP_SCLK: Clock Low Duration	$t_{wlWPSCLK}$	62.5			ns	
			$2 \times t_{XIN}$				1
4	WP_SCS_N: Input Data Setup Time	t_{sWPSCS}	25			ns	
			$1.5 \times t_{XIN}$				1
5	WP_SCS_N: Input Data Hold Time	t_{hWPSCS}	25			ns	
			$1.5 \times t_{XIN}$				1
6	WP_SDIN: Input Data Setup Time	t_{sWPSDI}	25			ns	
			$1.5 \times t_{XIN}$				1
7	WP_SDIN: Input Data Hold Time	t_{hWPSDI}	25			ns	
			$1.5 \times t_{XIN}$				1
8	WP_SDOUT: Output Data Delay Time	t_{dWPSDO}			30	ns	
9	WP_SDOUT: Output Data Turn Off Time	$t_{offWPSDO}$			20	ns	
10	WP_SCS_N: Pulse Inhibit Time	t_{iWPSCS}	400			ns	
			$4 \times t_{XIN}$				1

[Note 1] The alternative value must be used for consideration during the initialization period of YGV642. The clock signal to XIN pin is used as a system clock for during the initialization.

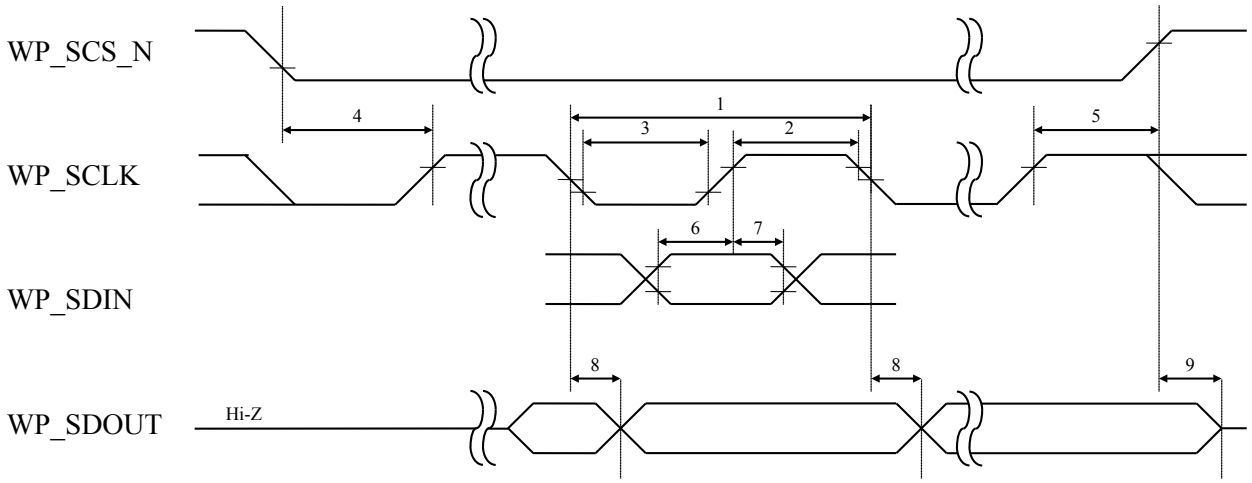


Figure 13 Pattern Memory Programming (1).

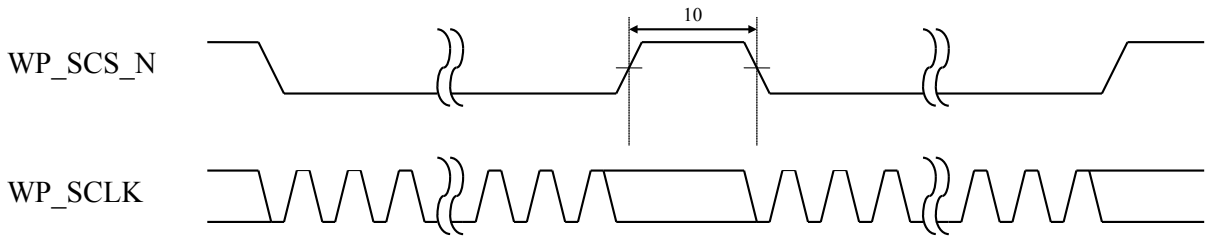


Figure 14 Pattern Memory Programming (2).

· Pattern Memory Interface

Table 18 Pattern Memory Interface

No.	Parameter	Symbol	Min.	Typ.	Max.	Unit	Note
1	MSCLKO: Clock Frequency	f_{MSCLK}	50		80	MHz	
	MSCLKO: Clock Cycle Time	t_{MSCLK}	12.5		20	ns	
2	MSCLKO: Clock High Level Pulse Width	$t_{whMSCLK}$	$t_{MSCLK} \times 0.4$			ns	
3	MSCLKO: Clock Low Level Pulse Width	$t_{wlMSCLK}$	$t_{MSCLK} \times 0.4$			ns	
4	MSIO3-0: Input Data Setup Time	t_{sMSI}	2			ns	
5	MSIO3-0: Input Data Hold Time	t_{hMSI}	0			ns	
6	MSCS1-0_N, MSIO3-0: Output Data Hold Time	t_{hMSO}	−0.5			ns	
7	MSCS1-0_N, MSIO3-0: Output Data Delay Time	t_{odMSO}			2	ns	
8	MSIO3-0: Output Turn on Time	t_{onMSO}	0			ns	
9	MSIO3-0: Output Turn off Time	t_{offMSO}			10	ns	
10	MSCLKI: Input Delay Time	$t_{idMSCLKI}$	0		4	ns	1

[Note 1] For MSCLKO and MSCLKI connections, see notes 8 and 9 in section ■ *Pin Descriptions*.

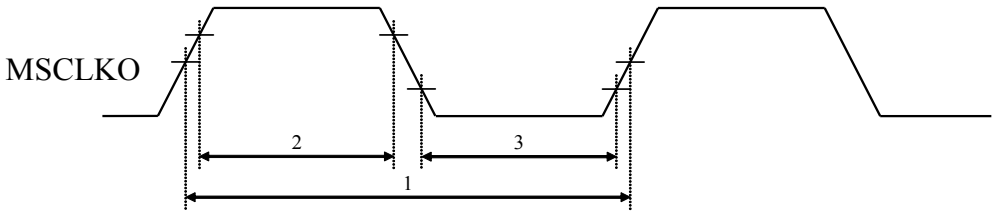


Figure 15 Pattern Memory Access Timing (1).

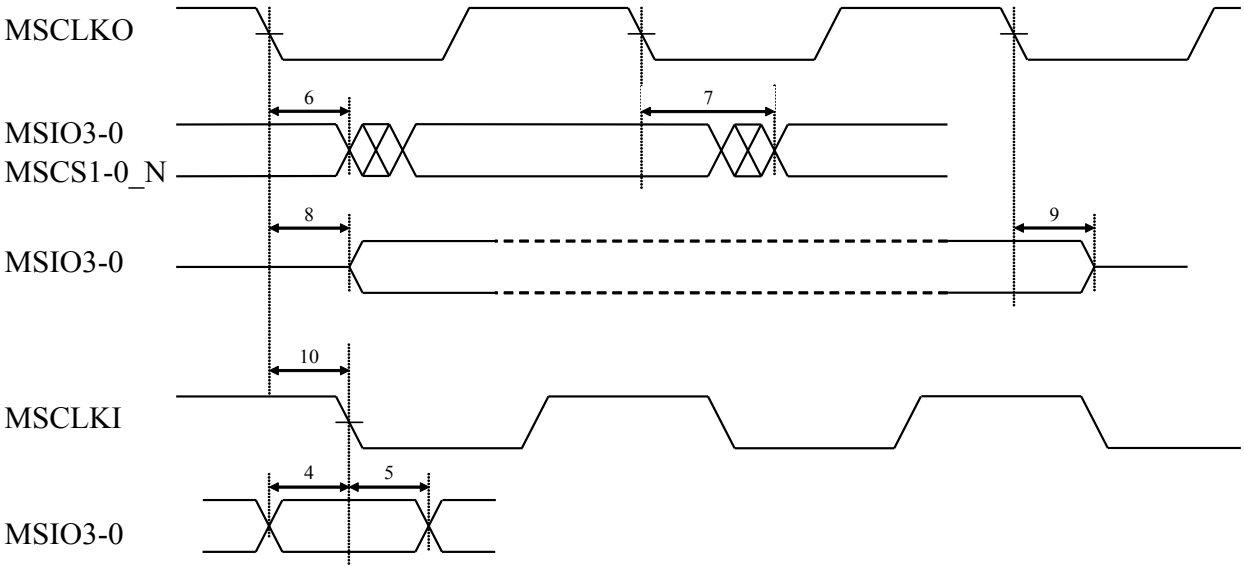
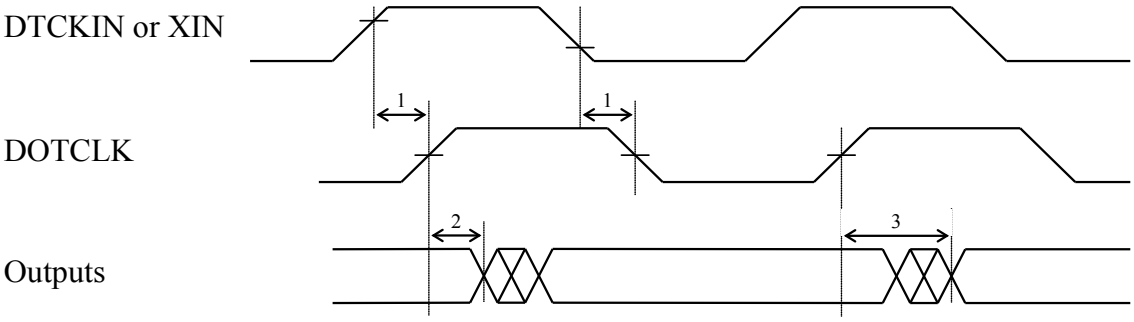


Figure 16 Pattern Memory Access Timing (2).

· Display Timing Signals

Table 19 Display Timing Signals

No.	Parameter	Symbol	Min.	Typ.	Max.	Unit	Note
1	DOTCLK: Delay Time	t_{dDOTC}			26	ns	
2	VSYNC_N, HCSYNC_N, BLANK_N, DR7-0, DG7-0, DB7-0, CLKV, STARTH, STARTV, LOADH, POL, OUTENV: Output Hold Time	t_{hDISP}	0			MHz	
3	VSYNC_N, HCSYNC_N, BLANK_N, DR7-0, DG7-0, DB7-0, CLKV, STARTH, STARTV, LOADH, POL, OUTENV: Output Delay Time	t_{dDISP}			8	ns	



* DOTCLK output not inverted

Figure 17 Display Timing Signals.

■ Package Information

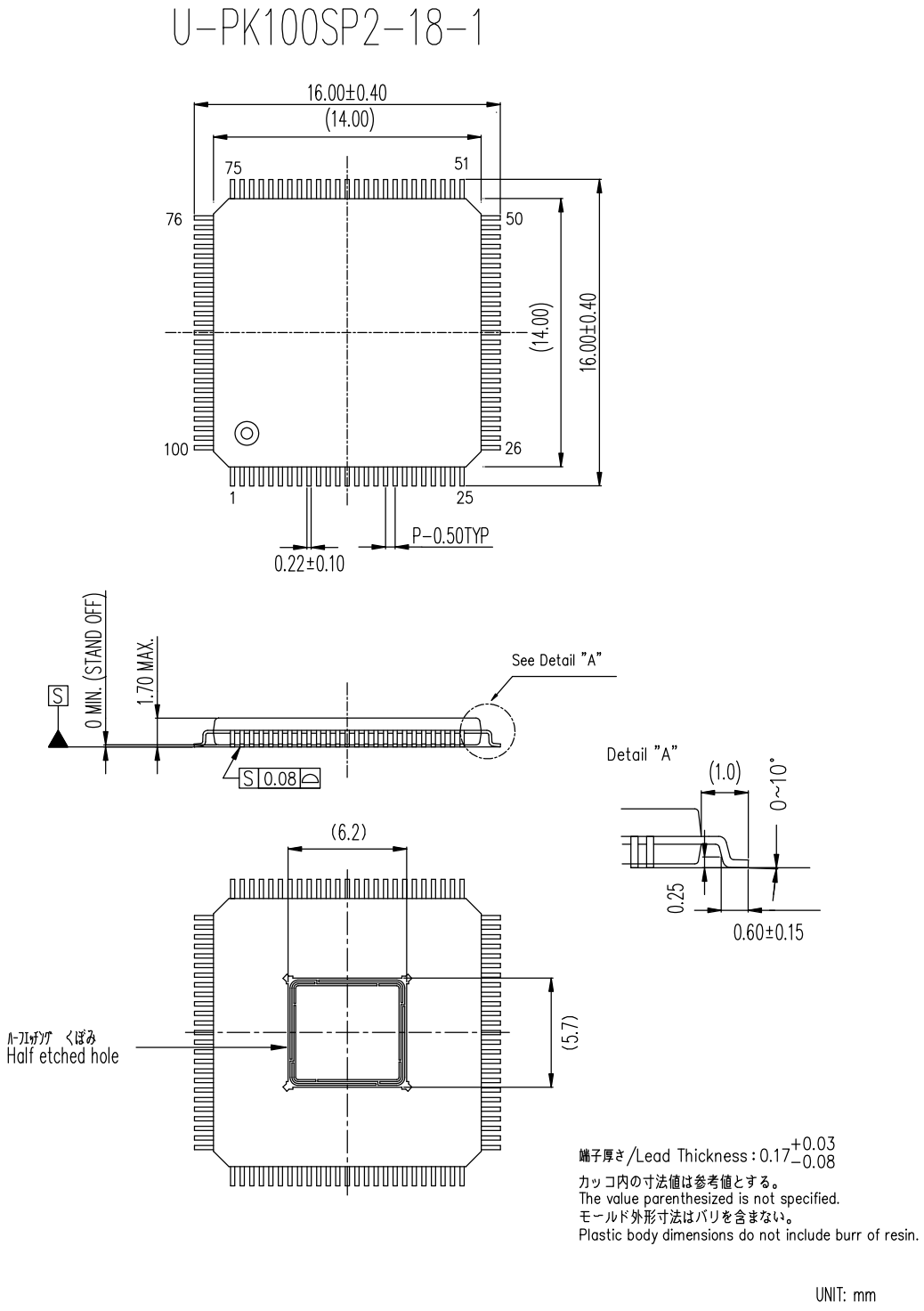


Figure 18 Package Information.

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Instructions	Products should be designed with fail safe in mind in case of malfunction of the built-in protection circuits. Note that the built-in protection circuits such as overcurrent protection circuit and high-temperature protection circuit do not always protect the internal circuits. In some cases, depending on usage or situations, such protection circuit may not work properly or the device itself may break down before the protection circuit kicks in.
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v02

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