

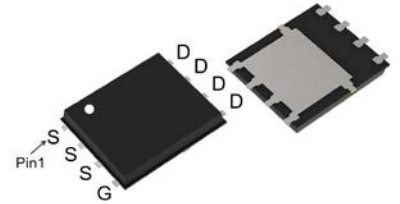


Features

- Enhancement mode
- VitoMOS[®] II Technology
- 100% Avalanche tested, 100% Rg tested
- Optimized Qg, Qgd, and Qgd/Qgs ratio to minimize switching losses

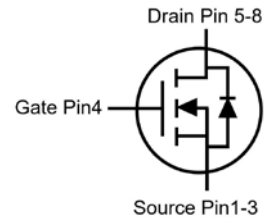
V _{DS}	100	V
R _{DS(on),TYP} @ V _{GS} =10 V	8.5	mΩ
R _{DS(on),TYP} @ V _{GS} =4.5 V	11	mΩ
I _D (Silicon limited)	69	A

PDFN5x6



Halogen-Free

Part ID	Package Type	Marking	Packing
VM9003	PDFN5x6	VM9003	3000pcs/Reel



Maximum ratings, at T_A=25°C, unless otherwise specified

Symbol	Parameter	Rating	Unit	
V(BR)DSS	Drain-source breakdown voltage	100	V	
VGS	Gate-source voltage	±20	V	
IS	Diode continuous forward current (Silicon limited)	T _C = 25°C	69	A
ID	Continuous drain current @VGS=10V (Silicon limited)	T _C = 25°C	69	A
ID	Continuous drain current @VGS=10V (Silicon limited)	T _C = 100°C	44	A
IDM	Pulse drain current tested ^①	T _C = 25°C	215	A
IDSM	Continuous drain current @VGS=10V	T _A = 25°C	11	A
		T _A = 70°C	9	A
EAS	Avalanche energy, single pulsed ^②	81	mJ	
PD	Maximum power dissipation ^③	T _C = 25°C	104	W
		T _C = 100°C	42	W
PDSM	Maximum power dissipation ^④	T _A = 25°C	2.6	W
		T _A = 70°C	1.7	W
TJ,TSTG	Operating junction and storage temperature range	-55 to 150	°C	

Thermal Characteristics

Symbol	Parameter	Typical	Max	Unit
RθJC	Thermal resistance, junction-to-case ^⑤	1	1.2	°C/W
RθJA	Thermal resistance, junction-to-ambient ^⑥	40	48	°C/W



Electrical Characteristics

Symbol	Parameter	Condition	Min.	Typ.	Max.	Unit
Static Electrical Characteristics @ T_j=25°C (unless otherwise stated)						
V(BR)DSS	Drain-source breakdown voltage	V _{GS} =0V, I _D =250μA	100	--	--	V
IDSS	Zero gate voltage drain current(T _j =25°C)	V _{DS} =100V, V _{GS} =0V	--	--	1	μA
	Zero gate voltage drain current(T _j =125°C) ^⑦	V _{DS} =100V, V _{GS} =0V	--	--	100	μA
IGSS	Gate-body leakage current	V _{GS} =±20V, V _{DS} =0V	--	--	±100	nA
V _{GS(th)}	Gate threshold voltage	V _{DS} =V _{GS} , I _D =250μA	1.3	1.8	2.4	V
R _{DS(on)}	Drain-source on-state resistance ^⑧	V _{GS} =10V, I _D =40A	--	8.5	12	mΩ
		(T _j =100°C) ^⑦	--	13	--	mΩ
R _{DS(on)}	Drain-source on-state resistance ^⑧	V _{GS} =4.5V, I _D =30A	--	11	16	mΩ
G _{FS}	Forward transconductance	V _{DS} =5V, I _D =40A	--	66	--	S
Dynamic Electrical Characteristics @ T_j = 25°C (unless otherwise stated)						
C _{iss}	Input capacitance ^⑦	V _{DS} =50V, V _{GS} =0V, f=100kHz	--	1540	--	pF
C _{oss}	Output capacitance ^⑦		--	470	--	pF
C _{rss}	Reverse transfer capacitance ^⑦		--	15	--	pF
R _g	Gate resistance	f=1MHz	--	1.5	--	Ω
Q _{g(10V)}	Total gate charge ^⑦	V _{DS} =50V, I _D =40A, V _{GS} =10V	--	24	--	nC
Q _{g(4.5V)}	Total gate charge ^⑦		--	12	--	nC
Q _{gs}	Gate-source charge ^⑦		--	5.3	--	nC
Q _{gd}	Gate-drain charge ^⑦		--	4.4	--	nC
Switching Characteristics^⑦						
T _{d(on)}	Turn-on delay time	V _{DD} =50V, I _D =40A, R _G =3Ω, V _{GS} =10V	--	7.7	--	ns
T _r	Turn-on rise time		--	35	--	ns
T _{d(off)}	Turn-off delay time		--	21	--	ns
T _f	Turn-off fall time		--	27	--	ns
Source- Drain Diode Characteristics @ T_j = 25°C (unless otherwise stated)						
V _{SD}	Forward on voltage	I _{SD} =40A, V _{GS} =0V	--	0.89	1	V
T _{rr}	Reverse recovery time ^⑦	V _{DD} =50V, I _{sd} =40A, V _{GS} =0V	--	28	--	ns
Q _{rr}	Reverse recovery charge ^⑦	di/dt=100A/μs	--	17	--	nC

NOTE:

- ① Single pulse; pulse width ≤ 100μs.
- ② This value is based on starting T_j = 25°C, L = 0.5mH, R_G = 25Ω, I_{AS} = 18A, V_{GS}=10V; 100% FT tested at L = 0.5mH, I_{AS} = 14A.
- ③ The power dissipation P_d is based on T_{j(max)}, using junction-to-case thermal resistance R_{θJC}.
- ④ The power dissipation P_{dsm} is based on T_{j(max)}, using junction-to-ambient thermal resistance R_{θJA}.
- ⑤ Thermal resistance from junction to soldering point (on the exposed drain pad). These tests are performed on a cold plate.
- ⑥ These tests are performed with the device mounted on 1 in2 FR-4 board with 2oz. Copper, in a still air environment with TA=25°C.
- ⑦ Guaranteed by design, not subject to production testing.
- ⑧ Pulse width ≤ 380μs; duty cycle ≤ 2%.



Typical Characteristics

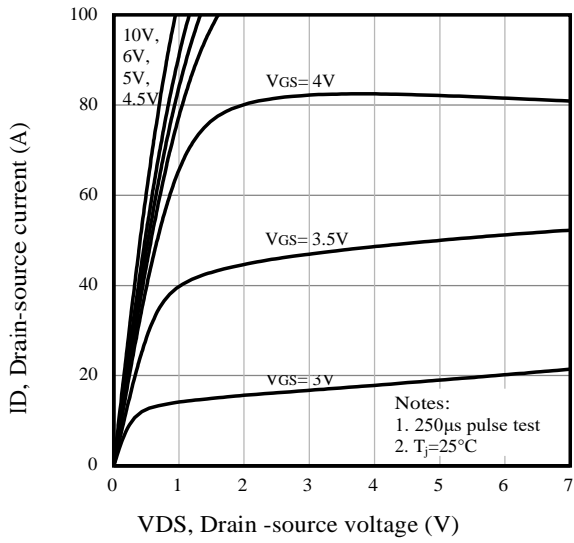


Fig1. Typical output characteristics

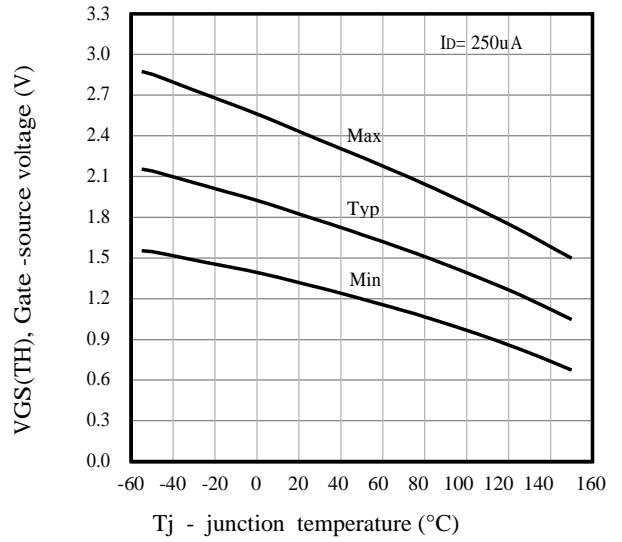


Fig2. Typical $V_{GS(TH)}$ gate-source voltage Vs. T_j

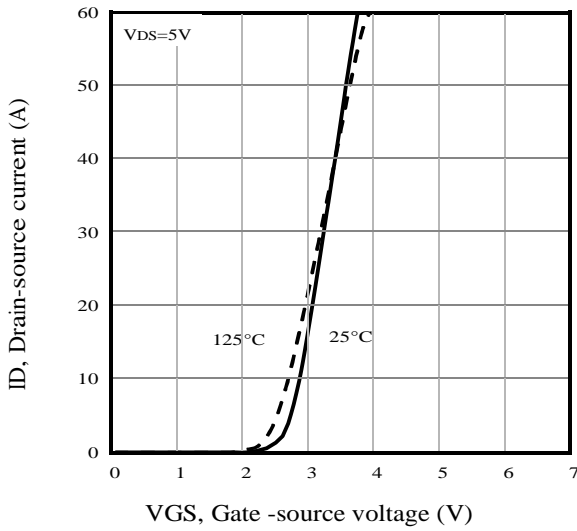


Fig3. Typical transfer characteristics

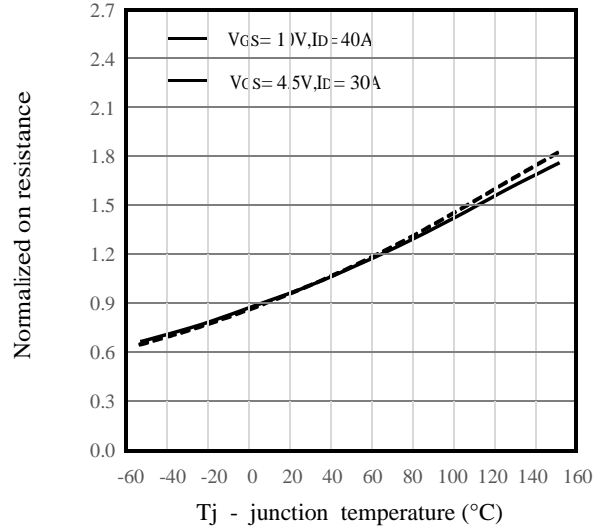


Fig4. Typical normalized on-resistance Vs. T_j

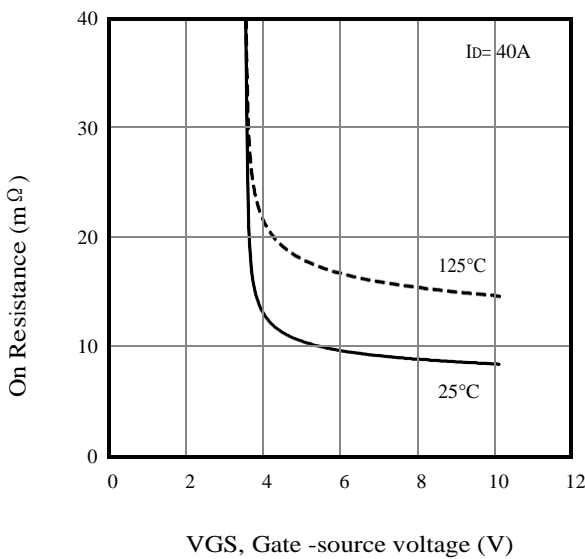


Fig5. Typical on resistance Vs gate-source voltage

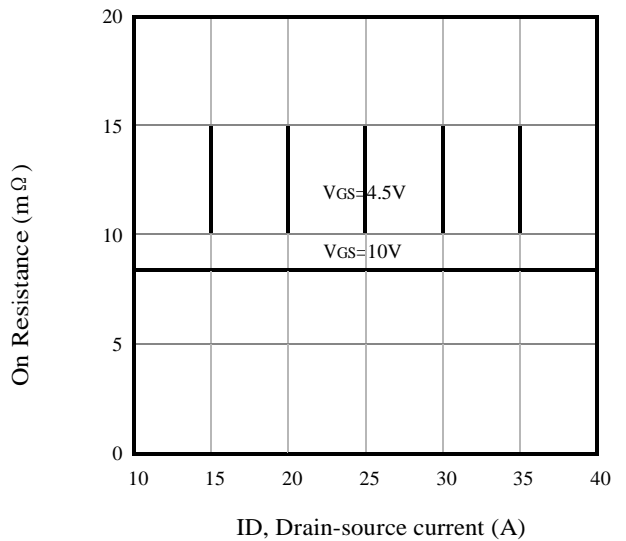


Fig6. Typical on resistance Vs drain current



Typical Characteristics

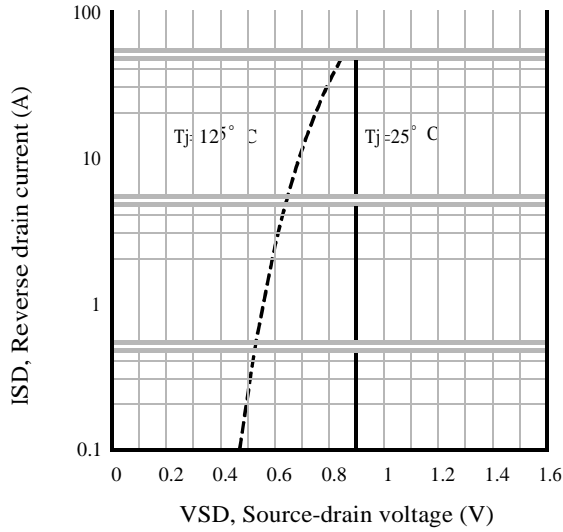


Fig7. Typical source-drain diode forward voltage

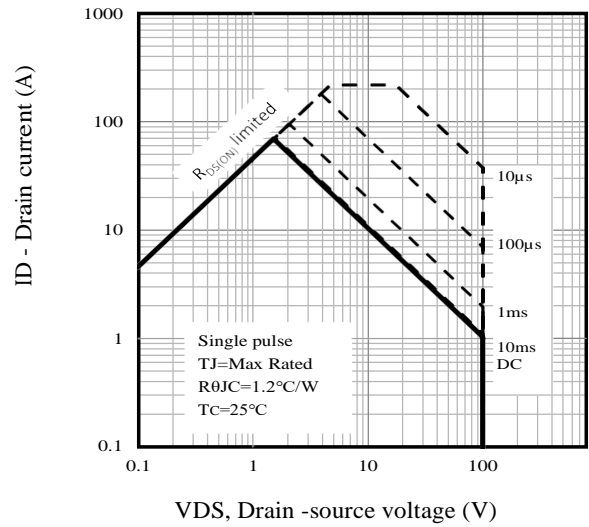


Fig8. Maximum safe operating area

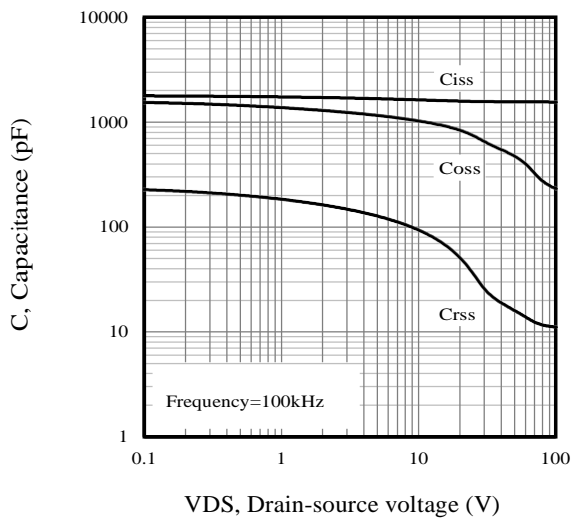


Fig9. Typical capacitance Vs. drain-source voltage

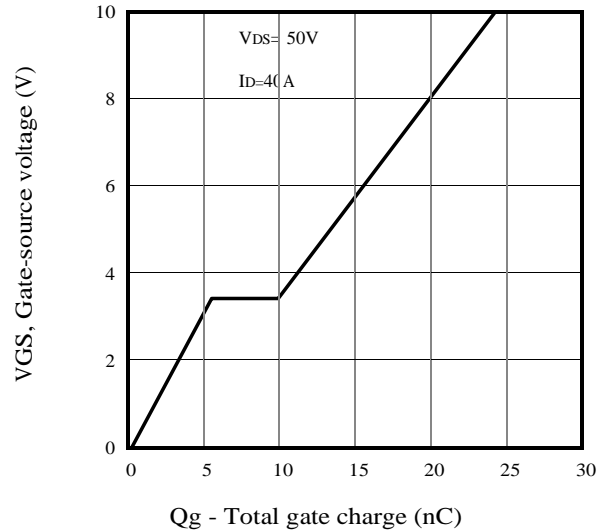


Fig10. Typical gate charge Vs. gate-source voltage

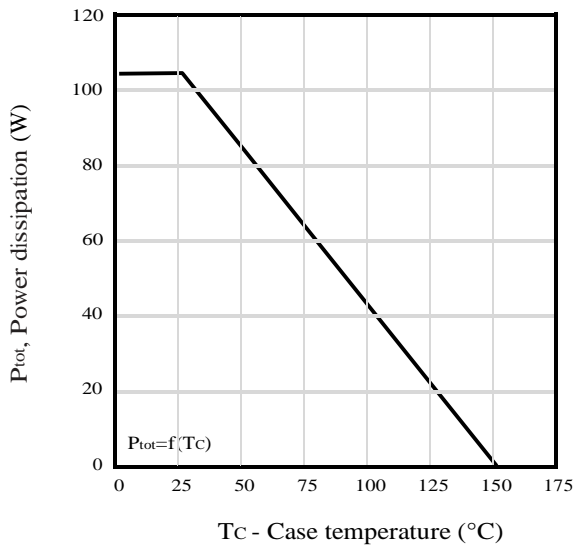


Fig11. Power dissipation Vs. case temperature

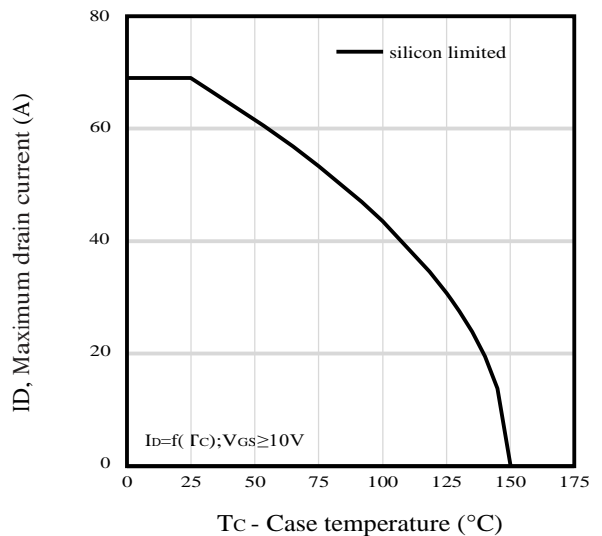
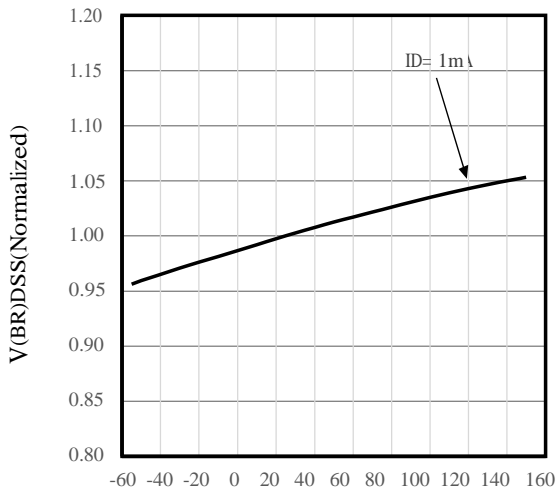


Fig12. Maximum drain current Vs. case temperature

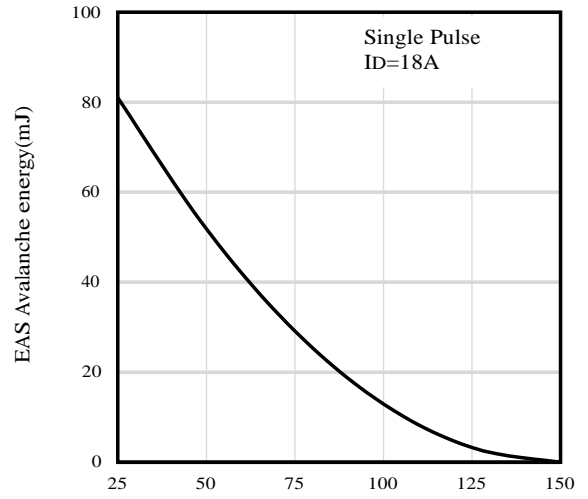


Typical Characteristics



Tj - Junction temperature (°C)

Fig13. Typical V(BR)DSS Vs Tj



Starting Tj junction temperature (°C)

Fig14. Maximum avalanche energy vs temperature (°C)

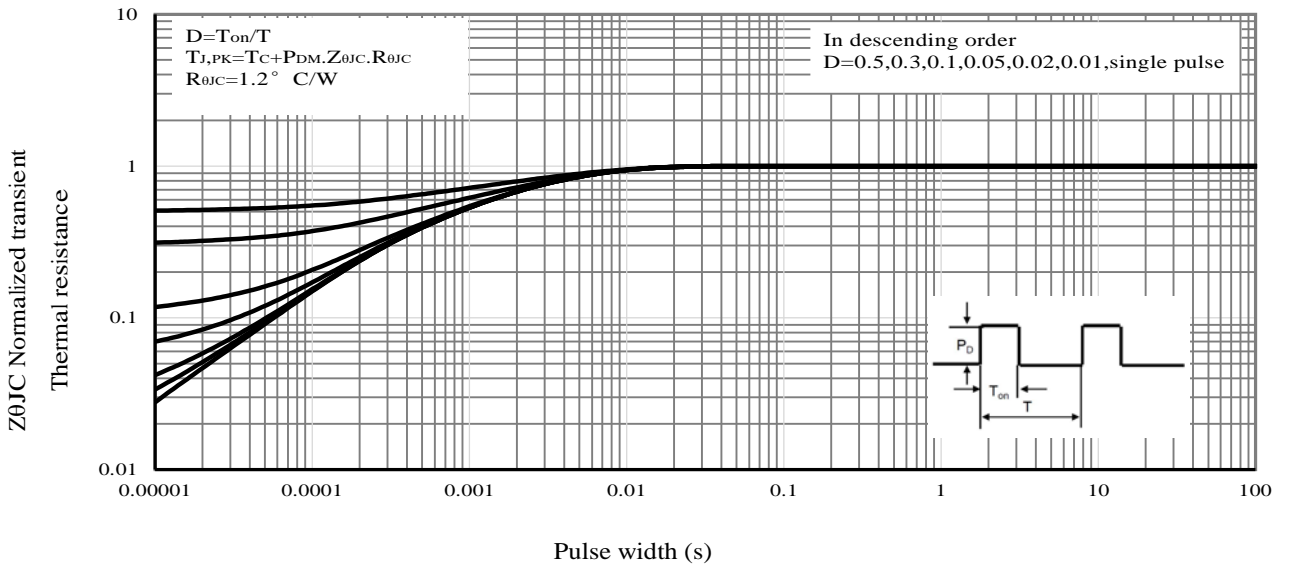


Fig15 . Normalized maximum transient thermal impedance

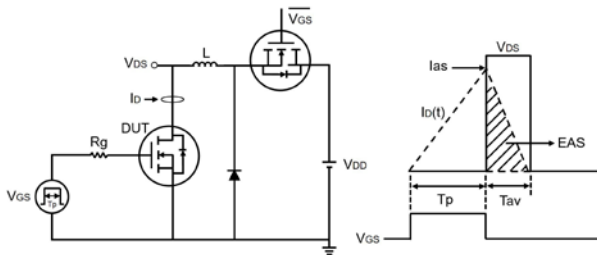


Fig16. Unclamped inductive test circuit and waveforms

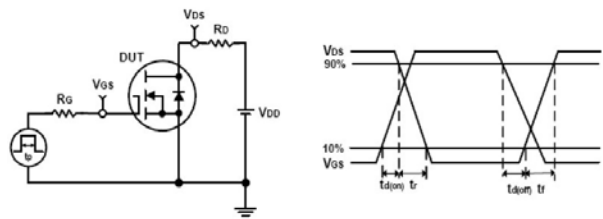
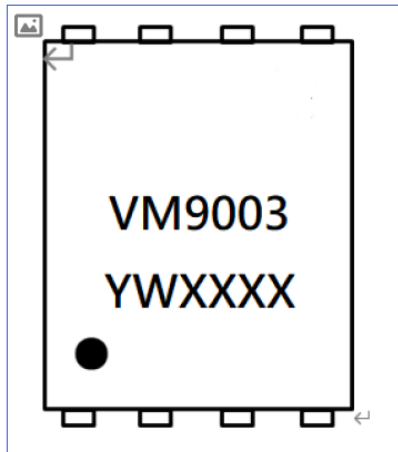


Fig17. Switching time test circuit and waveforms



Marking Information

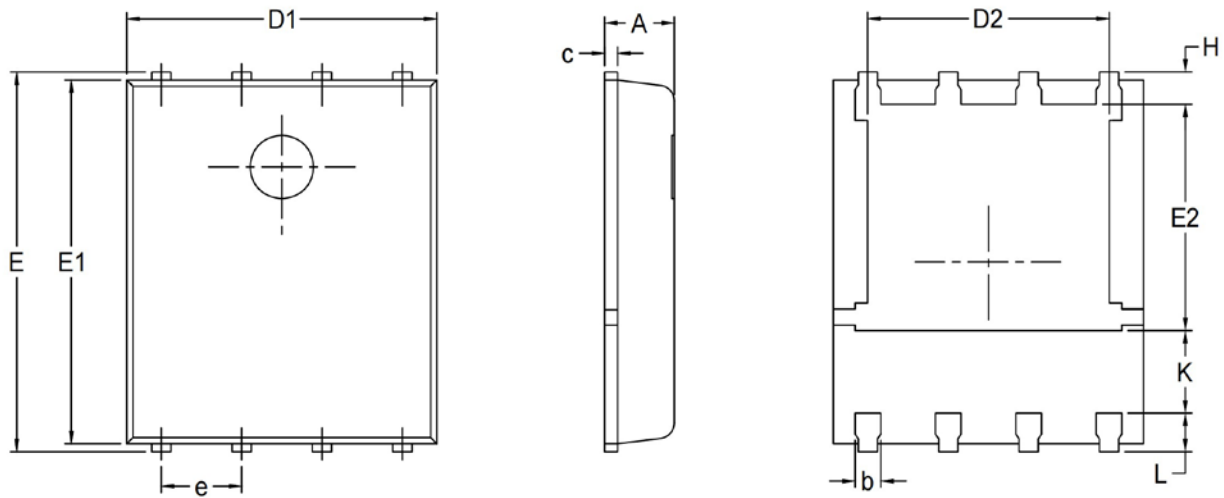


1st line: Part Number (VM9003)

2nd line: Date code (YWXXXX)



PDFN5x6 Package Outline Data



Symbol	DIMENSIONS (unit : mm)		
	Min	Typ	Max
A	0.90	1.00	1.10
b	0.33	0.41	0.51
c	0.20	0.25	0.30
D1	4.80	4.90	5.00
D2	3.61	3.81	3.96
E	5.90	6.00	6.10
E1	5.70	5.75	5.80
E2	3.38	3.58	3.78
e	1.27 BSC		
H	0.41	0.51	0.61
K	1.10	--	--
L	0.51	0.61	0.71

Notes:

- 1.Refer to JEDEC MO-240 variation AA.
- 2.Dimensions "D1" and "E1" do NOT include mold flash protrusions or gate burrs.
- 3.Dimensions "D1" and "E1" include interterminal flash or protrusion. Interterminal flash or protrusion shall not exceed 0.25mm per side.



Contact Information

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