A Product Line of Diodes Incorporated

PI3USB9201

Dual-Role USB Charging-Type Detector

Description

The PI3USB9201 is a dual-role BC1.2-compliance charging-type detector. It can be programmed to operate in host mode or client mode through I^2C.

Particularly for USB-C application with bottom and top D+/- pins common at USB-C connector, when device attachment is detected by USB-C detector, which can program PI3USB9201 to perform BC1.2-compliance charging-type detections on D+/- connection.

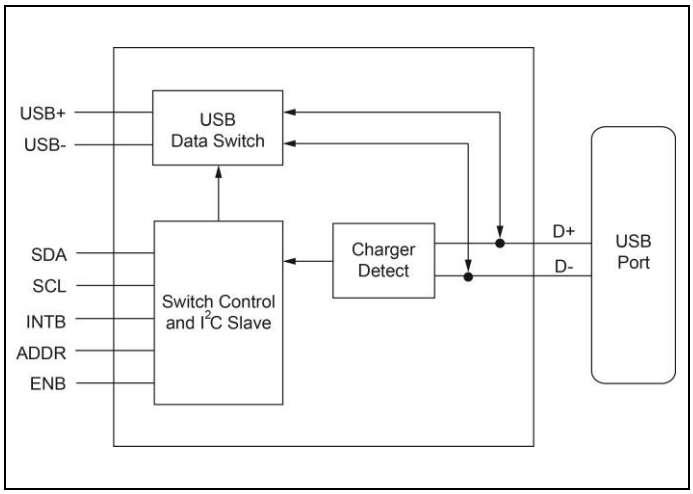
When operating as a host, PI3USB9201 enables BC1.2 SDP/CDP/DCP advertisement to the attached USB devices. When operating as a client, PI3USB9201 starts BC1.2 detection to detect the attached host type. In both host mode and client mode, the detection results are reported through I^2C to the controller.

The PI3USB9201 can operate over a temperature range of -40 to +85° in a tiny 12- contact QFN 2mm x2mm package.

Application(s)

- Mobile Devices

Block Diagram



Features

- Host Mode – SDP/CDP/DCP
  - USB Device Plug-in and Unplug Detection in SDP/CDP modes
  - Support USB Switch Pass-through for Mouse/Keyboard Wake up
- Client Mode USB Charging-type detection
  - Battery Charging 1.2 SDP/CDP/DCP
  - Proprietary 1A/2A/2.4A Modes
- Differential Bi-Directional USB Switches
- Wide Bandwidth: 2GHz
- 1MHz I^2C Interface for Control and Communication with Pin Selection of up to Four Slave Addresses
- Shutdown Mode of <1µA Current Consumption
- Wide Power Supply Range : 2.7V – 5.5V
- Packaging (Pb-free & Green):
  - 12- contact, UQFN 2mm x2mm
- Totally Lead-Free & Fully RoHS Compliant (Notes 1 & 2)
- Halogen and Antimony Free. "Green" Device (Note 3)
- For automotive applications requiring specific change control (i.e. parts qualified to AEC-Q100/101/104/200, PPAP capable, and manufactured in IATF 16949 certified facilities), please contact us or your local Diodes representative.
  https://www.diodes.com/quality/product-definitions/

Notes:
1. No purposely added lead. Fully EU Directive 2002/95/EC (RoHS), 2011/65/EU (RoHS 2) & 2015/863/EU (RoHS 3) compliant.
2. See https://www.diodes.com/quality/lead-free/ for more information about Diodes Incorporated's definitions of Halogen- and Antimony-free, "Green" and Lead-free.
3. Halogen- and Antimony-free "Green" products are defined as those which contain <900ppm bromine, <900ppm chlorine (<1500ppm total Br + Cl) and <1000ppm antimony compounds.

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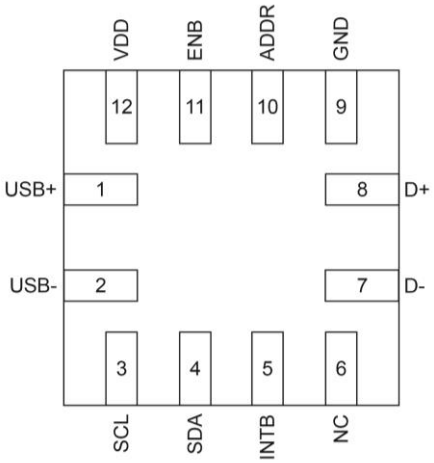
Pin Configuration (Top View)



Pin Descriptions

Pin Number	Name	Type	Default State	Description
USB Interface				
1	USB+	I/O	Open	D+ signal switch path, dedicated USB port to be connected to the resident USB transceiver on the device.
2	USB-	I/O	Open	D- signal switch path, dedicated USB port to be connected to the resident USB transceiver on the device.
Connector Interface				
8	D+	I/O	Open	USB-C connector D+ pin.
7	D-	I/O	Open	USB-C connector D- pin.
Power Interface				
12	V_{DD}	Power	NA	Input voltage supply pin to be connected to the device battery output or to an internal regulator.
9	GND	Power	NA	Ground pin.
6	NC	Open	NA	No Connection
I^2C Interface				
3	SCL	Input	Hi-Z	I^2C serial clock signal to be connected to the phone-based I^2C master.
4	SDA	I/O	Hi-Z	I^2C serial data signal to be connected to the phone-based I^2C master. It is an open-drain output requiring an external pull-up resistor for normal operation.
5	INTB	Output	Hi-Z	Interrupt active-low open-drain output used to prompt the phone baseband processor to read the I^2C register bits, indicates a change in client/host status registers.
Logic Interface				
10	ADDR	Input	Hi-Z	Selecting up to four different I^2C slave addresses (Table 1).
11	ENB	Input	Hi-Z	System enable for the circuit (active low).

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Details Description

Host Mode

The PI3USB9201 supports SDP/CDP/DCP host mode operation, according to REG00h<3:1> setting in Table 3. Since SDP/CDP support data communication, USB channel (D+/- to USB+/-) is ON if host mode SDP and CDP are selected. A DCP only provides power but does not support data connection, so USB channel is OFF if DCP is selected. In Host mode DCP, D+ and D- data lines will be shorted together with a maximum series impedance of 200 Ω.

During Host mode operation, SDP/CDP, if device plugin perform BC1.2 operation, the status is reported in REG03h<0>.

Device plug-in and unplug detection is reported in Host mode SDP/CDP according to USB2.0 specification. The detection status is reported in REG03h<2:1>.

Client Mode: USB Charging Type Detection

The PI3USB9201 supports client mode operation. Detection starts once REG01h Bit 3 is updated from 0 to 1. Device use D+ and D- voltage to determine the USB charging type attached, according to conditions stated in Table 3. Once the type of charger is detected, interrupt will trigger. The detection status is reported in REG02h.

PI3USB9201 support detection of Apple 1A, 2A, 2.4A and BC1.2 SDP/CDP/DCP type charger. In SDP/CDP, the USB channel will be ON, by default, upon detection is completed to enable data communication. This USB channel turn ON function could be overwritten by putting REG01h Bit 1 to “1”, to keep channel OFF upon detection is completed.

USB Path ON Mode

Under this mode of operation, the USB channel is ON. No detection will be reported.

Power Down Mode

Under this mode of operation, the USB channel is OFF. No detection will be reported.

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Maximum Ratings

Storage Temperature	-65°C to +150°C
Junction Temperature	-40°C to +125°C
Supply Voltage (V_{DD})	-0.3V to +6V
Switch I/O Voltage USB (D+/- & USB+/-)	-0.3V to +6V
Logic I/O Voltage (ENB/ADDR/SCL/SDA/INTB)	-0.3V to +6V
Switch I/O Current (Continuous) USB	50mA
ESD: (All pins)	2KV (HBM) and 1KV (CDM)

Note:
Stresses greater than those listed under MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

Recommended Operation Conditions

Symbol	Parameter	Min.	Max.	Units
V_{DD}	Core Supply Voltage	2.7	5.5	V
V_{SW}	Switch I/O Voltage (D+/- & USB+/-)	0	5.5	V
V_{LOGIC}	Logic I/O Voltage (ENB/ADDR/SCL/SDA/INTB)	0	5.5	V
T_A	Operating Temperature	-40	85	°C

DC Electrical Characteristics

Min and Max apply for T_A between -40°C to 85°C (unless otherwise noted). Typical values are referenced to T_A = +25°C, V_{DD} = 3.3V.

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Units
USB Data Switches						
R_{ONUSB}	USB Switch On-Resistance	I_{LOAD} = 8mA, $V_{I/O}$ = 0V, 0.4V		5	8	Ω
Δ Ron	On resistance between + and – channel	$V_{I/O}$ = 0V, 0.4V, I_{on} = –8 mA		0.5	1	Ω
Ron_Flat	ON resistance flatness	$V_{I/O}$ = 0V, 0.4V, I_{on} = –8 mA		0.2	0.5	Ω
Ioff	Power Off Leakage	V_{DD} = 0V, $V_{I/O}$ = 0V-5.5V	-5		5	µA
Ioz	Channel Off Leakage	ENB = 0V, $V_{I/O}$ = 0V-3.6V	-5		5	µA
Logic Pins						
V_{IH}	Input HIGH Voltage (ENB)	V_{DD} = 2.7V-5.5V	1.05			V
V_{IL}	Input LOW Voltage (ENB)	V_{DD} = 2.7V-5.5V			0.4	V
I_{IL}	Input Leakage Current (ENB)	V_I = 0V-5.5V	-5		5	µA
Current Consumption						
I_{CC}	Core Supply Current	Active Mode		200		µA
		Shut-down mode			1	µA

Note:
1. On-resistance is the voltage drop between the two terminals at the indicated current through the switch.
2. Limits based on electrical characterization data.

Capacitance

T_A = -40°C to 85°C

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Units
C_{ONUSB}	On Capacitance	f = 1MHz		5.0		pF

Switch Path AC Electrical Characteristics

Min and Max apply for T_A between -40°C to 85°C (unless otherwise noted). Typical values are referenced to T_A = +25°C, V_{DD} = 3.3V.

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Units
BW_{USB}	-3dB Bandwidth of USB channel			2000		MHz
DDIL	Insertion Loss	f = 240MHz		-0.8		dB

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Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Units
DDRL	Differential Return Loss	f = 240MHz		-15		dB
DDOFFI	Differential OFF Isolation	f = 240MHz		-28		dB
DDONI	Channel to Channel Isolation	f = 240MHz		-35		dB
T_{INT_MSK}	Time after INT Mask Cleared to "0" until INTB Goes LOW to Signal the Interrupt after Interruptible Event while INT Mask Bit Set to "1"			10		ms

USB Path Switching Characteristics

Min and Max apply for T_A between -40°C to 85°C (unless otherwise noted). Typical values are referenced to T_A = +25°C, V_{DD} = 3.3V.

Parameters	Description	Test Conditions	Min.	Typ.	Max.	Units
t_{PZH}, t_{PZL}	Chip Enable Time (2)				500	us
t_{PHZ}, t_{PLZ}	Turn-On Time (3)	ENB = 0, From Power-Off to USB Path ON		50		us
t_{PHZ}, t_{PLZ}	Turn-OFF Time (3)	ENB = 0, From USB Path ON to Power-Off		20		us
t_{Pd}	Propagation Delay	See Test Circuit for Electrical Characteristics		250		ps
t_{b-b}	Bit-to-bit Skew Within the Same Differential Pair (1)			8	20	ps

Note:
1) Guaranteed by design.
2) Time the chip takes to be ready for operation from power-up or disable.
3) Measured after I^2C acknowledgement is received.

BC1.2 Electrical Characteristics

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Units
$R_{DP\_DM\_SHORT}$	D+/- shorting resistance			140	200	Ω
V_{DM_SRC}	D- output voltage	ENB = 0; Reg00h b3: b1 = 011; V_{D+} = 0.6V; I_{D-} = 250uA to GND	0.5		0.7	V
V_{DP_SRC}	D+ output voltage	ENB = 0; Reg00h b3: b1 = 100; with D+/- short with 200ohm; I_{D+} = 250uA to GND; measured at D+ after INTB = 0V (i.e. DCP is detected)	0.5		0.7	V

I^2C Controller DC Electrical Characteristics

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Units
Input SCL, input/output SDA						
V_{IL_I2C}	Low-level Input Voltage (SCL&SDA&ADDR)				0.3	V
V_{IH_I2C}	High-level Input Voltage (SCL&SDA&ADDR)		1.05			V
I_{OL_I2C}	SDA Low-level Output Current	V_{OL}= 0.4V	20			mA
I_{L_I2C}	Leakage Current	V_{IN} = V_{DD} or 0	-1		1	µA
C_{i_I2C}	Input Capacitance	V_{IN} = 0		2.4		pF
Interrupt INTB						

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Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Units
I_{OL_INT}	Low-level Output Current	V_{OL} = 0.4V	3			mA
C_o	Output Capacitance			7		pF

I2C AC Electrical Characteristics Symbol

Symbol	Parameter	Standard mode I²C		Fast mode I²C		Fast mode Plus I²C		Unit
		Min	Max	Min	Max	Min	Max	
f_{SCL}	SCL clock frequency	0	100	0	400	0	1000	kHz
t_{BUF}	bus free time between a STOP and START condition	4.7		1.3		0.5		µs
$t_{HD;STA}$	hold time (repeated) START condition	4.0		0.6		0.26		µs
$t_{SU;STA}$	set-up time for a repeated START condition	4.7		0.6		0.26		µs
$t_{SU;STO}$	set-up time for STOP condition	4.0		0.6		0.26		µs
$t_{VD;ACK}$[1]	data valid acknowledge time		3.45		0.9		0.45	µs
$t_{HD;DAT}$[2]	data hold time	0		0		0		ns
$t_{VD;DAT}$	data valid time		3.45		0.9		0.45	ns
$t_{SU;DAT}$	data set-up time	250		100		50		ns
t_{LOW}	LOW period of the SCL clock	4.7		1.3		0.5		µs
t_{HIGH}	HIGH period of the SCL clock	4.0		0.6		0.26		µs
t_f	fall time of both SDA and SCL signals		300		300		120	ns
t_r	rise time of both SDA and SCL signals		1000		300		120	ns
t_{SP}	pulse width of spikes that must be suppressed by the input filter		50		50		50	ns

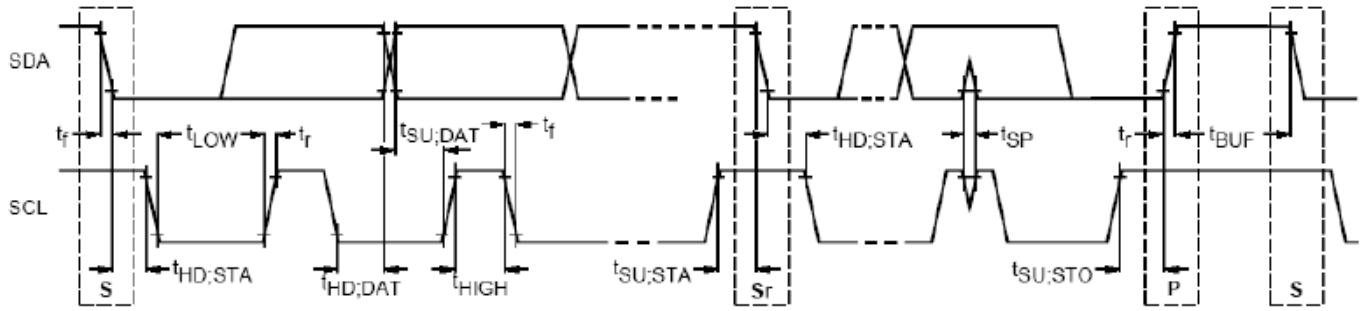

Figure 1. Definition of Timing for Full-Speed Mode Devices on the I²C Bus

Table 1. I²C Slave Address

Name	Size (Bits)	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Slave Address #1 (ADDR=SCL)	8	1	0	1	1	1	0	0	R/W
Slave Address #2 (ADDR=SDA)		1	0	1	1	1	0	1	R/W
Slave Address #3 (ADDR=VDD)	8	1	0	1	1	1	1	0	R/W
Slave Address #4 (ADDR=GND)		1	0	1	1	1	1	1	R/W

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Bus Transaction

Writing to the Port Registers

Data is transmitted to the PI3USB9201 by sending the device address and setting the least significant bit to a logic 0. The command byte is sent after the address and determines which register will receive the data following the command byte.

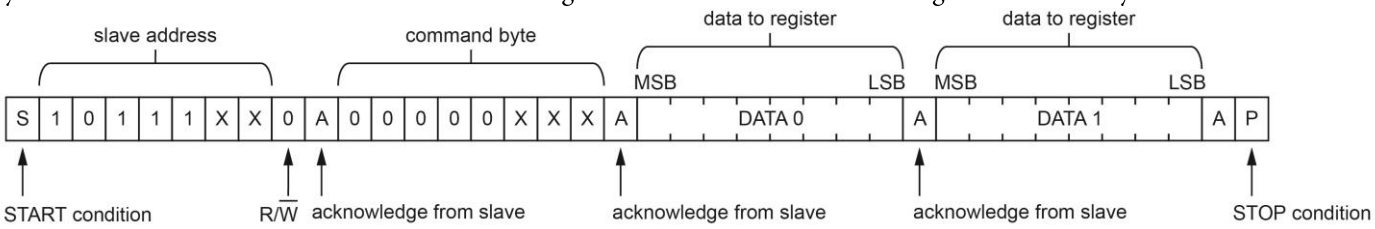

Figure 2. Write to Output Port Register

Reading the Port Register

In order to read data from the PI3USB9201, the bus master must first send the PI3USB9201 address with the least significant bit set to a logic 0. The command byte is sent after the address and determines which register will be accessed. After a restart, the device address is sent again, but this time the lease significant bit is set to a logic 1. Data from the register defined by the command byte will then be sent by the PI3USB9201. Data is clocked into the register on the falling edge of the acknowledge clock pulse.

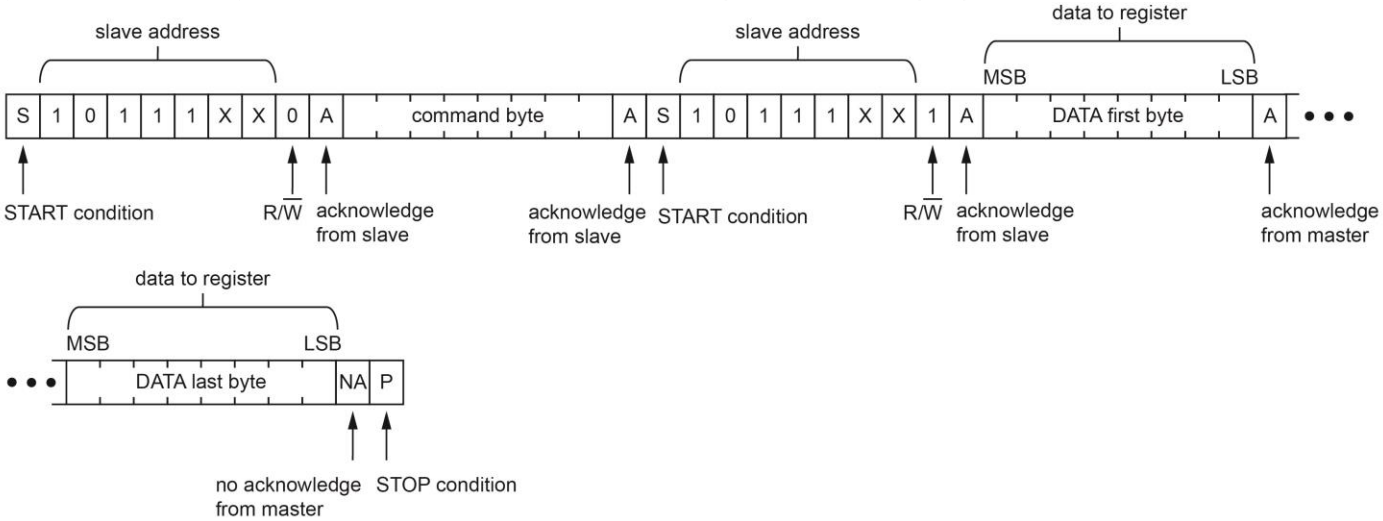

Figure 3. Read from Register

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Table 2. Registers Map

Address	Register	Type	Reset Value	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
00h	Control 1	Write/Read	00h	Reserved	Reserved	Reserved	Reserved	000=Power Down 001=SDP Host Mode 010=DCP Host Mode 011=CDP Host Mode 100=Client Mode 101=reserved 110=reserved 111=USB Path ON			1=Interrupt Mask
01h	Control 2	Write/Read	00h	Reserved	Reserved	Reserved	Reserved	0=Client mode No detection 1=Client mode detection (1)	Reserved	0=Enable USB switch auto ON 1=Disable USB switch auto ON (2)	Reserved
02h	Client Status (3)	Read & Clear	00h	1=DCP Detected	1=SDP Detected	1=CDP Detected	Reserved	1=1A Charger Detected	1=2A Charger Detected	1=2.4A Charger Detected	Others Detected
03h	Host Status(3)	Read & Clear	00h	Reserved	Reserved	Reserved	Reserved	Reserved	1=Unplug observed in Host mode SDP/CDP	1=Plug observed in Host mode SDP/CDP	1=BC1.2 detect pulse observed in Host mode SDP/CDP

Notes:

1) Write 01h bit3 form 0 to 1 for Client mode detect after 00h bit 3-1 = 100 Client mode. For USB-C application, write 1 to 01h bit3 when the system in ATTACHED.SNK state. Write 0 to 01h bit3 when it leaves ATTACHED.SNK state. For non-USB-C application, write 1 to 01h bit3 when the system detects the existence of VBUS. Write 0 to 01h bit3 when VBUS is removed.

2) Host mode SDP/CDP data switch on at 01h bit1 = 0 and switch off at 01h bit1 = 1; Client mode data switch will on after BC1.2 detect at 01h bit1 = 0 and keeps off at 01h bit1 = 1. Host mode DCP data switch keeps off ignore 01h bit1 = 0 or 1. USB path on mode data switch keeps on ignore 01h bit1 = 0 or 1

3) Client/Host Status registers will be cleared after I2C read.

4) For USB-C application, after CC detector detects detach, please program PI3USB9201 to “Power Down” mode.

Table 3. State of Operation

Reg00h[3:1]			States		USB Switch	D+/- Short
0	0	0	Power Down		OFF	OFF
0	0	1	SDP Host		ON	OFF
0	1	0	DCP Host		OFF	ON
0	1	1	CDP Host		ON	OFF
1	0	0	Client Mode (1A)	D+ = 2V; D- = 2.7V	OFF	OFF
			Client Mode (2A)	D+ = 2.7V; D- = 2V		
			Client Mode (2.4A)	D+ = 2.7V; D- = 2.7V		
			Client Mode (SDP)	D+/- < 1.7V (1)	ON	
			Client Mode (DCP)		OFF	
			Client Mode (CDP)		ON	
			Client Mode (Others)		OFF	
1	1	1	USB Path ON		ON	OFF

Note:

1) PI3USB9201 follows the Battery Charging 1.2 Specification, using D+/- to determine what is attached. Data Contact Detect, Primary Detection and Secondary Detection included.

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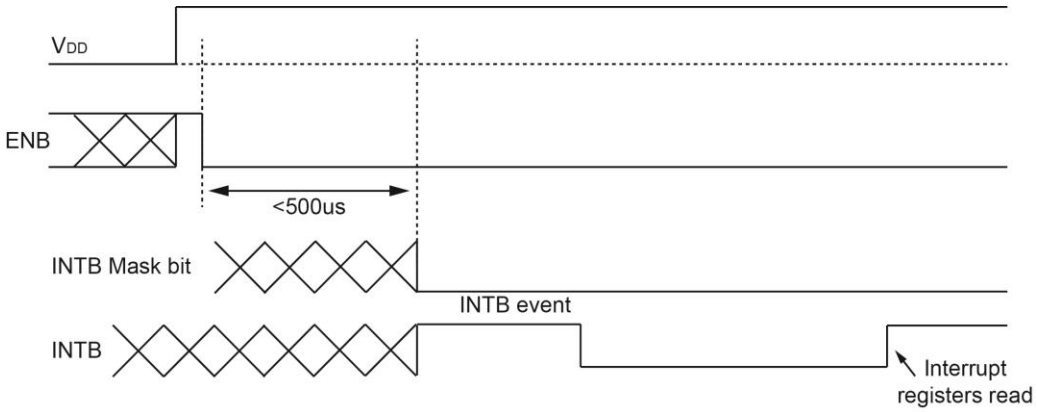

Figure 4. Power up INTB Timing Diagram

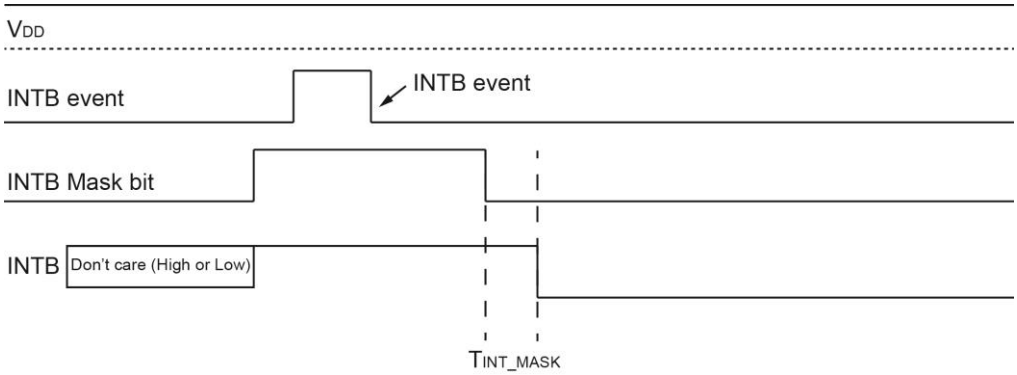

Figure 5. INT Mask to INTB Timing Diagram

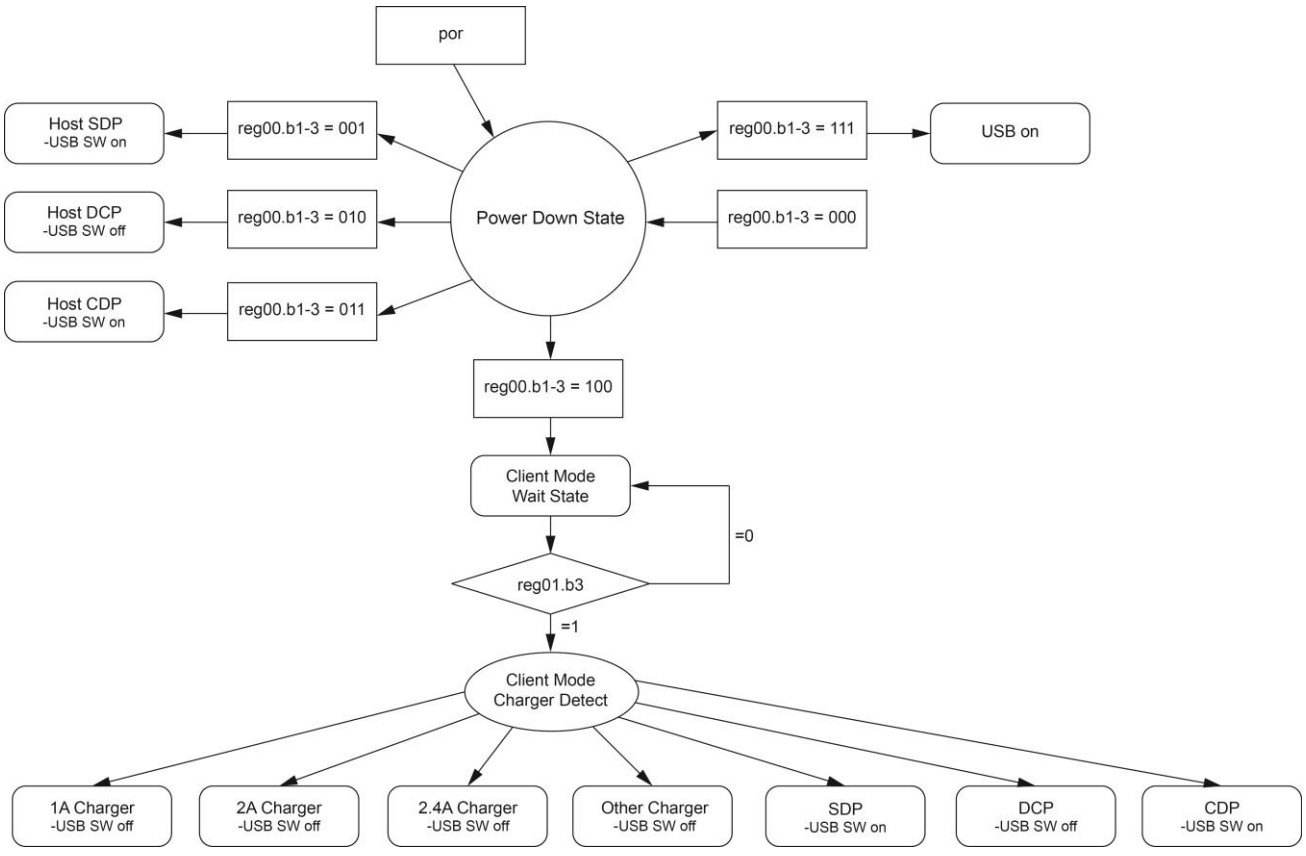

Figure 6. Flowchart

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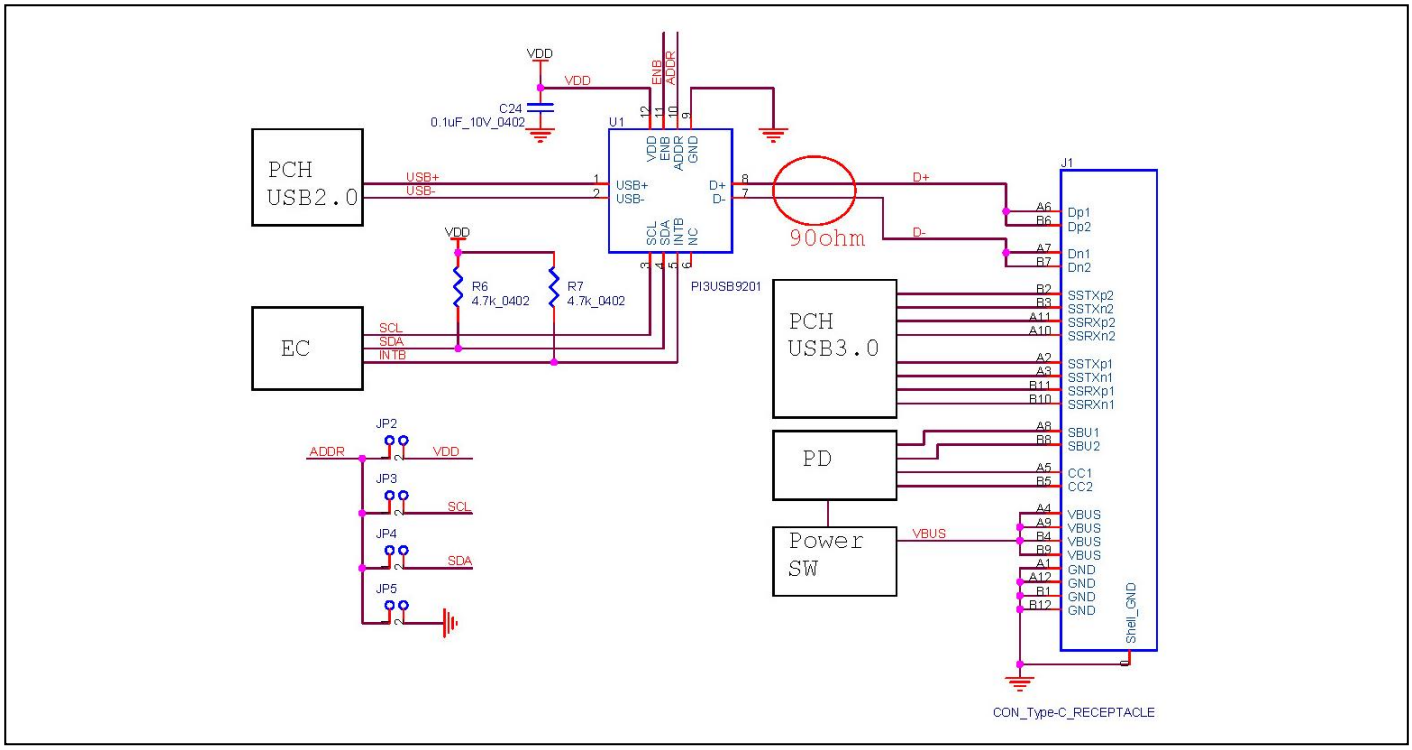
Application Diagram



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Part Marking

wU = PI3USB9201ZTAE

Z: Die Rev
Y: Date Code (Year)
W: Date Code (Workweek)

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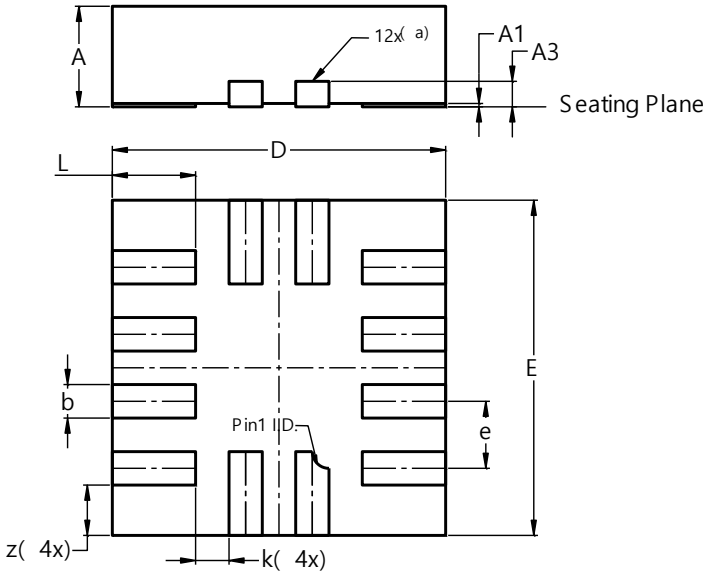
Packaging Mechanical

12-UQFN (ZTA)



Note (a) Actual shape dependent upon the manufacturing technology used.

U-QFN2020-12 (Type C)			
Dim	**Min**	**Max**	**Typ**
A	0.55	0.65	0.60
A1	0.00	0.05	0.02
A3	--	--	0.152
b	0.15	0.25	0.20
D	1.95	2.05	2.00
E	1.95	2.05	2.00
e	0.40 BSC		
L	0.45	0.55	0.50
k	--	--	0.20
z	--	--	0.30
All Dimensions in mm			

For latest package info.

please check: http://www.diodes.com/design/support/packaging/pericom-packaging/packaging-mechanicals-and-thermal-characteristics/

Ordering Information

Orderable Part Numbers	Package Code	Package Description
PI3USB9201ZTAEX	ZTA	12-Pin, 2x2mm (UQFN)

Notes:

1. No purposely added lead. Fully EU Directive 2002/95/EC (RoHS), 2011/65/EU (RoHS 2) & 2015/863/EU (RoHS 3) compliant.
2. See https://www.diodes.com/quality/lead-free/ for more information about Diodes Incorporated's definitions of Halogen- and Antimony-free, "Green" and Lead-free.
3. Halogen- and Antimony-free "Green" products are defined as those which contain <900ppm bromine, <900ppm chlorine (<1500ppm total Br + Cl) and <1000ppm antimony compounds.
4. E = Pb-free and Green
5. X suffix = Tape/Reel

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