# Precision 24 MHz CMOS Rail-to-Rail Input/Output Operational Amplifiers

## Features

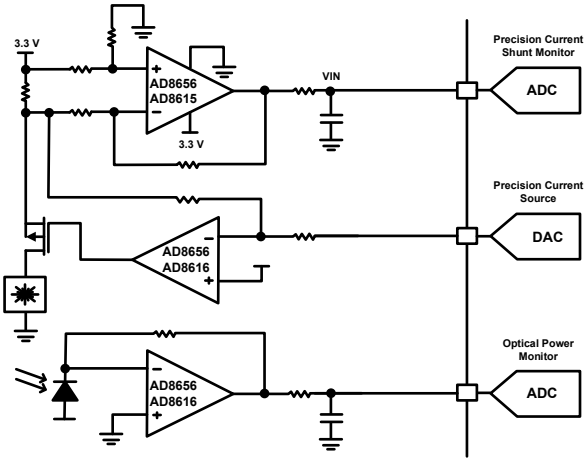
- Continuous Time Amplifier, No Chopper or Auto-zero Glitch
- Low Offset Voltage: 50 µV max
- Low Offset Voltage Drift: 0.2 µV/°C
  1 µV/°C max
- Low Input Bias Current: 0.6 pA
  3 pA max
- Low Noise: 6 nV/√Hz @1 kHz
  4 nV/√Hz @10 kHz
  0.1 Hz to 10 Hz 1.4 $\mu V_{P-P}$
- High Unit Gain Bandwidth: 24 MHz
- High Slew Rate: 6.8 V/µs
- Fast Settling Time: 0.5 µs to 0.01%
- Supply Current: 1.8 mA per amplifier
- Wide Supply Voltage: 2.7 V to 5.5 V; ±1.35 V to ±2.75 V
- Rail-to-rail Input and Output
- Drive Large Capacitive Load Up to 10 nF
- Large Output Current: ±150 mA
- Wide Temperature Range: -40 °C to +125 °C

## Applications

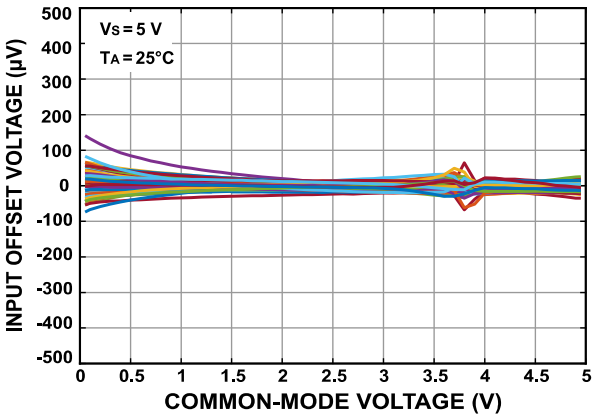
- Multi-parameter Patient Monitor
- Chemistry and Gas Analyzer
- Multi-pole Filters
- Sensor Analog Front End
- ASIC Input or Output Amplifiers
- ADC Input Driver and DAC Output Buffer
- Photodiode Trans-impedance Amplifier

| Model | Channels | Package |
|---|---|---|
| AD8616 | 1 | SOT23-5 |
| AD8656 | 1 | SOT23-5 |
| | 2 | SOIC-8/MSOP-8 |
| | 4 | SOIC-14/TSSOP-14 |

## Typical Application




## Typical Characteristics



## Pin Configurations and Function

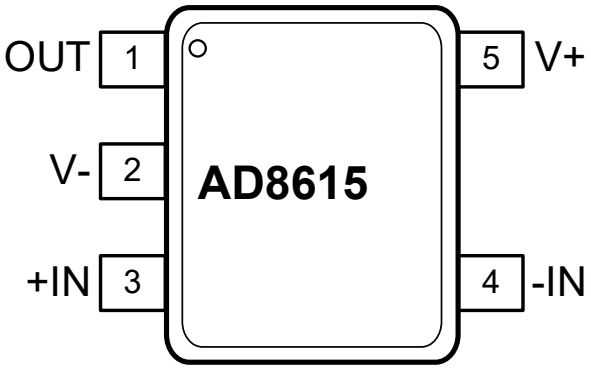



Figure 1. AD8615 Pin Configuration (5-lead SOT23)

| Mnemonic | Pin No. | I/O[1] | Description |
|---|---|---|---|
| OUT | 1 | AO | Amplifier output |
| V- | 2 | P | Negative power supply |
| +IN | 3 | AI | Amplifier non-inverting input |
| -IN | 4 | AI | Amplifier inverting input |
| V+ | 5 | P | Positive power supply |

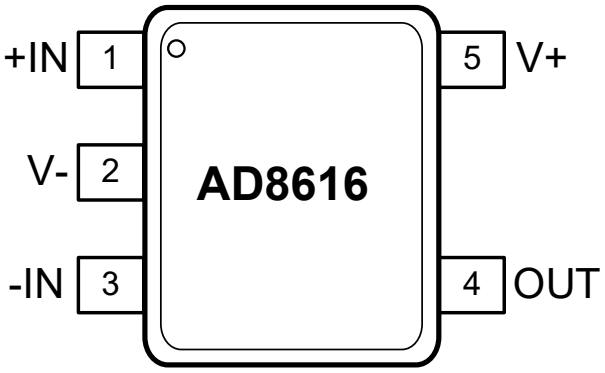



Figure 2. AD8616 Pin Configuration (5-lead SOT23)

| Mnemonic | Pin No. | I/O[1] | Description |
|---|---|---|---|
| +IN | 1 | AI | Amplifier non-inverting input |
| V- | 2 | P | Negative power supply |
| -IN | 3 | AI | Amplifier inverting input |
| OUT | 4 | AO | Amplifier output |
| V+ | 5 | P | Positive power supply |

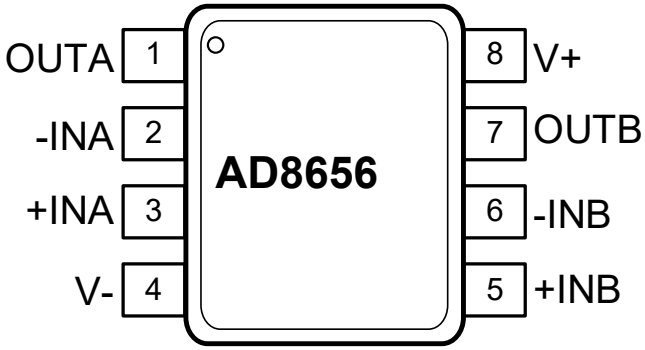



Figure 3. AD8656 Pin Configuration (8-lead SOIC and MSOP)

| Mnemonic | Pin No. | I/O[1] | Description |
|---|---|---|---|
| OUTA | 1 | AO | Channel A output |
| -INA | 2 | AI | Channel A inverting input |
| +INA | 3 | AI | Channel A Non-inverting input |
| V- | 4 | P | Negative power supply |
| +INB | 5 | AI | Channel B Non-inverting input |
| -INB | 6 | AI | Channel B inverting input |
| OUTB | 7 | AO | Channel B output |
| V+ | 8 | P | Positive power supply |

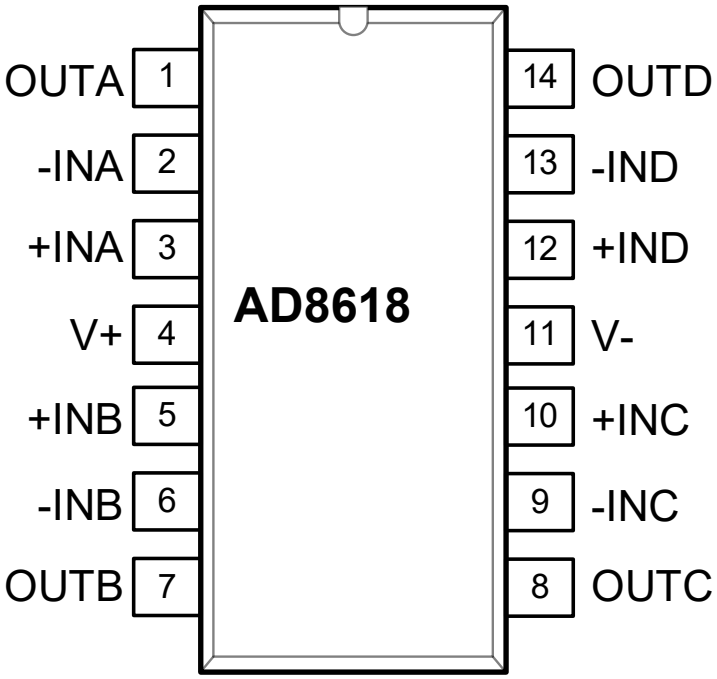



Figure 4. AD8616 Pin Configuration (14-lead SOIC and TSSOP)

| Mnemonic | Pin No. | I/O[1] | Description |
|---|---|---|---|
| OUTA | 1 | AO | Channel A output |
| -INA | 2 | AI | Channel A inverting input |
| +INA | 3 | AI | Channel A non-inverting input |
| V+ | 4 | P- | Positive power supply |
| +INB | 5 | AI | Channel B non-inverting input |
| -INB | 6 | AI | Channel B inverting input |
| OUTB | 7 | AO | Channel B output |
| OUTC | 8 | AO | Channel C output |
| -INC | 9 | AI | Channel C inverting input |
| +INC | 10 | AI | Channel C non-inverting input |
| V- | 11 | P | Negative power supply |
| +IND | 12 | AI | Channel D non-inverting input |
| -IND | 13 | AI | Channel D inverting input |
| OUTD | 14 | AO | Channel D output |

## Absolute Maximum Ratings

| Parameter | Rating |
|---|---|
| Supply Voltage | 6 V |
| Input Voltage | V- to V+ |
| Output Short-Circuit Duration to GND | Indefinite |
| Operating Temperature Range | -40 °C to 125 °C |
| Storage Temperature Range | -65 °C to 150 °C |
| Junction Temperature Range | -65 °C to 150 °C |
| Lead Temperature, Soldering (10 sec) | 300 °C |
| ESD Rating (ESD) | |
| Human Body Model (HBM) | 6 kV |
| Charge Device Model (CDM) | 2 kV |

## Thermal Resistance

| Package Type | $\theta_{JA}$ | $\theta_{JC}$ | Unit |
|---|---|---|---|
| 5-lead SOT23 | 230 | 76 | °C/W |
| 8-lead SOIC | 158 | 43 | °C/W |
| 8-lead MSOP | 190 | 44 | °C/W |
| 14-lead SOIC | 120 | 36 | °C/W |
| 14-lead TSSOP | 240 | 43 | °C/W |

## Specifications

The ● denotes the specification which apply over the full operating temperature range, otherwise specifications are at $V_S$ = 5 V, $V_{CM}$ = $V_S$ / 2, $T_A$ = 25 °C, unless otherwise noted.

| Parameter | Symbol | Conditions | | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|---|
| **INPUT CHARACTERISTICS** | | | | | | | |
| Offset Voltage | $V_{OS}$ | $V_{CM}$ = 2.5 V and 4.5 V | <br>● | | 10<br>70 | 50<br>150 | µV<br>µV |
| | | $V_{CM}$ = 0 V to 5 V | ● | | | 500 | µV |
| Offset Voltage Drift | $\Delta V_{OS}/\Delta T$ | -40 °C < $T_A$ < +125 °C | ● | | 0.2 | 1 | µV/°C |
| Input Bias Current | $I_B$ | | <br>● | | 0.6 | 3<br>1000 | pA<br>pA |
| | | -40 °C < $T_A$ < +85 °C | | | | 80 | pA |
| Input Offset Current | $I_{OS}$ | | <br>● | | | 5<br>400 | pA<br>pA |
| | | -40 °C < $T_A$ < +85 °C | | | | 20 | pA |
| Input Capacitance | $C_{DIFF}$ | Differential | | | 3.2 | | pF |
| | $C_{CM}$ | Common-Mode | | | 7.4 | | pF |
| Input Voltage Range | IVR | | | 0 | | 5 | V |
| Common-Mode Rejection Ratio | CMRR | $V_{CM}$ = 0 V to 4.5 V | | 80 | 105 | | dB |
| Large Signal Voltage Gain | $A_{VO}$ | $R_L$ = 2 kΩ, $V_O$ = 0.5 V to 4.5 V | | 110 | 140 | | dB |
| **OUTPUT CHARACTERISTICS** | | | | | | | |
| Output Voltage High | $V_{OH}$ | $I_L$ = 1 mA | <br>● | 4.98<br>4.97 | 4.988 | | V<br>V |
| | | $I_L$ = 10 mA | <br>● | 4.85<br>4.80 | 4.895 | | V<br>V |
| Output Voltage Low | $V_{OL}$ | $I_L$ = 1 mA | <br>● | | 12 | 20<br>30 | mV<br>mV |
| | | $I_L$ = 10 mA | <br>● | | 105 | 150<br>200 | mV<br>mV |
| Output Current | $I_{OUT}$ | | | | ±150 | | mA |
| Closed-Loop Output Impedance | $Z_{OUT}$ | f = 1 MHz, $A_V$ = 1 | | | 5.6 | | Ω |
| **POWER SUPPLY** | | | | | | | |
| Supply Current Per Amplifier | $I_S$ | $I_{OUT}$ = 0 mA | <br>● | | 1.8 | 2<br>2.1 | mA<br>mA |
| Power Supply Rejection Ratio | PSRR | $V_S$ = 2.7 V to 5.5 V | | 80 | 103 | | dB |
| **DYNAMIC PERFORMANCE** | | | | | | | |
| Slew Rate | SR | $R_L$ = 2 kΩ | | | 6.8 | | V/µs |
| Unit Gain Bandwidth | UGB | | | | 24 | | MHz |
| Settling Time | | To 0.01% | | | 0.5 | | µs |
| THD + Noise | THD + N | | | | 0.0004 | | % |
| Phase Margin | $\Phi_M$ | | | | 49 | | Degree |
| Channel Separation | $C_S$ | f = 10 kHz | | | -115 | | dB |
| | | f = 100 kHz | | | -110 | | dB |
| **NOISE PERFORMANCE** | | | | | | | |
| Voltage Noise Density | $e_n$ | f = 1 kHz | | | 6 | | $nV/\sqrt{Hz}$ |
| | | f = 10 kHz | | | 4.2 | | $nV/\sqrt{Hz}$ |
| Peak-to-Peak Voltage Noise | $e_{nP-P}$ | 0.1 Hz to 10 Hz | | | 1.4 | | $\mu V_{P-P}$ |
| Current Noise Density | $i_n$ | f = 1 kHz | | | 0.4 | | $fA/\sqrt{Hz}$ |

The ● denotes the specification which apply over the full operating temperature range, otherwise specifications are at $V_S$ = 2.7 V, $V_{CM}$ = $V_S$ / 2, $T_A$ = 25 °C, unless otherwise noted.

| Parameter | Symbol | Conditions | | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|---|
| **INPUT CHARACTERISTICS** | | | | | | | |
| Offset Voltage | $V_{OS}$ | Vs = 3.5 V, $V_{CM}$ = 1.75 V and 3.0 V | | | 40 | 160 | µV |
| | | Vs = 2.7 V, $V_{CM}$ = 0 V to 2.7 V | ● | | | 500 | µV |
| Offset Voltage Drift | $\Delta V_{OS}/\Delta T$ | -40 °C < $T_A$ < +125 °C | ● | | 0.2 | 1 | µV/°C |
| Input Bias Current | $I_B$ | | ● | | 0.6 | 3<br>1000 | pA<br>pA |
| | | -40 °C <$T_A$ < +85 °C | | | | 80 | pA |
| Input Offset Current | $I_{OS}$ | | ● | | | 5<br>400 | pA<br>pA |
| | | -40 °C < $T_A$ < +85 °C | | | | 20 | pA |
| Input Capacitance | $C_{DIFF}$ | Differential | | | 3.2 | | pF |
| | $C_{CM}$ | Common-Mode | | | 7.4 | | pF |
| Input Voltage Range | IVR | | | 0 | | 2.7 | V |
| Common-Mode Rejection Ratio | CMRR | $V_{CM}$ = 0 V to 2.2 V | | 70 | 95 | | dB |
| Large Signal Voltage Gain | $A_{VO}$ | $R_L$ = 2 kΩ, $V_O$ = 0.5 V to 2.2 V | | 100 | 135 | | dB |
| **OUTPUT CHARACTERISTICS** | | | | | | | |
| Output Voltage High | $V_{OH}$ | $I_L$ = 1 mA | ● | 2.65<br>2.65 | 2.683 | | V<br>V |
| Output Voltage Low | $V_{OL}$ | $I_L$ = 1 mA | ● | | 17 | 50<br>50 | mV<br>mV |
| Output Current | $I_{OUT}$ | | | | ±50 | | mA |
| Closed-Loop Output Impedance | $Z_{OUT}$ | f = 1 MHz, $A_V$ = 1 | | | 5.6 | | Ω |
| **POWER SUPPLY** | | | | | | | |
| Supply Current Per Amplifier | $I_S$ | $I_{OUT}$ = 0 mA | ● | | 1.8 | 2<br>2.1 | mA<br>mA |
| Power Supply Rejection Ratio | PSRR | $V_S$ = 2.7 V to 5.5 V | | 80 | 103 | | dB |
| **DYNAMIC PERFORMANCE** | | | | | | | |
| Slew Rate | SR | $R_L$ = 2 kΩ | | | 6.8 | | V/µs |
| Unit Gain Bandwidth | UGB | | | | 24 | | MHz |
| Settling Time | | To 0.01% | | | 0.5 | | µs |
| THD + Noise | THD + N | | | | 0.0004 | | % |
| Phase Margin | $\Phi_M$ | | | | 43 | | Degree |
| Channel Separation | $C_S$ | f = 10 kHz | | | -115 | | dB |
| | | f = 100 kHz | | | -110 | | dB |
| **NOISE PERFORMANCE** | | | | | | | |
| Voltage Noise Density | $e_n$ | f = 1 kHz | | | 6 | | $nV/\sqrt{Hz}$ |
| | | f = 10 kHz | | | 4.2 | | $nV/\sqrt{Hz}$ |
| Current Noise Density | $i_n$ | f = 1 kHz | | | 0.4 | | $fA/\sqrt{Hz}$ |
| Peak-to-Peak Voltage Noise | $e_{nP-P}$ | 0.1 Hz to 10 Hz | | | 1.4 | | $\mu V_{P-P}$ |

## Typical Performance Characteristics

Unless otherwise stated, $T_A$ = 25 °C, $V_S$ = 5 V, $R_L$ = 2 kΩ.

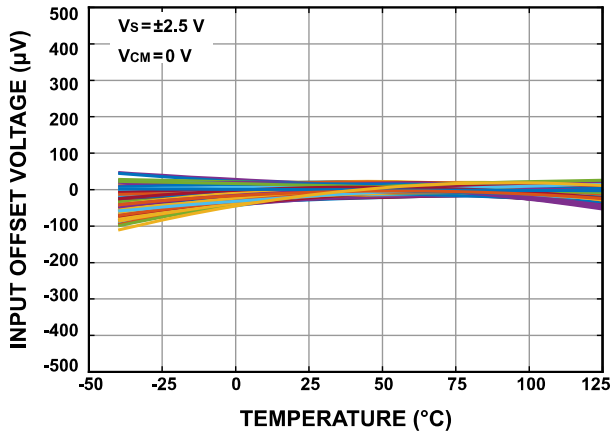



Figure 5. Input Offset Voltage vs. Temperature

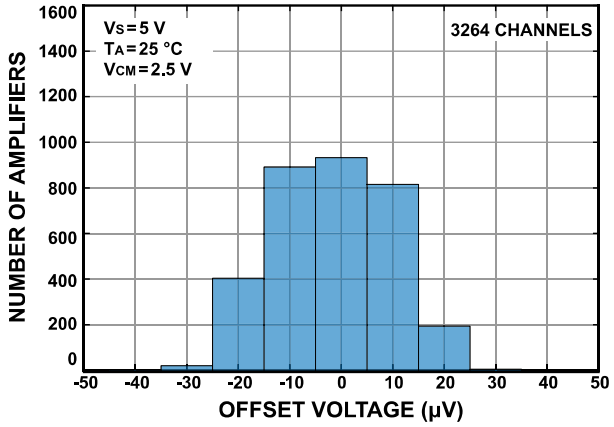



Figure 6. Input Offset Voltage Distribution

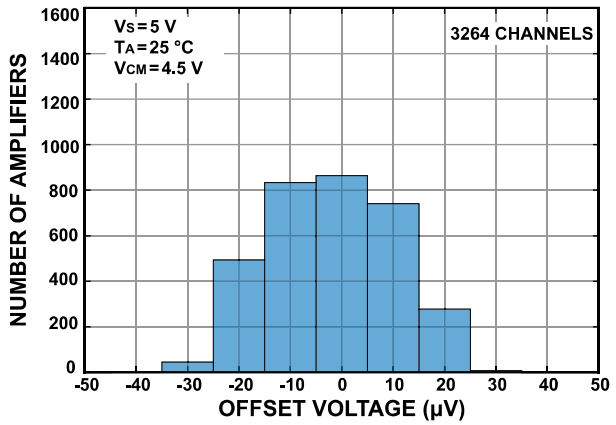



Figure 7. Input Offset Voltage Distribution

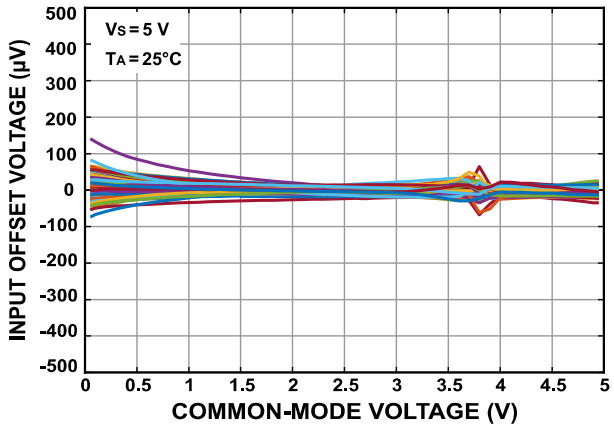



Figure 8. Input Offset vs. Common Mode Voltage

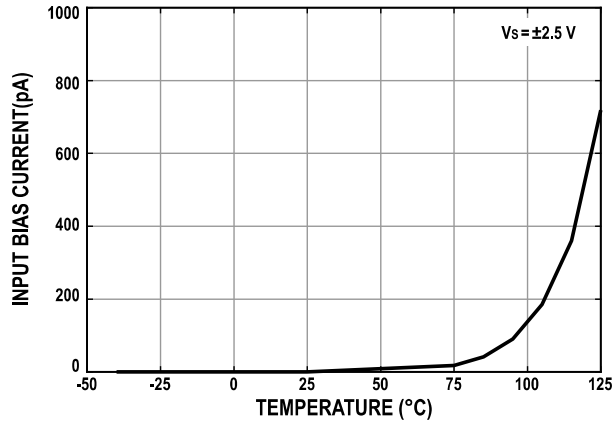



Figure 9. Input Bias Current vs. Temperature

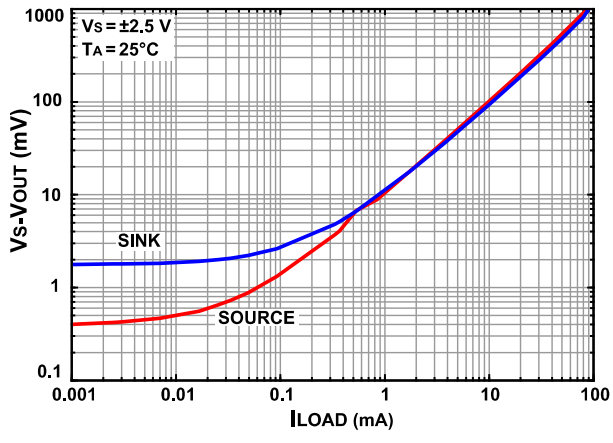



Figure 10. Output Voltage to Supply Rail vs. Load Current

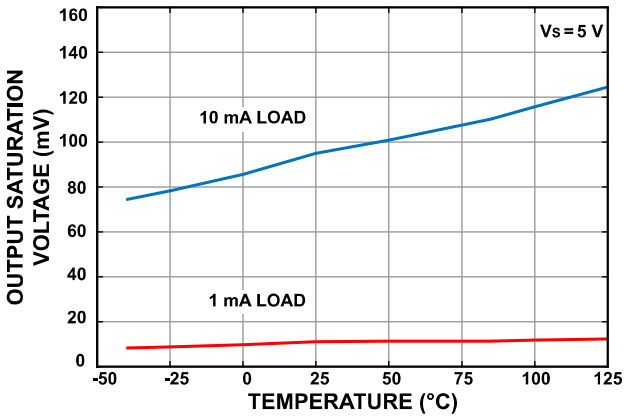



Figure 11. Output Saturation Voltage vs. Temperature

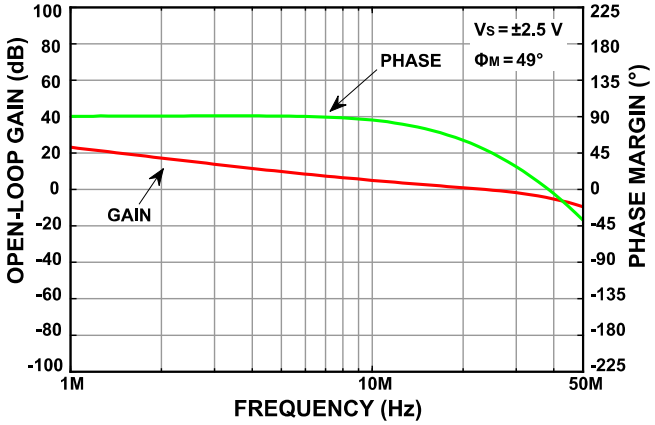



Figure 12. Open-Loop Gain and Phase vs. Frequency

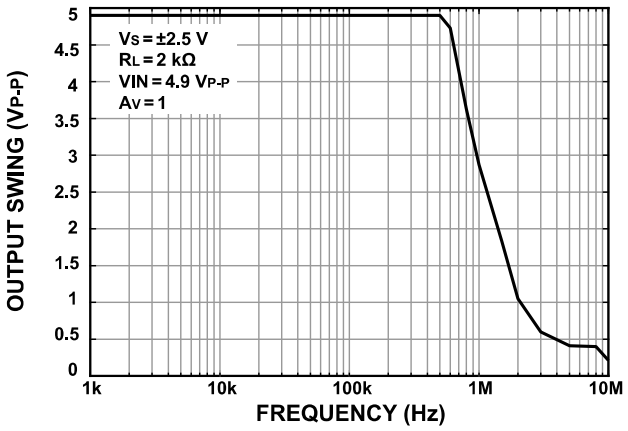



Figure 13. Close-Loop Output Swing vs. Frequency

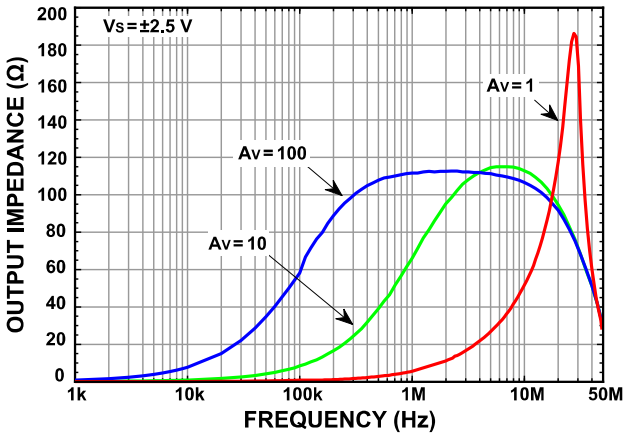



Figure 14. Output Impedance vs. Frequency

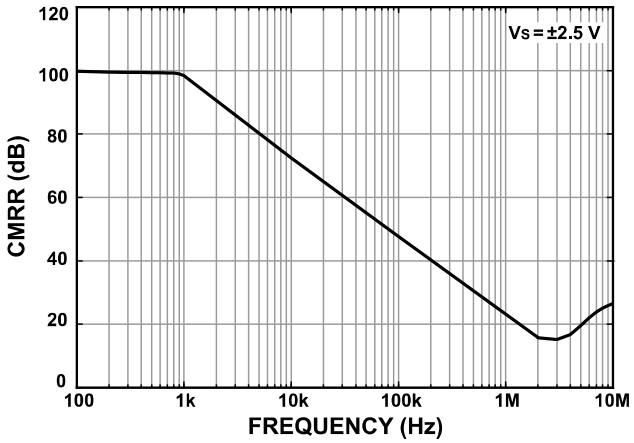



Figure 15. CMRR vs. Frequency

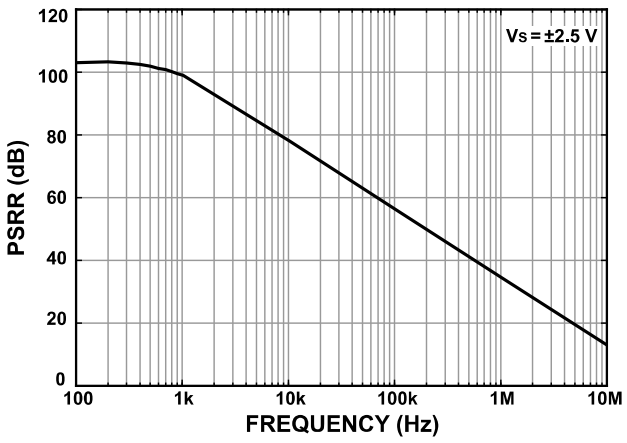



Figure 16. PSRR vs. Frequency

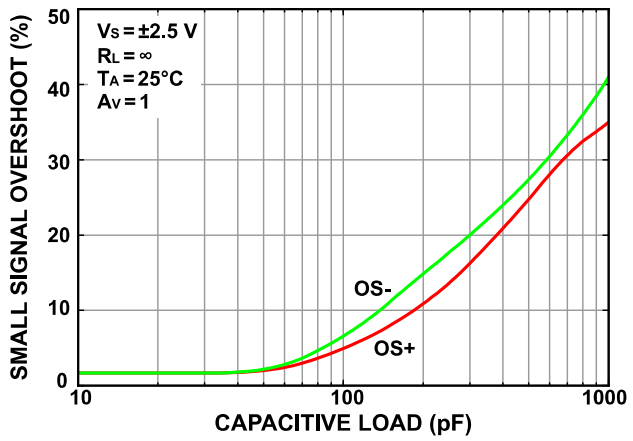



Figure 17. Small-Signal Overshoot vs. Load Capacitance

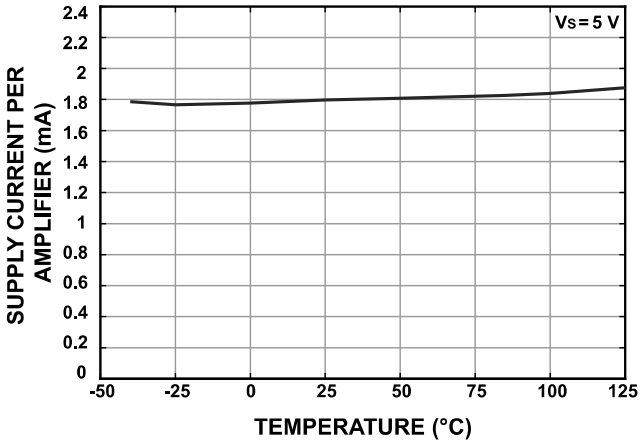



Figure 18. Supply Current vs. Temperature

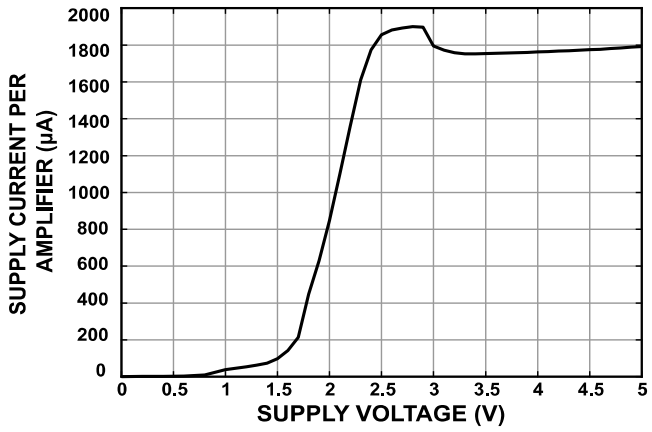



Figure 19. Supply Current per Amplifier vs. Supply Voltage

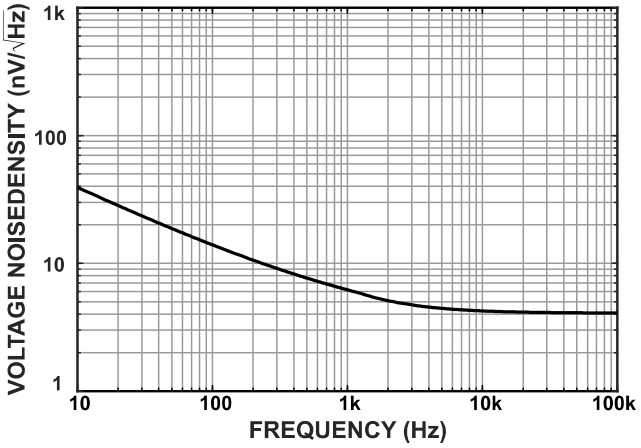



Figure 20. Voltage Noise Density vs. Frequency

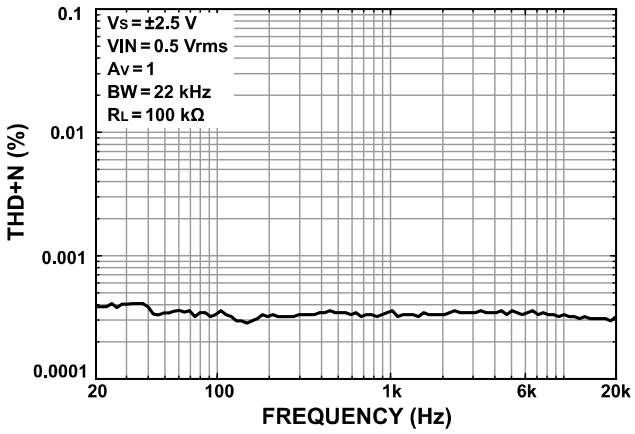



Figure 21. THD+Noise vs. Frequency

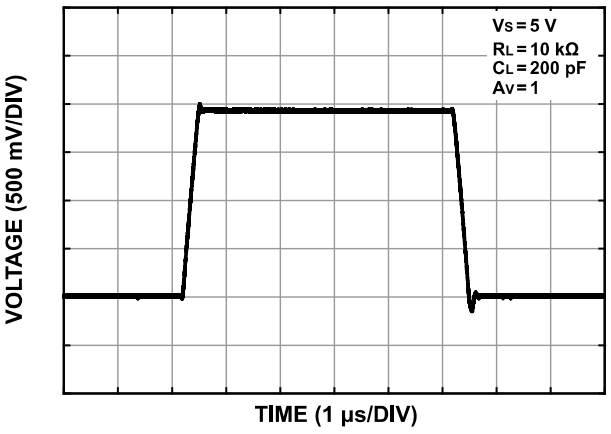



Figure 22. Large Signal Transient Response

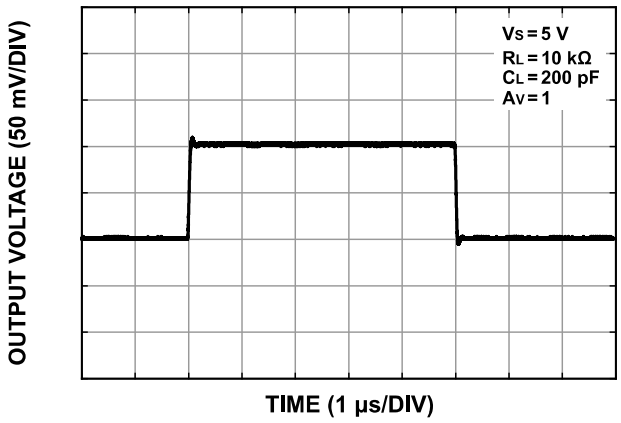



Figure 23. Small Signal Transient Response

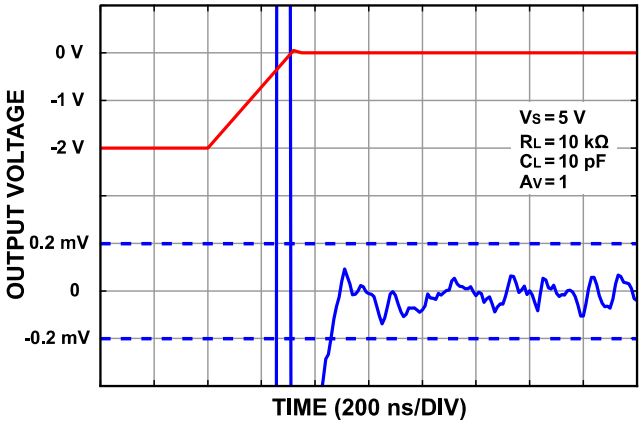



Figure 24. Rising Edge Settling

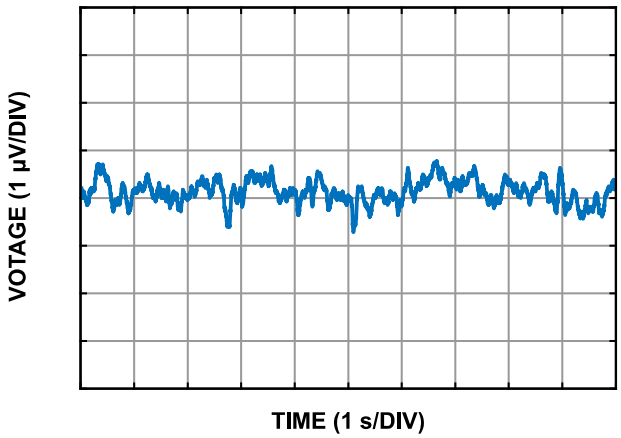



Figure 25. 0.1 Hz to 10 Hz Input Voltage Noise

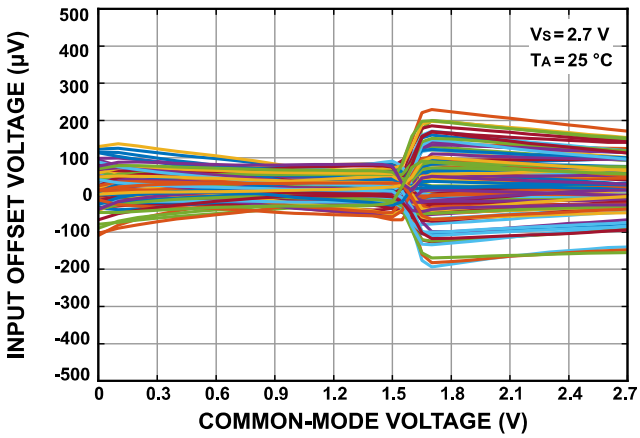



Figure 26. Input Offset vs. Common-Mode Voltage

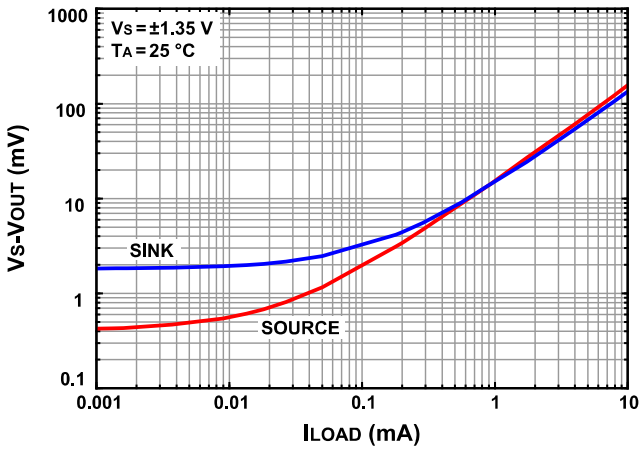



Figure 27. Output Saturation Voltage vs. Temperature

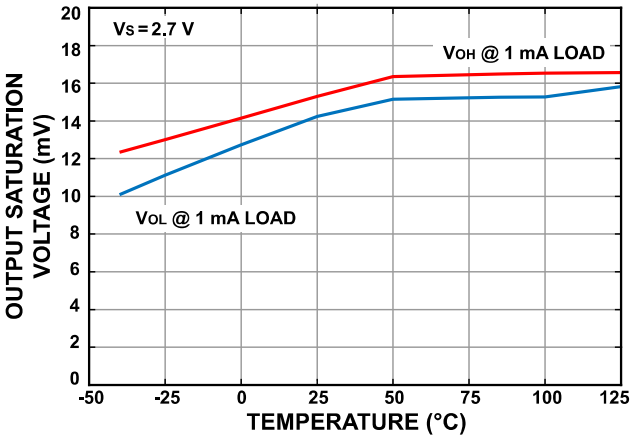



Figure 28. Output Saturation Voltage vs. Temperature

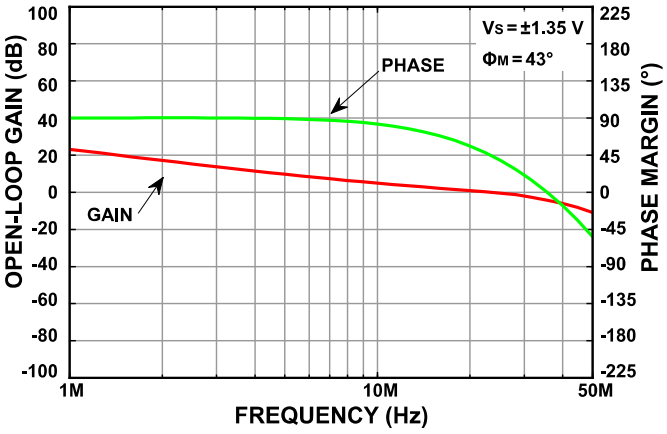



Figure 29. Open-Loop Gain and Phase vs. Frequency

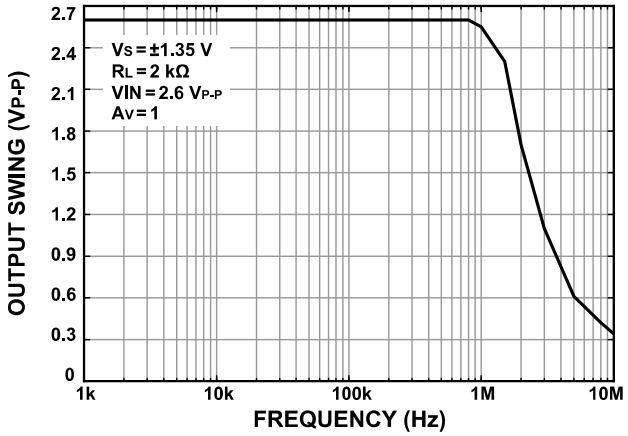



Figure 30. Close-Loop Output Swing vs. Frequency

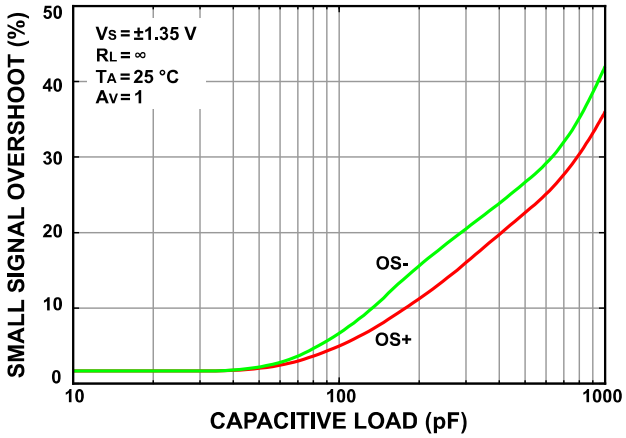



Figure 31. Small-Signal Overshoot vs. Load Capacitance

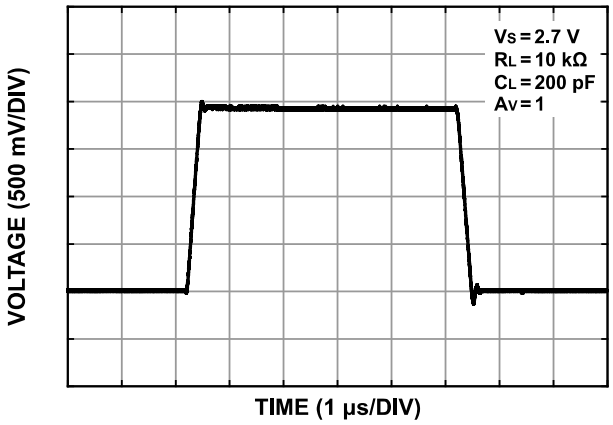



Figure 32. Large Signal Transient Response

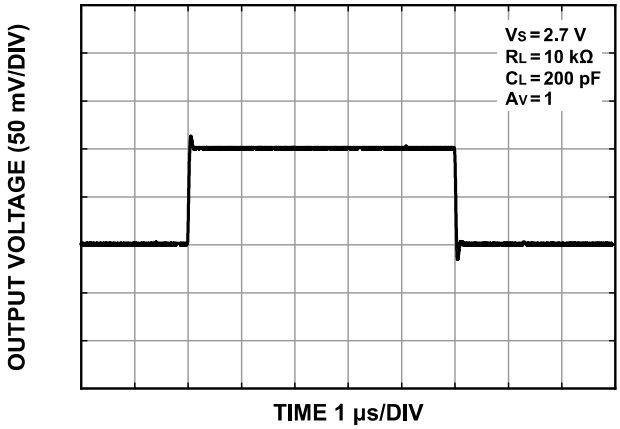



Figure 33. Small Signal Transient Response

# General Application Information

## Output Phase Reversal

Phase reversal is a change of polarity in the transfer function of the amplifier. This can occur when the voltage applied at the input of an amplifier exceeds the maximum common-mode voltage. Phase reversal can cause permanent damage to the device and may result in system lockups. The AD8615 , AD8656 , AD8618 and AD8616 do not exhibit phase reversal when input voltages are beyond the supplies.

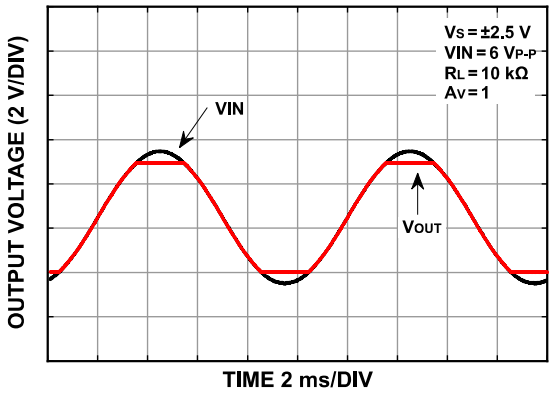



Figure 34. No Phase Reversal

## THD+Noise

AD86XX features low total harmonic distortion (THD) and excellent gain linearity, making these amplifiers a great choice for precision circuits with high closed-loop gain and for audio application circuits. Figure 35 demonstrates that when configured with positive unity gain (the worst case) and driving a 100 kΩ load, the total distortion and noise of AD86XX is approximately 0.0004%.

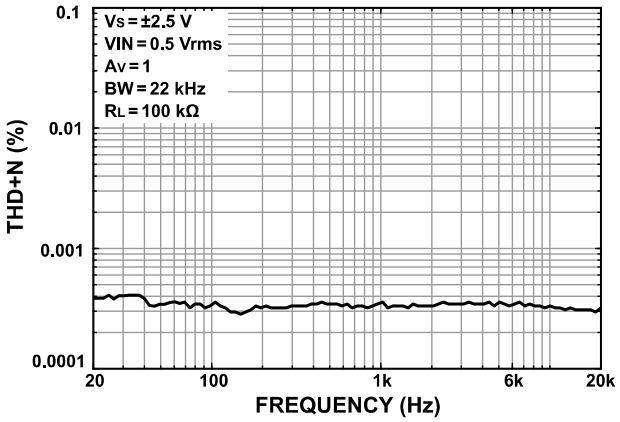



Figure 35. THD+N vs. Frequency

## Total Noise Including Source Resistors

The low input current noise and input bias current of the AD86XX make it the ideal amplifier for circuits with substantial input source resistance. Input offset voltage increases by less than 15 nV per 500 Ω of source resistance at room temperature. The total noise density of the circuit is

$$e_{nTOTAL} = \sqrt{e_n^2 + (i_n R_s)^2 + 4kTR_s}$$

## Outline Information

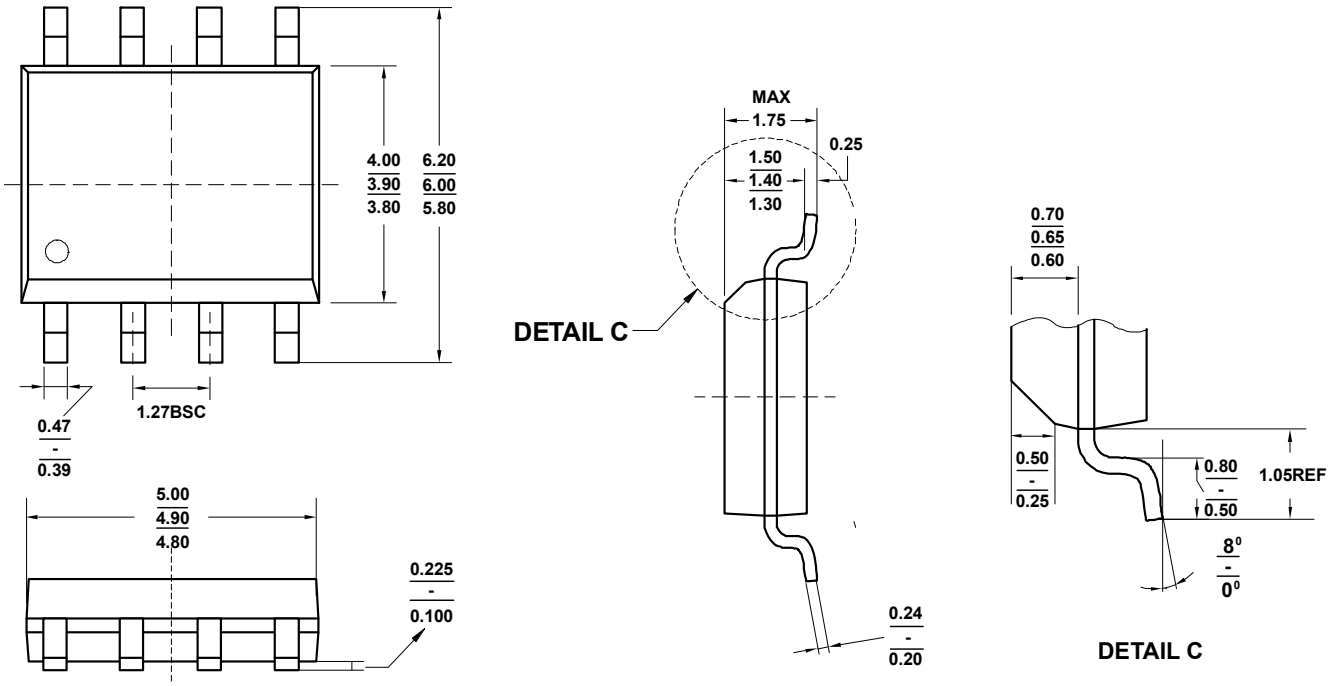



Figure 44. 8-Lead SOIC Package Dimensions shown in millimeters

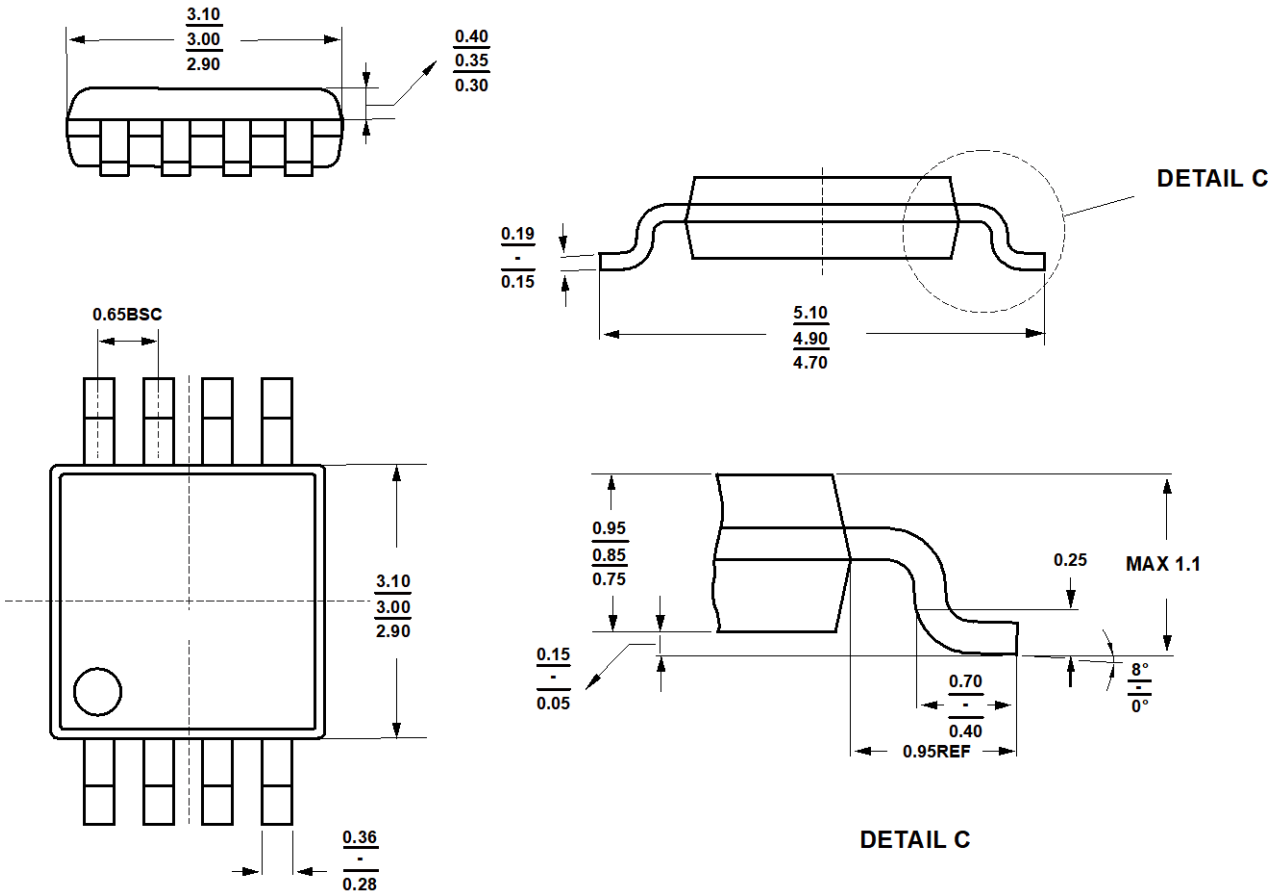



Figure 45. 8-Lead MSOP Package Dimensions shown in millimeters

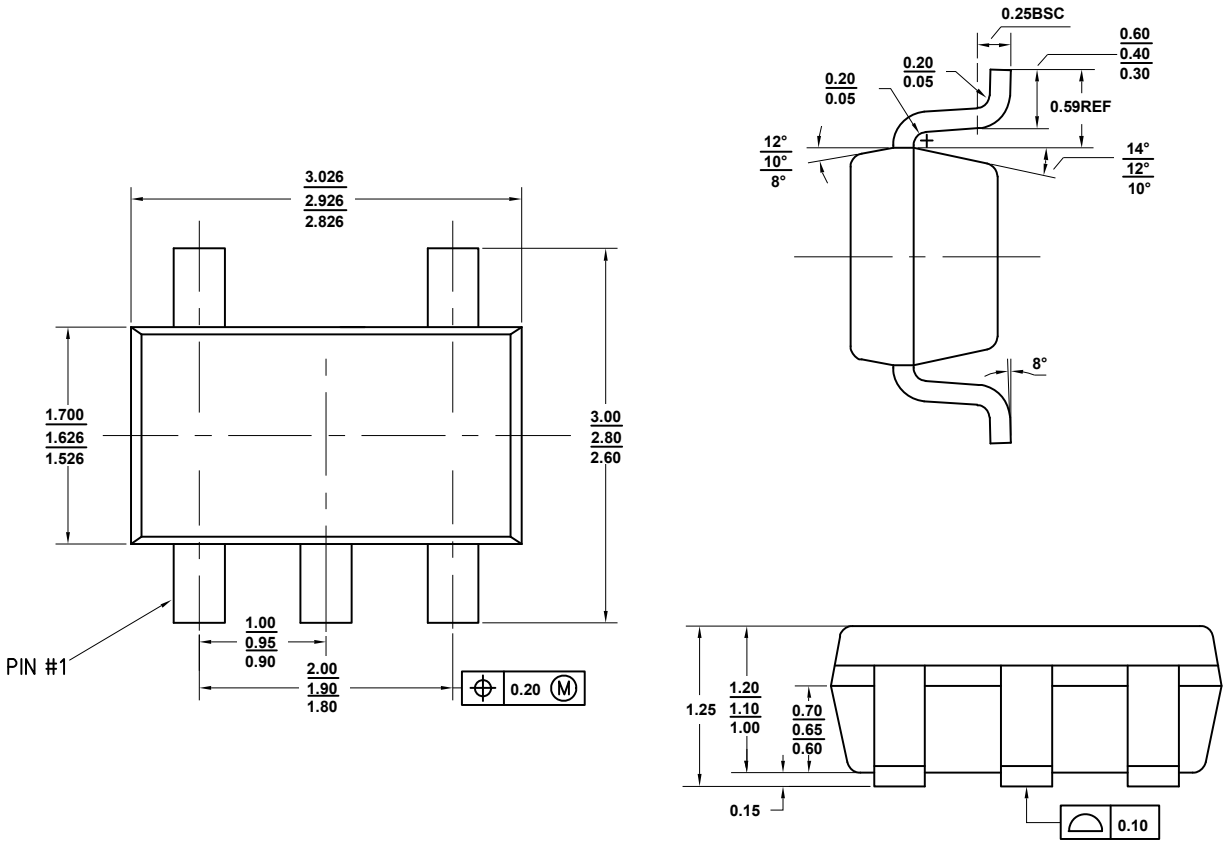



Figure 46. 5-Lead SOT23 Package Dimensions shown in millimeters

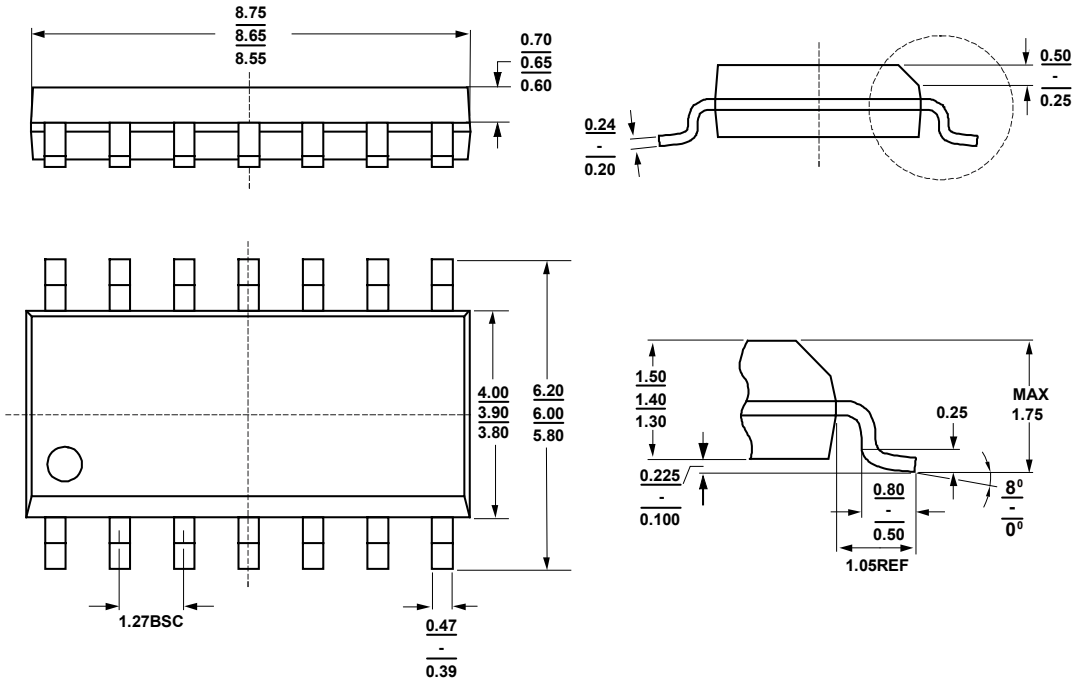



Figure 47. 14-Lead SOIC Package Dimensions shown in millimeters

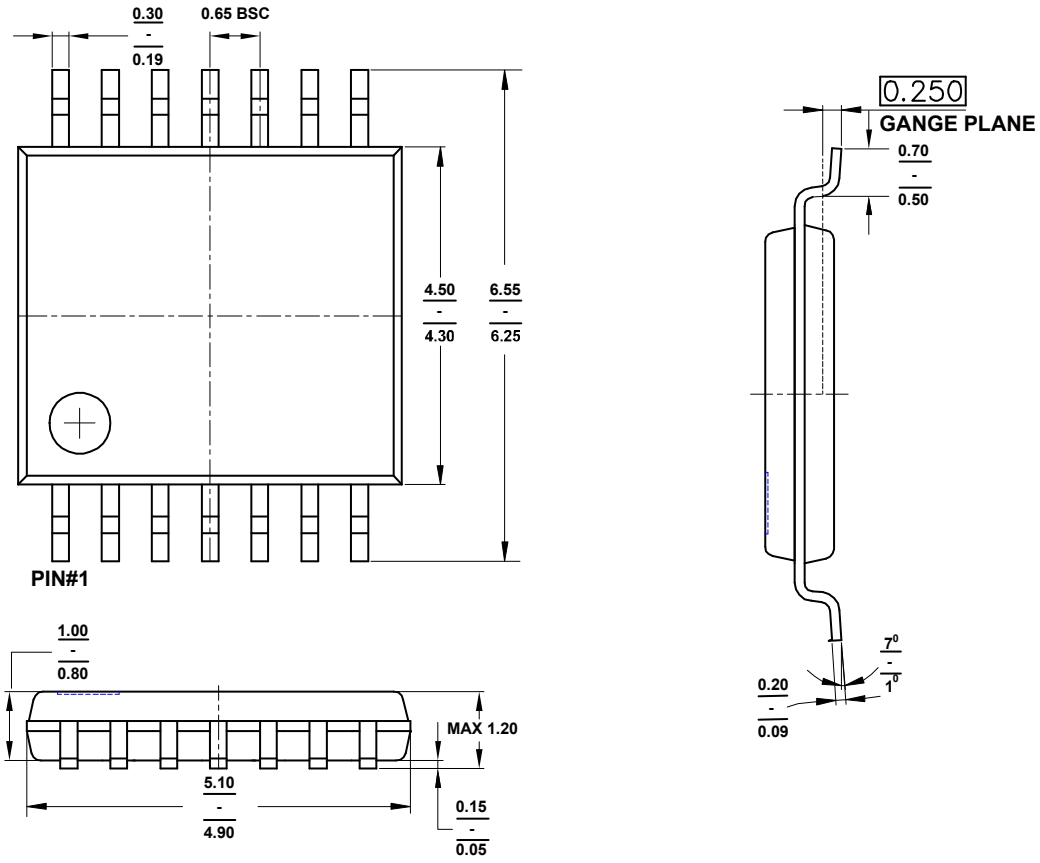



Figure 48. 14-Lead TSSOP Package Dimensions shown in millimeters

## Ordering Guide

| Model | Orderable Device | Status[1] | Channels | Package | Temperature Range (°C) | External Package |
|---|---|---|---|---|---|---|
| AD8615 | AD8615R | ACTIVE | 1 | SOT23-5 | -40 to +125 | 7” Reel |
| AD8656 | AD8656ARZ | ACTIVE | 2 | SOIC-8 | -40 to +125 | Tube |
| | AD8656ARZ-REEL7 | ACTIVE | | | | 13” Reel |
| | AD8656BRZ | ACTIVE | | MSOP-8 | | Tube |
| | AD8656BR | ACTIVE | | | | 13” Reel |
| AD8618 | AD8618CR | PREVIEW | 4 | SOIC-14 | -40 to +125 | Tube |
| | AD8618CRZ | PREVIEW | | | | 13” Reel |
| | AD8618CRB | PREVIEW | | TSSOP-14 | | Tube |
| | AD8618CS | PREVIEW | | | | 13” Reel |
| AD8616 | AD8616R | PREVIEW | 1 | SOT23-5 | -40 to +125 | 7” Reel |