Features

- Super Low Gate Charge
- Green Device Available
- Excellent Cdv/dt effect decline
- Advanced high cell density Trench technology

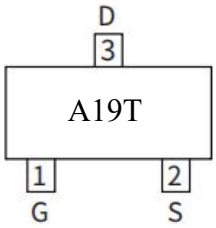
Bvdss	Rdson	ID
-30V	32mΩ	-4.5A

Application

- Battery protection
- Load Switch
- Uninterruptible power supply

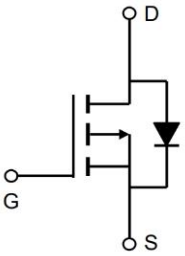
RoHS

Package



Marking and pin assignment

SOT23 top view



Schematic diagram

Package Marking and Ordering Information

Device Marking	Device	Device Package	Quantity
A19T	HL3401	SOT23	3000

Absolute Maximum Ratings (T_A=25℃unless otherwise specified)

Parameter	Symbol	Value	Unit
Drain-Source Voltage	V_{DSS}	-30	V
Gate-Source Voltage	V_{GS}	±16	V
Continuous Drain Current	I_D@T_A=25℃	-4.5	A
	I_D@T_A=70℃	-3.6	A
Pulsed Drain Current Tested[1]	I_{DM}@T_A=25℃	-16.8	A
Single Pulsed Avalanche Energy	EAS	-	mJ
Total Power Dissipation	P_D@T_A=25℃	1.2	W
	P_D@T_A=70℃	0.9	W
Storage Temperature Range	T_{STG}	-50 ~ 150	℃
Maximum Junction Temperature	T_J	150	℃

Thermal Resistance Ratings

Parameter	Symbol	Value	Unit
Thermal Resistance Junction-Ambient[2]	$R_{\theta JA}$	80	℃/W
Thermal Resistance Junction-Case	$R_{\theta JC}$	-	℃/W

Ordering Information

Ordering Number	Package	Pin Assignment			Packing
Halogen Free		G	S	D	
HL3401	SOT23	1	2	3	Tape Reel

Electrical Characteristics (T_J=25℃unless otherwise noted)

Parameter	Symbol	Test Conditions	Min	Typ	Max	Units
Drain-Source Breakdown Voltage	BV_{DSS}	V_{GS}=0V,I_D=-250μA	-30	-	-	V
Drain-Source Leakage Current	I_{DSS}	V_{DS}=-30V,V_{GS}=0V	-	-	-1	μA
		V_{DS}=-24V,V_{GS}=0V	-	-	-100	
Gate-Source Leakage Current	I_{GSS}	V_{DS}=0V,V_{GS} = ±16V	-	-	±100	nA
Gate-Threshold Voltage	$V_{GS(th)}$	V_{DS}=V_{GS},I_D=-250μA	-0.5	-0.9	-1.3	V
Static Drain-Source On-Resistance[2]	$R_{DS(on)}$	V_{GS}=-10V, I_D=-4A	-	32	42	mΩ
		V_{GS}=-4.5V, I_D=-3A	-	37	45	
		V_{GS}=-3.3V, I_D=-2A	-	46	60	
Input Capacitance	C_{iss}	V_{DS}= -15V, V_{GS}=0V, f=1MHz	-	942	-	pF
Output Capacitance	C_{oss}		-	62	-	
Reverse Transfer Capacitance	C_{rss}		-	57	-	
Total Gate Charge	Q_g	V_{DS}= -15V,V_{GS}= -5V,I_D= -4A	-	7.7	-	nC
Gate−Source Charge	Q_{gs}		-	1.5	-	
Gate−Drain("Miller")Charge	Q_{gd}		-	2.6	-	
Turn-on Delay Time	$t_{d(on)}$	V_{GS}= -10V,V_{DD}= -15V, R_G=3.3Ω,I_D= -2A	-	7	-	ns
Turn-on Rise Time	t_r		-	3.8	-	
Turn-off Delay Time	$t_{d(off)}$		-	35	-	
Turn-off Fall Time	t_f		-	10.5	-	
Source drain current(Body Diode)	I_{SD}	T_A=25℃	-	-	-4.5	A
Drain to Source Diode Forward Current	I_{SM}	-	-	-	-	A
Forward on voltage[2]	V_{SD}	T_J=25℃V_{GS}=0V, I_S= -2A	-	-	-1.2	V

Notes:

1. Pulse width limited by maximum allowable junction temperature
2. $R_{\theta JA}$ is measured with the device mounted on a 1inch^2 pad of 2oz copper FR4 PCB
3. Pulse Test: Pulse Width≤300μs, Duty Cycle≤0.5%.

Typical Performance Characteristics

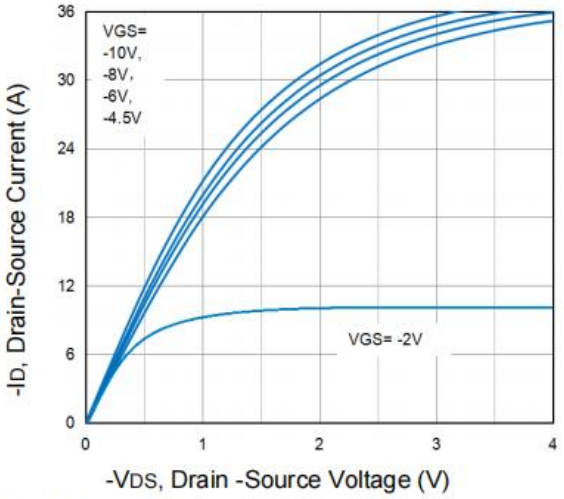


Fig1. Typical Output Characteristics

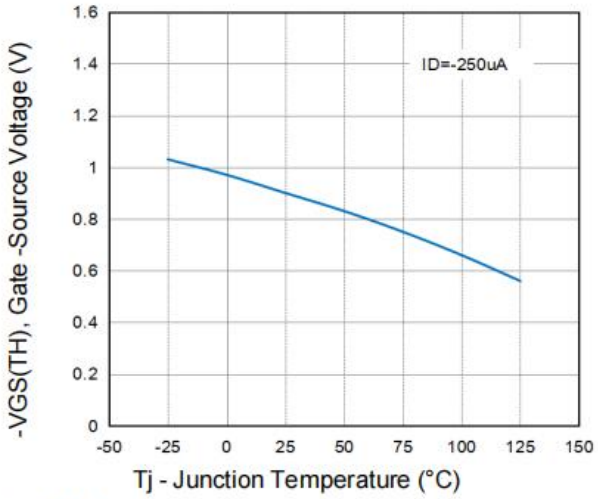


Fig2. Normalized Threshold Voltage Vs. Temperature

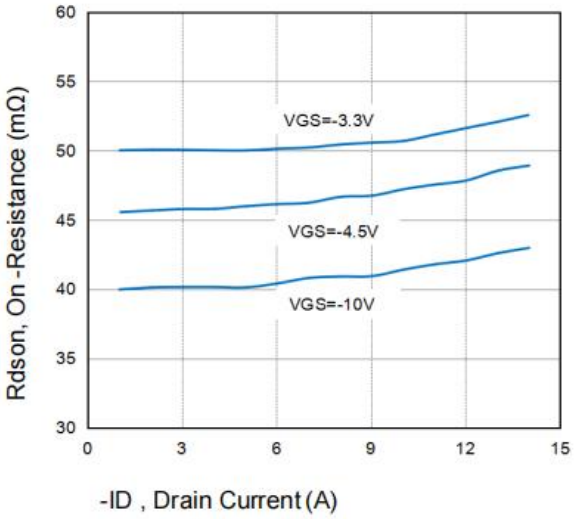


Fig3. On-Resistance vs. Drain Current and Gate Voltage

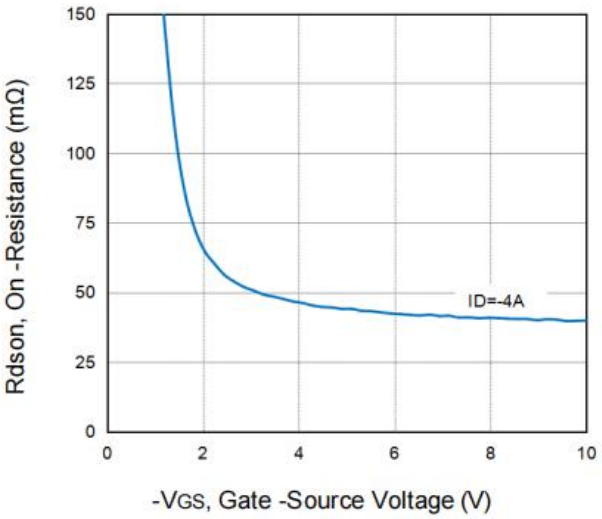


Fig4. On-Resistance vs.Gate Source Voltage

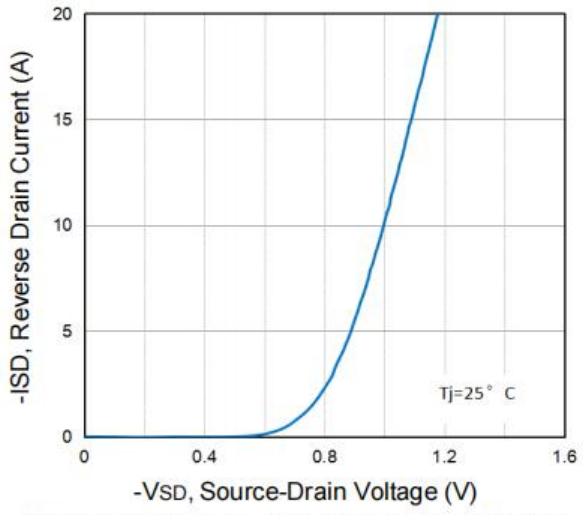


Fig5. Typical Source-Drain Diode Forward Voltage

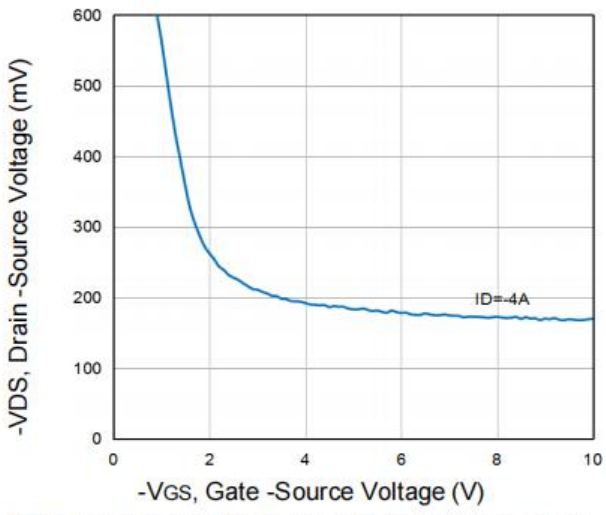


Fig6. Drain-Source Voltage vs Gate-Source Voltage

Typical Characteristics

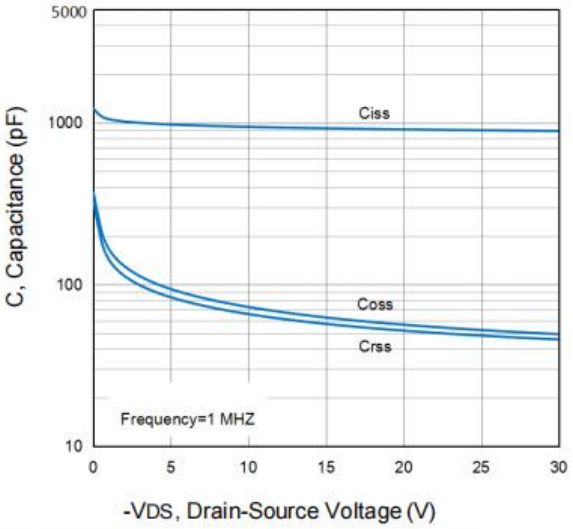


Fig7. Typical Capacitance Vs. Drain-Source Voltage

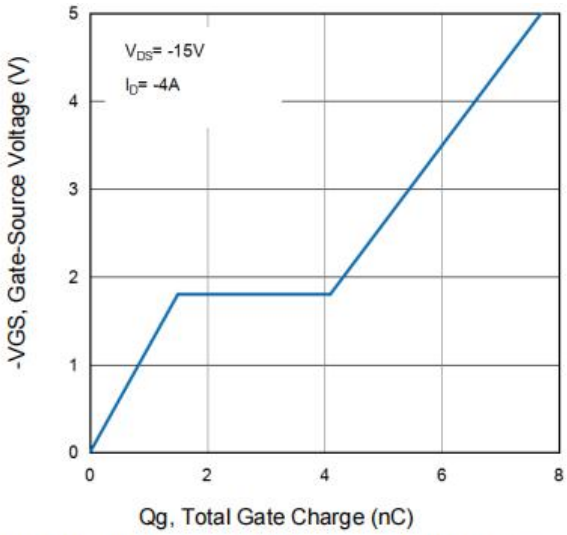


Fig8. Typical Gate Charge Vs. Gate-Source Voltage

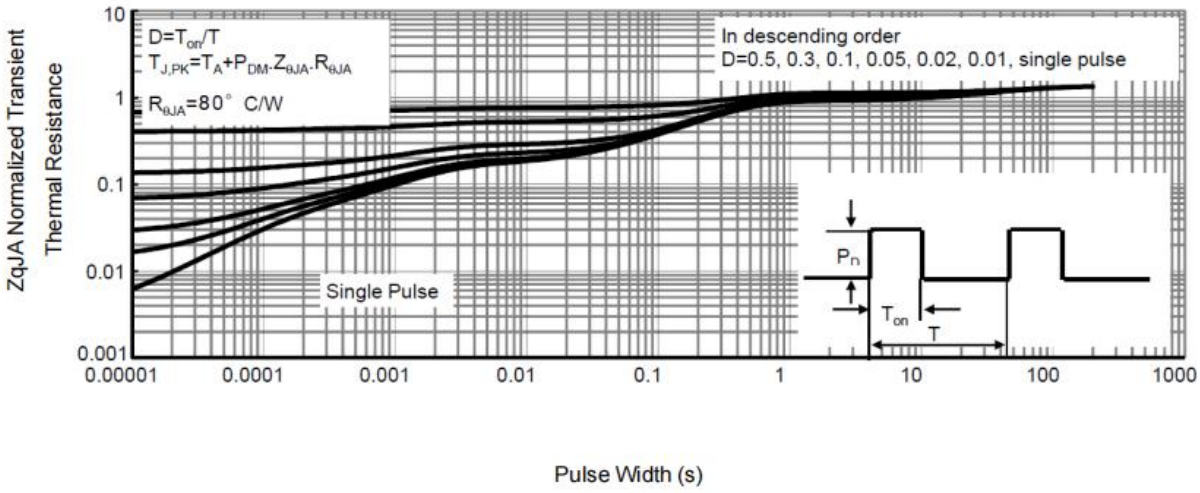


Fig9. Normalized Maximum Transient Thermal Impedance

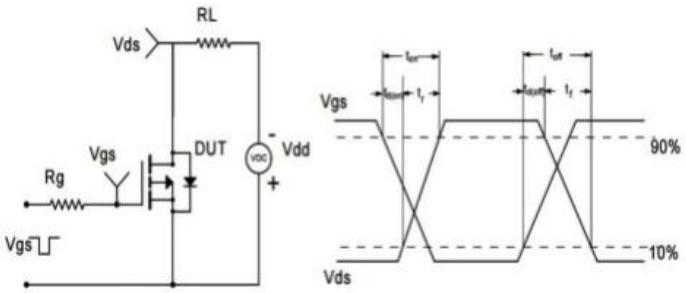
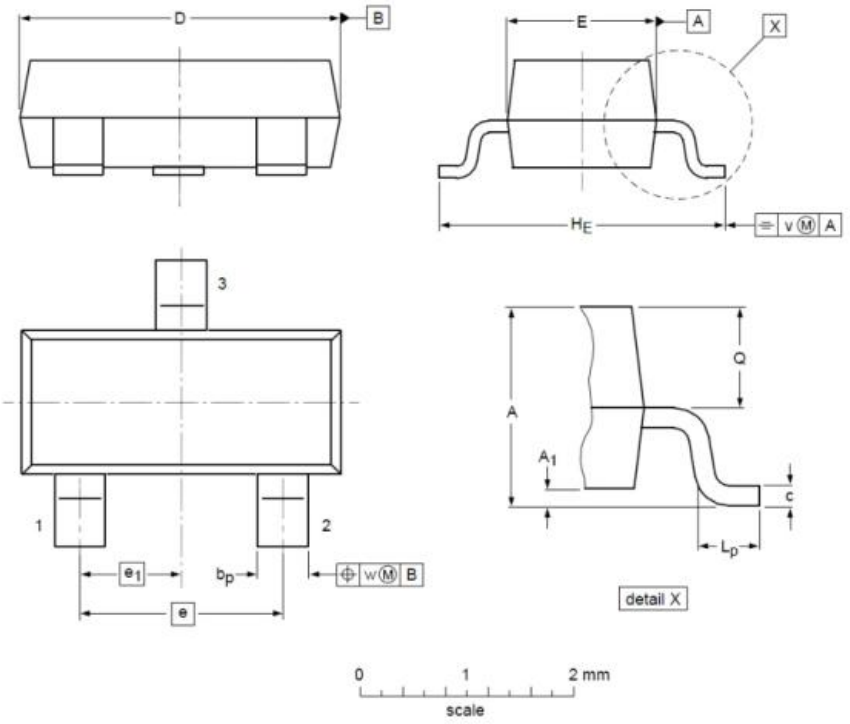


Fig10. Switching Time Test Circuit and waveforms

Package Dimensions SOT 23



DIMENSIONS (unit : mm)

Symbol	Min	Typ	Max	Symbol	Min	Typ	Max
A	0.90	1.01	1.15	**A_1**	0.01	0.05	0.10
b_p	0.30	0.42	0.50	**c**	0.08	0.13	0.15
D	2.80	2.92	3.00	**E**	1.20	1.33	1.40
e	--	1.90	–	**e_1**	–	0.95	--
H_E	2.25	2.40	2.55	**L_p**	0.30	0.42	0.50
Q	0.45	0.49	0.55	**v**	–	0.20	--
w	--	0.10	–				

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