1.General Description

The EMP2112 device is a synchronous step-down buck DC-DC converter optimized for high efficiency and compact solution size. The device integrates switches capable of delivering an output current up to 1.2A.

At medium to heavy loads, the device operates in pulse width modulation (PWM) mode with 1.5-MHz switching frequency. At light load, the device automatically enters PFM mode to maintain high efficiency over the entire load current range. In shutdown, the current consumption is reduced to less than 2 μA.

The EMP2112 provides an adjustable output voltage via an external resistor divider. An internal soft start circuit limits the inrush current during startup. Other features like over current protection, thermal shutdown protection and power good are built-in.

The device is available in a SOT23 package.

2.Features and Benefits

- 2.5V to 5.5V Input Voltage Range
- 35μA Operating Quiescent Current
- Internal Soft Startup
- Adjustable Output Voltage from 0.6 V to VIN
- 100% Duty Cycle for Lowest Dropout
- 1.5MHz Switching Frequency
- Integrated Low RDS(ON) Switches 200mΩ / 100mΩ
- Optimized PFM mode for battery applications to improve light load efficieny
- Power Good Output for EMP2112P
- Short circuit protection with Hiccup mode
- Thermal Shutdown Protection
- EMP2112 available in SOT23-5 package and EMP2112P available in SOT23-6 pakcage

3.Applications

- General Purpose POL Supply
- Mobile Phone, Mobile handsets
- Network Video Camera
- Set Top Box
- Wireless Router

4.Ordering information

Table 1 Ordering information

Type number	Topside marking	Package		
		Name	Description	Quantity
EMP2112GV	P16YW	SOT23-5	SOT23 package, 5 pins 2.92mm x 2.8mm; 1.25 mm (Max) height	3000
EMP2112PGV	P16PYW	SOT23-6	SOT23 package, 6pins 2.92mm x 2.8mm; 1.25 mm (Max) height	3000

5.Function diagram

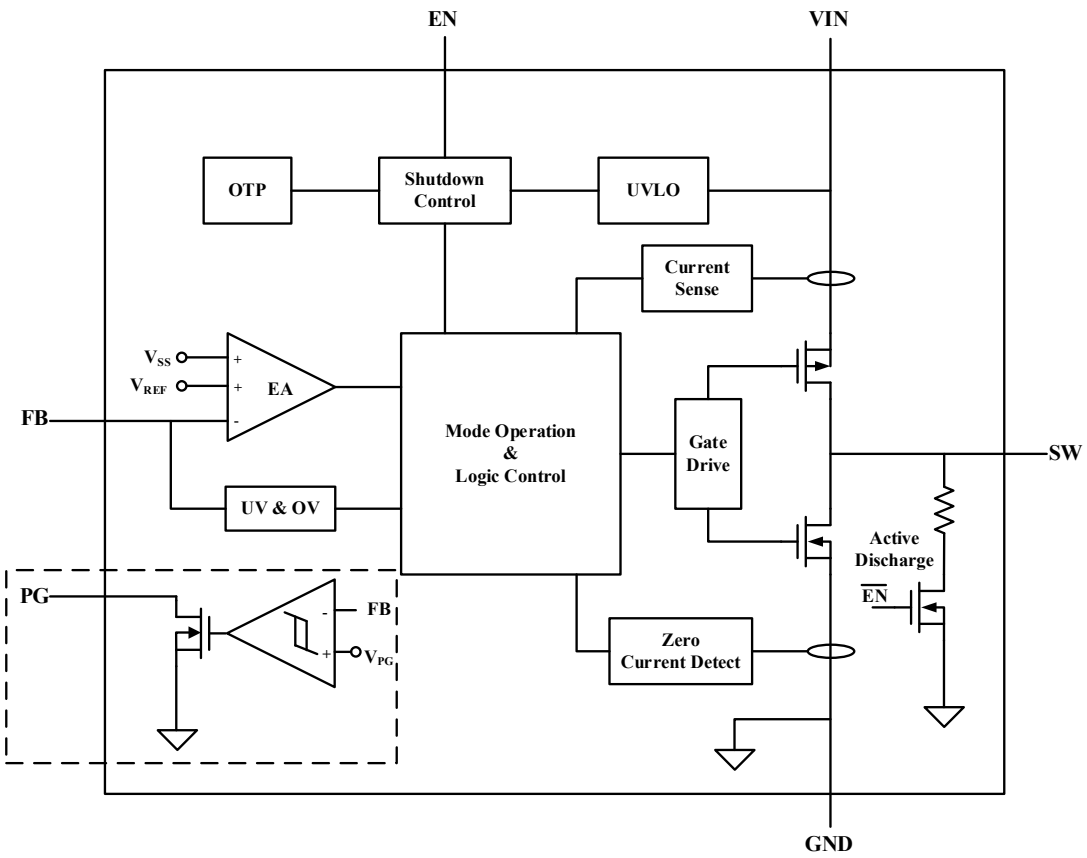


Fig 1. EMP2112(P) function diagram

6.Pinning information

6.1. Pin map

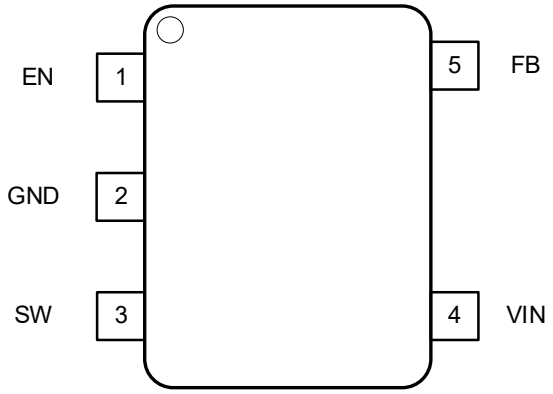


Fig 2. EMP2112 top view pin map

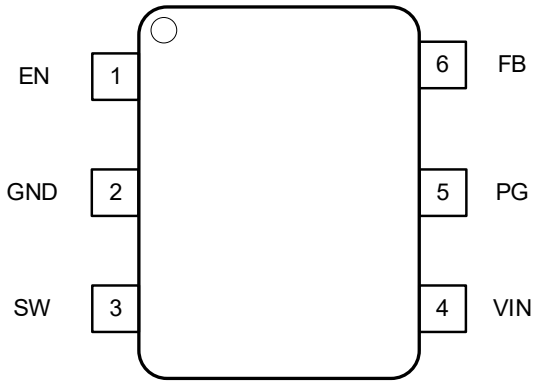


Fig 3. EMP2112P top view pin map

6.2. Pin description

Table 2 Pin description

Pin Name	EMP2112 Pin Number	EMP2112P Pin Number	Type	Description
EN	1	1	Input	Device enable logic input. Logic high enables the device, logic low disables the device and turns it into shutdown. Do not leave floating
GND	2	2	Power	Ground Pin
SW	3	3	Power	Switch pin connected to the internal FET switches and inductor terminal.Connect the inductor of the output filter to this pin
VIN	4	4	Power	Power supply voltage input
PG	-	5	Output	Power good open drain output pin for EMP2112P. The pull-up resistor shouldnot be connected to any voltage higher than 5.5V. If it's not used, leave the pin floating.
FB	5	6	Input	Feedback pin for the internal control loop. Connect this pin to an externalfeedback divider.

7.Functional description

The EMP2112 is a high-efficiency synchronous step-down converter. The device operates with an adaptive offtime with peak current control scheme. The device operates at typically 1.5MHz frequency pulse width modulation (PWM) at moderate to heavy load currents. Based on the VIN/VOUT ratio, a simple circuit sets the required off time for the low-side MOSFET. It makes the switching frequency relatively constant regardless of the variation of input voltage, output voltage, and load current.

7.1. PWM and PFM Mode

The device integrates PWM/PFM hybrid control modes to improve the efficiency at light load. When the output current is in heavy load, the device operates in PWM mode. When the output current is in light load, the device enters PFM mode to improve the efficiency and reduce power loss.

7.2. 100% Duty Cycle Low Dropout Operation

The device offers a low input-to-output voltage differential by entering 100% duty cycle mode. In this mode, the high-side MOSFET switch is constantly turned on and the low-side MOSFET is switched off. The minimum input voltage to maintain output regulation, depending on the load current and output voltage.

7.3. Soft Start

During power up of the device, internal soft startup circuitry ramps up the output voltage which reaches nominal output voltage during a startup time. This avoids excessive inrush current and creates a smooth output voltage rise slope.

7.4. Under Voltage Lockout

To avoid mis-operation of the device at low input voltages, under voltage lockout is implemented that shuts down the device at voltages lower than VUVLO with VHYS_UVLO hysteresis.

7.5. Thermal Shutdown

The device enters thermal shutdown once the junction temperature exceeds the thermal shutdown rising threshold, TJSD. Once the junction temperature falls below the falling threshold, the device returns to normal operation automatically.

7.6. Power Good

The EMP2112P has a power good output. The PG pin goes high impedance once the output is above 90% ofthe nominal voltage, and is driven low once the output voltage falls below typically 90% of the nominal voltage. The PG pin is an open-drain output and is specified to sink up to 2 mA. The power good output requires a pull-up resistor connecting to any voltage rail less than 5.5 V. The PG signal can be used for sequencing of multiple rails by connecting it to the EN pin of other converters. Leave the PG pin unconnected when not used.

7.7. Over Current Protection

The over current protection circuit prevents the device from high inductor current and drawing excessive current from a battery or input voltage rail. Excessive current might occur with a heavy load or shorted output circuit condition. The EMP2112 adopts the peak current control by sensing the current of the high-side switch. Once the high-side switch current limit is reached, the high-side switch is turned off and low-side switch is turned on to ramp down the inductor current with an adaptive off-time.

8. Application Diagram

The following diagram and section discusse the design of the external components to complete the power supply design for a typical applications as a reference.

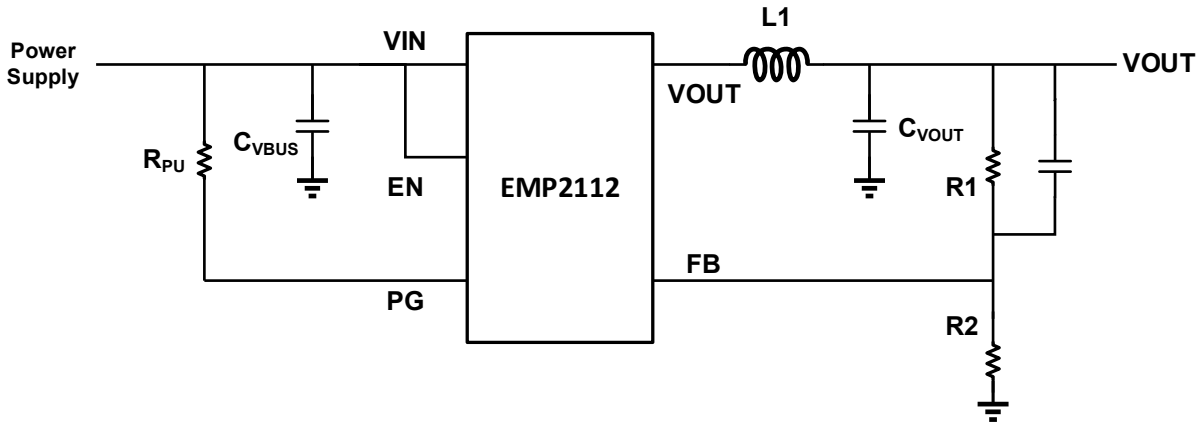


Fig 4. EMP2112 Application Diagram

8.1. Setting the Output Voltage

The output voltage is set by an external resistor divider according to Equation 1:

$$V_{OUT} = V_{FB} \times \left(1 + \frac{R_1}{R_2}\right) = 0.6V \times \left(1 + \frac{R_1}{R_2}\right) \quad (1)$$

There is no strict requirement for the feedback resistor. An R_1 value greater than 10kΩ is reasonable for most applications. R_2 must not be higher than 100kΩ to achieve high efficiency at light load while providing acceptable noise sensitivity.

8.2. Selecting the Inductor

Most applications work best with a 1-2.2µH inductor. Select an inductor with a DC resistance less than 50mΩ to optimize efficiency. A high-frequency, switch-mode power supply with a magnetic device produces a strong electronic magmetic inference in the system. Any shield inductor is ideal for applications as they can decrease the influence effectively. For most designs, estimate the inductance value with Equation 2:

$$L = \frac{V_{OUT} \times (V_{IN} - V_{OUT})}{V_{IN} \times \Delta I_L \times f_S} \quad (2)$$

Where:

- ΔI_L is the inductor current ripple
- f_S is the switching frequency
- L is the inductor value

Choose an inductor current that is approximately 30% of the maximum load current. The maximum inductor peak current can be calculated with Equation 3:

$$I_{PEAK} = I_{LOAD} + \frac{\Delta I_L}{2} \quad (3)$$

Where:

- I_{PEAK} is the maximum inductor peak current

8.3. Selecting the Input Capacitor

A typical X5R or better grade ceramic capacitor with 6.3V rating and no less than 10µF capacitance is recommended. To minimize the potential noise problem, we place this ceramic capacitor really close to the VIN and GND pins. Care should be taken to minimize the loop area formed by input capacitor, VIN and GND pins.

When using ceramic capacitors, ensure that they have enough capacitance to provide a sufficient charge to prevent an excessive voltage ripple at the input. The input voltage ripple caused by the capacitance can be estimated with Equation 4:

$$\Delta V_{IN} = \frac{I_{LOAD}}{f_S \times C_{IN}} \times \frac{V_{OUT}}{V_{IN}} \times \left(1 - \frac{V_{OUT}}{V_{IN}}\right) \quad (4)$$

Where:

- ΔV_{IN} is the input voltage ripple
- C_{IN} is the input vapacitor

8.4. Selecting the Output Capacitor

The output capacitor is selected to handle the output ripple noise requirements. Both steady state ripple and transient requirements must be taken into consideration when selecting this capacitor. Estimate the output voltage ripple with Equation:

$$\Delta V_{OUT} = \frac{V_{OUT}}{f_S \times L} \times \left(1 - \frac{V_{OUT}}{V_{IN}}\right) \times \left(R_{ESR} + \frac{1}{8 \times f_S \times C_{OUT}}\right) \quad (5)$$

Where:

- ΔV_{OUT} is the output voltage ripple
- C_{OUT} is the output vapacitor
- R_{ESR} is the equivalent series resistance value of the output vapacitor

For the best performance, it is recommended to use X5R or better grade ceramic capacitor with 6.3V rating and no less than 10μF capacitance.

8.5. PCB Layout Guidelines

Efficient layout of the switching power supplies is critical for stable operation. For best results, follow the guidelines below.

- Place the high-current paths (GND, VIN and SW) very close to the device with short, direct and wide traces.
- Place the input capacitor as close as possible to the IC.
- Place the external feedback resistors next to FB.
- Keep the switching node SW short and away from the feedback network.
- Keep the VOUT sense line as short as possible and away from the power inductor.

9.Absolute Maximum Ratings

Stresses exceeding the absolute maximum ratings may damage the device. The device may not function or be operable above the recommended operating conditions and stressing the parts to these levels is not recommended. In addition, extended exposure to stresses above the recommended operating conditions may affect device reliability. The absolute maximum ratings are stress ratings only.

Table 3 Absolute Maximum Ratings

In accordance with the Absolute Maximum Rating System (IEC 60134)

Symbol	Parameter	Conditions	Min	Max	Unit
V_{IN}[1]	Input voltage		-0.3	6.5	V
V_{SW}[1]	SW voltage		-0.3	6.5	V
V_{EN}, V_{FB}, V_{PG}[1]	EN, FB, PG pin voltage		-0.3	6.5	V
T_{stg}	Storage temperature		-55	150	°C
θ_{JA}	Thermal Resistance	Junction-to-Ambient		170	°C/W
θ_{JC}	Thermal Resistance	Junction-to-case (top)		130	°C/W
ESD	HBM	ANSI/ESDA/JEDEC JS-001 Class 2		2	kV
	CDM	ANSI/ESDA/JEDEC JS-002		1	kV

[1] All voltage values, except differential voltages, are with respect to network ground terminal.

10. Recommended Operating Conditions

The Recommended Operating Conditions table defines the conditions for actual device operation. Recommended operating conditions are specified to ensure optimal performance to the datasheet specifications. EnergyMath does not recommend exceeding them or designing to Absolute Maximum Ratings.

Table 4 Recommended Operating Conditions

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{IN}	Input voltage		2.5		5.5	V
V_{OUT}	Output voltage		0.6		V_{IN}	V
T_{amb}	Ambient Operating temperature		-40		+85	°C

11. Electrical Characteristics

T_{amb} = -40°C to 85°C unless otherwise indicated. V_{IN}=5V, V_{OUT}=2.5V, L=2.2uH, C_{OUT}=10uF,T_{amb} = 25°C unless otherwise indicated. All typical values at T_{amp} = 25°C.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{IN}	Input voltage range		2.5	5	5.5	V
V_{UVLO}	Input UVLO threshold	V_{IN} rising		2.3	2.45	V
	UVLO hysteresis			180		mV
I_Q	Quiescent current	I_{OUT}=0V, V_{FB}=V_{REF}*105%		35	65	μA
I_{SHDN}	Shutdown current	V_{EN}=0V		0.1	10	μA
V_{REF}	Feedback reference voltage		0.588	0.600	0.612	V
$R_{DS(ON)}$	High-side FET on resistance			200		mΩ
	Low-side FET on resistance			100		mΩ
I_{LIM}	High-side FET current limit		1.8			A
I_{DIS}	SW discharge current	V_{EN}=0V		160		mA
V_{IH}	High-level threshold at EN pin		1.5			V
V_{IL}	Low-level threshold at EN pin				0.4	V
$I_{EN,LKG}$	Input leakage current into EN pin			0.01	2.0	μA
V_{PG_TH}	Power good threshold	PG low, FB falling (EMP2112P)		90		%
		PG high, FB rising (EMP2112P)		90		%
I_{SINK_PG}	Sink current at PG pin	EMP2112P			2	mA
Thermal Protection						
T_{THMP}	Thermal shutdown threshold	Junction temperature rising		165		°C
T_{THMP_HYS}	Thermal shutdown hysteresis			25		°C
Timing specifications						
F_{OSC}	Oscillator frequency	I_{OUT}=0.5A		1.5		MHz
		V_{OUT}=0V		400		kHz
t_{ON_MIN}	Minimum ON time			60		ns
D_{MAX}	Maximum duty cycle		100			%
t_{SS}	Soft start time			500		μs

11.1. Testing waveforms

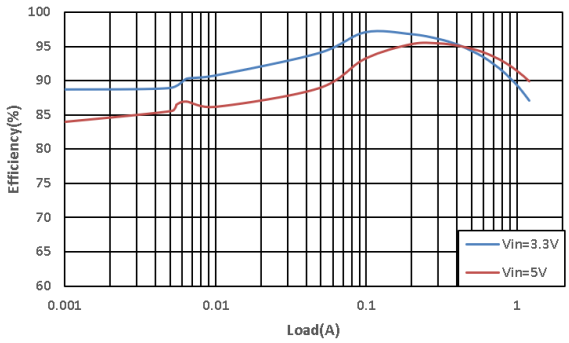


Fig 5. 2.5-V Output Efficiency

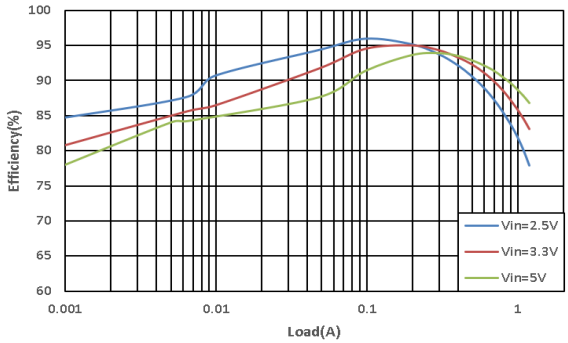
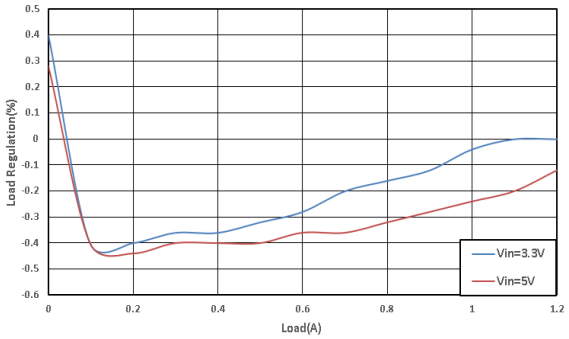
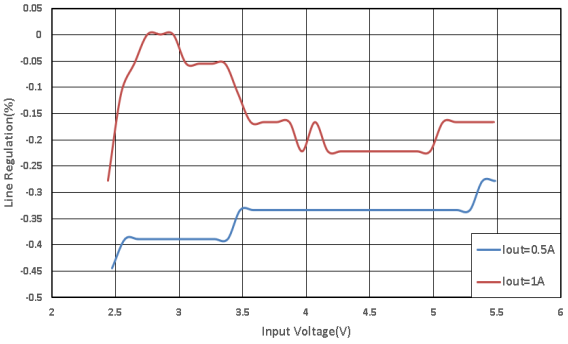


Fig 6. 1.8-V Output Efficiency



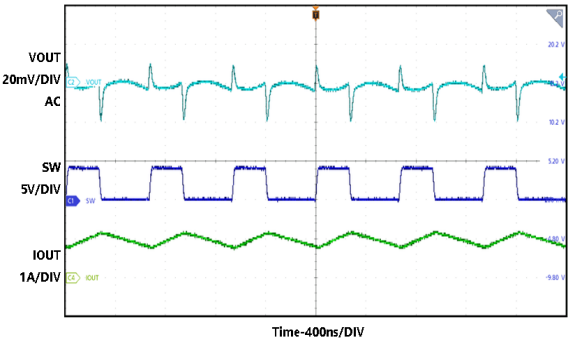
V_{OUT}=2.5V

Fig 7. Load Regulation



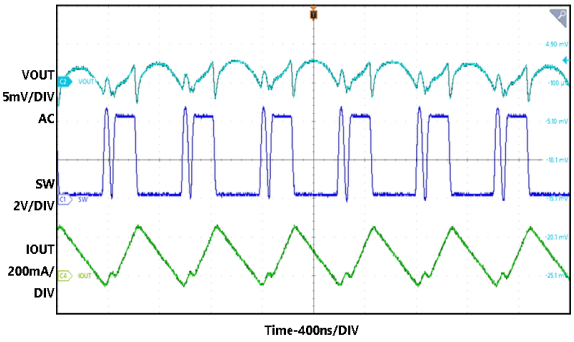
V_{OUT}=2.5V

Fig 8. Line Regulation



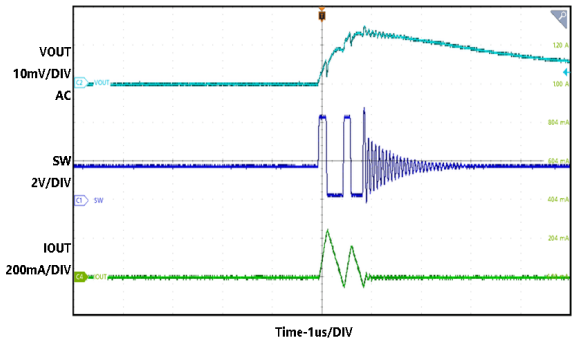
V_{IN}=5V, V_{OUT}=1.8V

Fig 9. 1-A Output Ripple



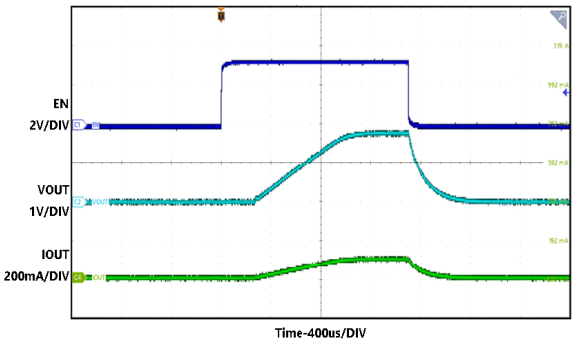
V_{IN}=5V, V_{OUT}=1.8V

Fig 10. 0.1-A Output Ripple



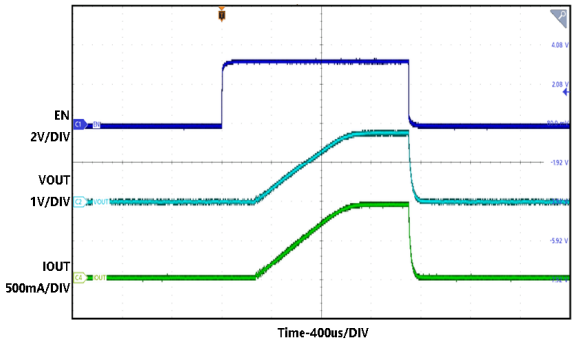
V_{IN}=5V, V_{OUT}=1.8V

Fig 11. 0-A Output Ripple



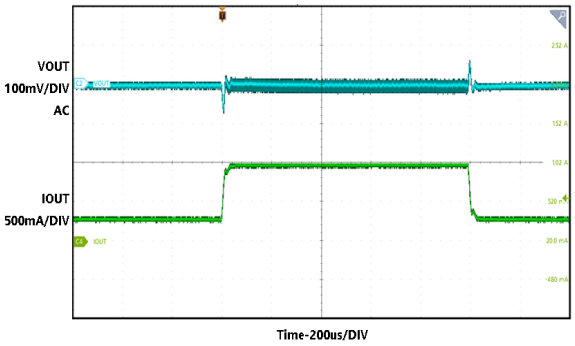
I_{OUT}=0.1A

Fig 12. Startup with Load



I_{OUT}=1A

Fig 13. Startup with Load

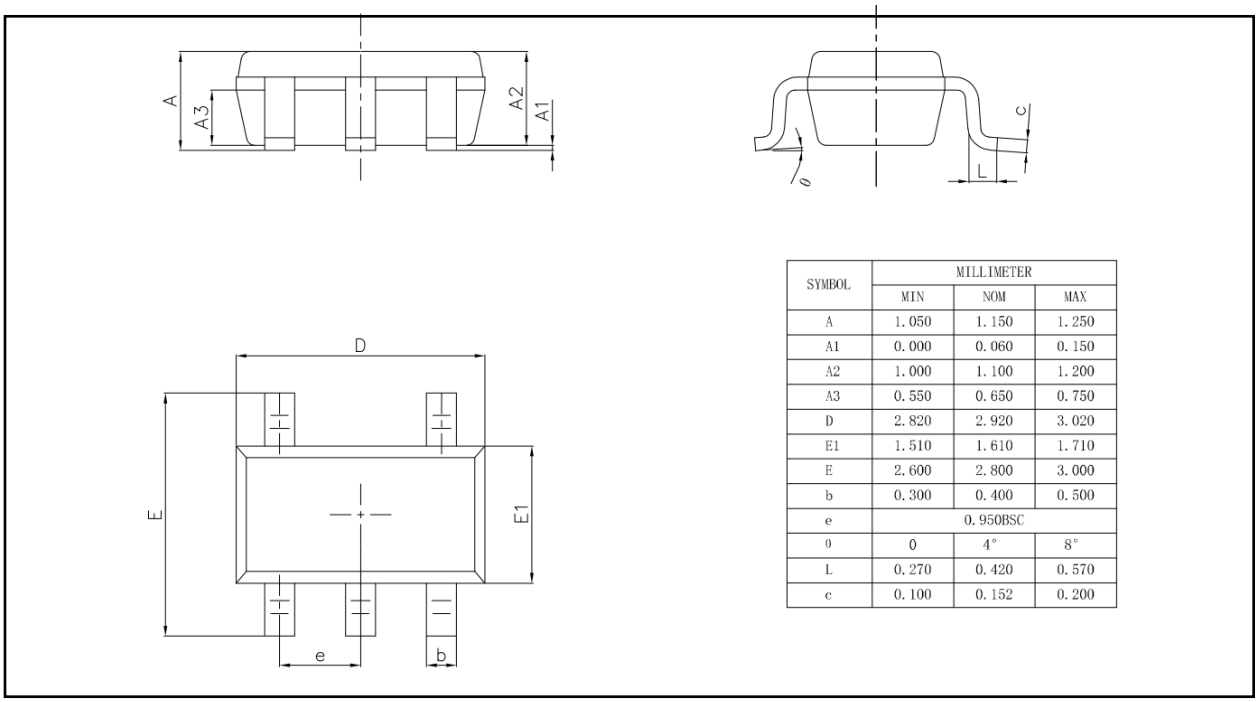


Load Step 0.3A to 1A, 1A/µs slew rate

Fig 14. Load Transient

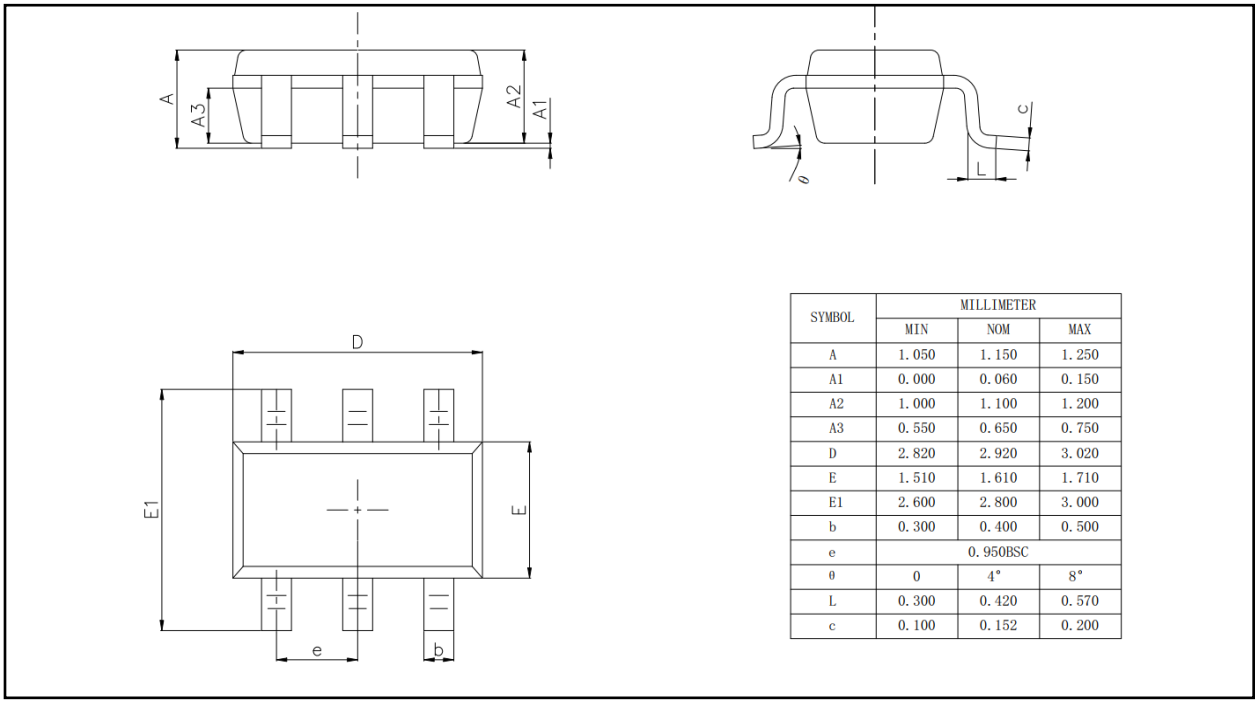
12. Package outline

SOT23-5



SYMBOL	MILLIMETER		
	MIN	NOM	MAX
A	1.050	1.150	1.250
A1	0.000	0.060	0.150
A2	1.000	1.100	1.200
A3	0.550	0.650	0.750
D	2.820	2.920	3.020
E1	1.510	1.610	1.710
E	2.600	2.800	3.000
b	0.300	0.400	0.500
e	0.950BSC		
θ	0	4°	8°
L	0.270	0.420	0.570
c	0.100	0.152	0.200

SOT23-6



SYMBOL	MILLIMETER		
	MIN	NOM	MAX
A	1.050	1.150	1.250
A1	0.000	0.060	0.150
A2	1.000	1.100	1.200
A3	0.550	0.650	0.750
D	2.820	2.920	3.020
E	1.510	1.610	1.710
E1	2.600	2.800	3.000
b	0.300	0.400	0.500
e	0.950BSC		
θ	0	4°	8°
L	0.300	0.420	0.570
c	0.100	0.152	0.200

13. Abbreviations

Table 5 Abbreviations

Acronym	Description
CDM	Charged Device Model
HBM	Human Body Model

14. Revision history

Table 6 Revision history

Document ID	Release Date	Data sheet status	Change notice	Supersedes
EMP2112 Rev1.1	Nov 08, 2023	Product datasheet		EMP2112 Rev1.0
Modifications:	• Change the topside marking.			
EMP2112 Rev1.0	Dec 08, 2022	Product datasheet		