

NST5P3N40 N and P-Channel Power MOSFET

1 Features and Benefits

- Low $R_{DS(ON)}$ to minimize conductive loss
- Low Gate Charge for fast switching
- Low Thermal resistance
- 100% Avalanche tested
- 100% DVDS tested
- N-Channel

$$V_{DS} = 40V, I_D = 5A$$

$$R_{DS(ON)} = 33m\Omega @ V_{GS} = 10V(Typ)$$

$$R_{DS(ON)} = 52m\Omega @ V_{GS} = 4.5V(Typ)$$

- P-Channel

$$V_{DS} = -40V, I_D = -3A$$

$$R_{DS(ON)} = 65 m\Omega @ V_{GS} = -10V(Typ)$$

$$R_{DS(ON)} = 85 m\Omega @ V_{GS} = -4.5V(Typ)$$

2 Application

- Electronic Ballast
- Electronic Transformer
- Switch Mode Power Supply

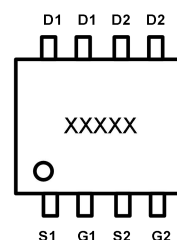
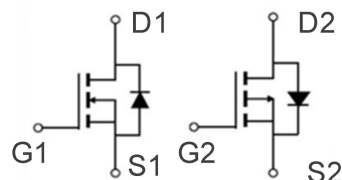
3 Description

The NST5P3N40 with a low resistance package to provide extremely low $R_{DS(ON)}$. This device is ideal for load switch and battery protection applications. The complementary MOSFETs may be used to form a level shifted high side switch, and for a host of other applications.

Device information

Part Number	Package	Body size
NST5P3N40	SOP8	4.9mm*3.9mm


SOP8 Pin Configuration



4 Selection Guide

Part Number	TYPE	$R_{DS_N(ON)}$	$R_{DS_P(ON)}$	VDS	VTH_N	VTH_P
NST5P3N40	P + N	33m Ω	65m Ω	40V	1.5V	-1.8V

5 Ordering Guide

Part Number	LOGO	Package	Package	SPQ
NST5P3N40	 NST5P3N40 XXXXXX	SOP8	Tape & Reel	4000

6 Revision history

Version	Content	Time
V1.0	Create	2024.02.13



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7 Function Pin Description

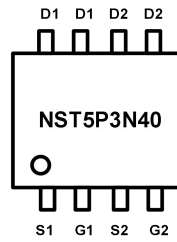


Figure7-1 8-Pin SOP8 Top view

Table7-1 Lead Definitions

Number	Symbol	Description
1	S1	SOURCE1
2	G1	GATE1
3	S2	SOURCE2
4	G2	GATE2
5	D2	DRAIN2
6	D2	DRAIN2
7	D1	DRAIN1
8	D1	DRAIN1

8 Product specifications

8.1 Absolute Maximum Ratings

Parameter	Symbol	Limit		Unit
		N-Ch	P-ch	
Drain-Source Voltage	V_{DS}	40	-40	V
Gate-Source Voltage	V_{GS}	± 20	± 20	V
Drain Current-Continuous	I_D	5	-3	A
Drain Current-Pulsed (Note 1)	I_{DM}	24	-16	A
Single pulse avalanche energy (Note 5)	EAS	15	20	mJ
Maximum Power Dissipation	P_D	2	2	W
Operating Junction and Storage Temperature Range	T_J, T_{STG}	-55 To 150	-55 To 150	$^{\circ}C$

Thermal Characteristic

Thermal Resistance, Junction-to-Ambient (Note2)	$R_{\theta JA}$	N-Ch	62.5	$^{\circ}C/W$
Thermal Resistance, Junction-to-Ambient (Note2)	$R_{\theta JA}$	P-Ch	62.5	$^{\circ}C/W$

8.2 Electrical Characteristics (TA=25 $^{\circ}C$ unless otherwise noted)

N-CH Electrical Characteristics (TA=25 $^{\circ}C$ unless otherwise noted)

Parameter	Symbol	Condition	Min	Typ	Max	Unit
Off Characteristics						
Drain-Source Breakdown Voltage	BV_{DSS}	$V_{GS}=0V, I_D=250\mu A$	40	-	-	V
Zero Gate Voltage Drain Current	I_{DSS}	$V_{DS}=40V, V_{GS}=0V$	-	-	1	μA
Gate-Body Leakage Current	I_{GSS}	$V_{GS}=\pm 20V, V_{DS}=0V$	-	-	± 100	nA
On Characteristics (Note 3)						
Gate Threshold Voltage	$V_{GS(th)}$	$V_{DS}=V_{GS}, I_D=250\mu A$	1.0	1.5	2.0	V
Drain-Source On-State Resistance	$R_{DS(on)}$	$V_{GS}=10V, I_D=5A$	-	33	40	m Ω
		$V_{GS}=4.5V, I_D=3A$	-	52	68	m Ω
Forward Transconductance	g_{FS}	$V_{DS}=5V, I_D=3A$	-	6	-	S
Dynamic Characteristics (Note4)						
Input Capacitance	C_{iss}	$V_{DS}=20V, V_{GS}=0V, F=1.0MHz$	-	265	-	PF
Output Capacitance	C_{oss}		-	35	-	PF
Reverse Transfer Capacitance	C_{rss}		-	32	-	PF
Switching Characteristics (Note 4)						
Turn-on Delay Time	$t_{d(on)}$	$V_{DD}=20V, I_D=3A, V_{GS}=10V, R_{GEN}=1\Omega$	-	5	-	nS
Turn-on Rise Time	t_r		-	10	-	nS
Turn-Off Delay Time	$t_{d(off)}$		-	12	-	nS
Turn-Off Fall Time	t_f		-	8	-	nS
Total Gate Charge	Q_g	$V_{DS}=20V, I_D=3A, V_{GS}=10V$	-	10.2	-	nC
Gate-Source Charge	Q_{gs}		-	1.7	-	nC
Gate-Drain Charge	Q_{gd}		-	2.1	-	nC
Drain-Source Diode Characteristics						
Diode Forward Voltage (Note 3)	V_{SD}	$V_{GS}=0V, I_S=3A$	-	-	1.2	V

P-CH Electrical Characteristics (TA=25°C unless otherwise noted)

Parameter	Symbol	Condition	Min	Typ	Max	Unit
Off Characteristics						
Drain-Source Breakdown Voltage	BV_{DSS}	$V_{GS}=0V, I_D=-250\mu A$	-40	-	-	V
Zero Gate Voltage Drain Current	I_{DSS}	$V_{DS}=-40V, V_{GS}=0V$	-	-	-1	μA
Gate-Body Leakage Current	I_{GSS}	$V_{GS}=\pm 20V, V_{DS}=0V$	-	-	± 100	nA
On Characteristics (Note 3)						
Gate Threshold Voltage	$V_{GS(th)}$	$V_{DS}=V_{GS}, I_D=-250\mu A$	-1.2	-1.8	-2.5	V
Drain-Source On-State Resistance	$R_{DS(on)}$	$V_{GS}=-10V, I_D=-3A$	-	65	80	m Ω
		$V_{GS}=-4.5V, I_D=-2A$	-	85	130	m Ω
Forward Transconductance	g_{FS}	$V_{DS}=-5V, I_D=-3A$	-	8	-	S
Dynamic Characteristics (Note 4)						
Input Capacitance	C_{iss}	$V_{DS}=-20V, V_{GS}=0V,$ $F=1.0MHz$	-	485	-	pF
Output Capacitance	C_{oss}		-	97	-	pF
Reverse Transfer Capacitance	C_{riss}		-	70	-	pF
Switching Characteristics (Note 4)						
Turn-on Delay Time	$t_{d(on)}$	$V_{DD}=-20V, R_L=5\Omega$ $V_{GS}=-10V, R_{GEN}=3\Omega$	-	9	-	nS
Turn-on Rise Time	t_r		-	8	-	nS
Turn-Off Delay Time	$t_{d(off)}$		-	44	-	nS
Turn-Off Fall Time	t_f		-	41	-	nS
Total Gate Charge	Q_g	$V_{DS}=-20V, I_D=-3A$ $V_{GS}=-10V$	-	12	-	nC
Gate-Source Charge	Q_{gs}		-	2.1	-	nC
Gate-Drain Charge	Q_{gd}		-	2.4	-	nC
Drain-Source Diode Characteristics						
Diode Forward Voltage (Note 3)	V_{SD}	$V_{GS}=0V, I_S=-3A$	-	-	-1.2	V

Notes:

1. Repetitive Rating: Pulse width limited by maximum junction temperature.
2. Surface Mounted on FR4 Board, $t \leq 10$ sec.
3. Pulse Test: Pulse Width $\leq 300\mu s$, Duty Cycle $\leq 2\%$.
4. Guaranteed by design, not subject to production.
5. EAS condition : $T_j=25^\circ C, N: V_{DD}=20V, V_G=10V, L=0.5mH, R_g=25\Omega$. P: $V_{DD}=-20V, V_G=-10V, L=0.5mH, R_g=25\Omega$.

9 Package Information

SOP-8 Package Dimensions

Size Symbol	MIN(mm)	TYP(mm)	MAX(mm)	Size Symbol	MIN(mm)	TYP(mm)	MAX(mm)
A	-	-	1.75	D	4.70	4.90	5.10
A1	0.10	-	0.225	E	5.80	6.00	6.20
A2	1.30	1.40	1.50	E1	3.70	3.90	4.10
A3	0.60	0.65	0.70	e	1.27BSC		
b	0.39	-	0.48	h	0.25	-	0.50
b1	0.38	0.41	0.43	L	0.50		
c	0.21	-	0.26	L1	1.05BSC		
c1	0.19	0.20	0.21	θ	0	-	8°

SOP-8 Package Outlines

