

NST03N60K N-Channel Enhancement Mode Power MOSFET

1 Features and Benefits

- 100% Avalanche Tested
- Fast Switching
- Intrinsic capacitances and Qg minimized
- Parameters

$$V_{DS\ min@T_{jmax}} = 650V$$

$$R_{DS(ON)TYP} = 2.6\Omega$$

$$I_D = 3A$$

$$Q_g = 21nC$$

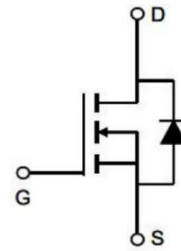
3 Description

The series of Power MOSFETs, the silicon N-channel Enhanced VDMOSFETs, is obtained by the self-aligned planar technology, which use Pt diffusion process.

Device information

Part Number	Package	Device Marking
NST03N60K	TO-252	NST03N60K

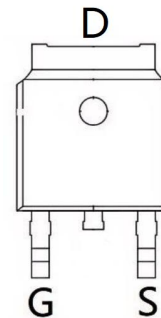
TO252 Pin Configuration



Schematic Diagram

2 Application

- Motor driver

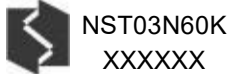


Pin Assignment

4 Selection Guide

Part Number	TYPE	R _{DS(ON)}	VDS	VTH
NST03N60K	N	2.6Ω	650V	4V

5 Ordering Guide

Part Number	LOGO	Package
NST03N60K		TO-252

6 Revision history

Version	Content	Time
V1.0	Create	2024.02.13

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7 Function Pin Description

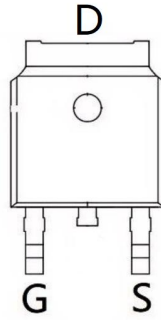


Figure7-1 3-Pin TO252 Top view

Table7-1 Lead Definitions

Symbol	Description
G	GATE
D	DRAIN
S	SOURCE

8 Product specifications

8.1 Absolute Maximum Ratings

PARAMETER	SYMBOL	MAX	UNIT
Drain-Source Voltage	V_{DS}	600	V
Gate-Source Voltage	V_{GS}	± 30	V
Drain Current-Continuous	$I_D(T_C=25^\circ C)$	3	A
	$I_D(T_C=100^\circ C)$	2.1	
Drain Current-Pulsed ^{BC}	I_{DM}	9	A
Single pulse avalanche energy ^D	EAS	225	mJ
Maximum Power Dissipation ^{AC}	P_D	64.5	W
Operating Junction and Storage Temperature Range	T_J, T_{STG}	-55 To 175	$^\circ C$

8.2 Thermal Characteristic

PARAMETER	SYMBOL	MAX	UNIT
Thermal Resistance,Junction-to-Case	R_{thJC}	2.33	$^\circ C/W$
Thermal Resistance,Junction-to-Ambient	R_{thJA}	50	$^\circ C/W$

8.3 Electrical Characteristics (TA=25 $^\circ C$ unless otherwise noted)

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Drain-Source Breakdown Voltage	BV_{DSS}	$V_{GS} = 0V, I_D = 250\mu A$	600	—	—	V
Gate-Threshold Voltage	$V_{th(GS)}$	$V_{DS} = V_{GS}, I_D = 250\mu A$	3	4	5	
Gate-Body Leakage	I_{GSS}	$V_{DS} = 0V, V_{GS} = \pm 20V$	—	—	± 100	nA
Zero Gate Voltage Drain Current(TC=25 $^\circ C$)	I_{DSS}	$V_{DS} = 600V, V_{GS} = 0V$	—	—	2	μA
Zero Gate Voltage Drain Current(TC=125 $^\circ C$)	I_{DSS}	$V_{DS} = 600V, V_{GS} = 0V$	—	—	200	
Drain-Source On-Resistance	$R_{DS(ON)}$	$V_{GS} = 10V, I_D = 1.5A$	—	2.6	3.3	Ω
Dynamic Characteristics						
Input Capacitance	C_{iss}	$V_{DS} = 40V, V_{GS} = 0V,$ $F = 1MHz$	—	439	—	pF
Output Capacitance	C_{oss}		—	34	—	
Reverse Transfer Capacitance	C_{rss}		—	4.4	—	
Intrinsic gate resistance	R_G	$f = 1 MHz$ open drain	—	2.9	—	Ω
Switching Capacitance						
Turn-On Delay Time	$t_{d(on)}$	$V_{DD} = 300V, I_D = 3A$ $V_{GS} = 10V, R_G = 10\Omega$	—	17.5	—	ns
Turn-On Rise Time	t_r		—	10	—	
Turn-Off Delay Time	$t_{d(off)}$		—	20	—	
Turn-Off Fall Time	t_f		—	10	—	
Total Gate Charge	Q_g	$V_{DS} = 420V, I_D = 3A$ $V_{GS} = 10V$	—	21	—	nC
Gate-Source Charge	Q_{gs}		—	3.9	—	
Gate-Drain Charge	Q_{gd}		—	5.88	—	

Drain-Source Diode Characteristics						
Source-drain current(Body Diode)	I_{SD}	$T_C=25^{\circ}C$	—	—	3	A
Pulsed Source-drain current(Body Diode)	I_{SDM}		—	—	9	
Forward On Voltage	V_{SD}	$T_J=25^{\circ}C, I_{SD} = 3A,$ $V_{GS} = 0V$	—	0.9	1.1	V
Reverse Recovery Time	t_{rr}	$T_J=25^{\circ}C, I_F = 3A,$ $di/dt=100A/\mu s$	—	55	—	ns
Reverse Recovery Charge	Q_{rr}		—	0.83	—	
PeakReverseRecoveryCurrent	I_{rm}		—	3	—	

Notes:

- 1.Repetitive Rating: Pulse width limited by maximum junction temperature
2. $T_J=25^{\circ}C, V_{DD}=50V, V_G=10V, R_G=25\Omega$

9 Package Information

TO-252 Package Information

SYMBOL	MILLIMETER			SYMBOL	MILLIMETER		
	MIN(mm)	TYP(mm)	MAX(mm)		MIN(mm)	NOM(mm)	MAX(mm)
A1	0.00	—	0.10	E	9.90	10.10	10.30
A2	2.20	2.30	2.40	E1	6.00	6.10	6.20
A3	1.02	1.07	1.12	E2	5.30REF		
b	0.65		0.77	e	2.286BSC		
b1	0.64	0.69	0.74	L	1.40	1.50	1.60
C	0.51	—	0.55	L2	0.90	—	1.25
c1	0.50	0.51	0.52	L3	0.60	0.80	1.00
D	6.50	6.60	6.70	L4	1.70	1.80	1.90
D1	5.33REF			θ	0		8°
D2	4.83REF						

TO-252 Package Outlines

