Description

The AL58263Q is an automotive AEC-Q100 grade 1 16-channel constant current LED driver with 16-bit grayscale Adaptive Pulse Density Modulation (APDM) PWM, supporting error diagnostics, power saving function and current gain control. This distinctive APDM technology abates the non-ideal IOUT distortion due to non-symmetric transient responses and enhances the refresh rate by separating efficiently the frame waveform.

The device operates over a 3V to 5.0V input voltage range, 15V output channel voltage, a fast 25MHz DCK input, and delivers up to 55mA of high accuracy current to each string of LED. Each channel average output current can be programmable independently via digital interface individually. All channels output current could be set by one external sensing resistor along with 6-bit global current control register.

The AL58263Q has built-in detection and diagnosis and LED open/short including error detection. Those errors results are stored in register for MCU to read out.

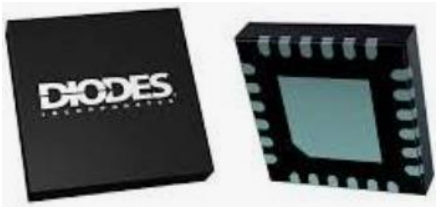
The AL58263Q is available in the Wettable Flank W-QFN4040-24/SWP (Type A1) package and specified over the -40°C to +125°C ambient temperature range.

Features

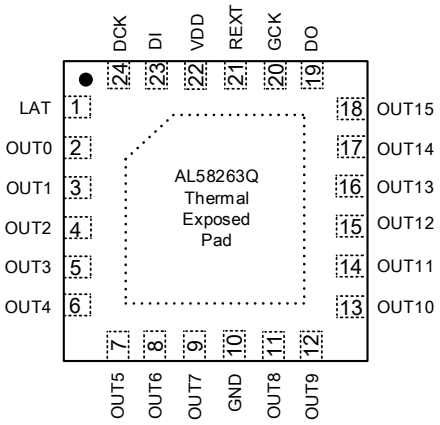
- AEC-Q100 Grade 1
- Input Voltage V_{DD}: 3V to 5.0V
- Output Current Range
  - 2 to 55mA/5.0V
  - ±0.1% (typ) Output Current Regulation
- 16 Constant-Current Sink Output Channel
  - 16-Bit Grayscale Resolution
  - 6-Bit Global Current Control
  - 15V Rated Output Channels
  - ±1.5% (typ) LED Current Accuracy Between Channels
  - ±3% (typ) LED Current Accuracy Between Chips
  - Stagger Outputs Delay for EMI Reduction
  - Cascaded Capability (max 1,440 Devices)
- Detection and Diagnosis
  - Error Detection Includes LED Open, LED Short, Output Port Leakage, Output Short-to-GND, Output Short-to-Power and REXT Short-to-GND
  - Pre-Overtemperature Warning
- 4-Wire Serial Interface +1 (LAT, DI, DO, DCK + GCK)
  - 25MHz Data Clock (DCK) Frequency for Data Transfer
  - Double Edge Gray Scale Clock up to 16MHZ (GCK)
  - External GCK Watchdog Timer
  - Zero Data and Sleep Mode for Power Saving
- Register Programmable Options
  - Regular PWM or Adaptive Pulse Density Modulation
  - Built Internal PWM or External Gray Scale Clock (GCK)
  - Short Detection Threshold Voltage Selection (2/3/4/4.5V)
- **Totally Lead-Free & Fully RoHS Compliant (Notes 1 & 2)**
- **Halogen and Antimony Free. "Green" Device (Note 3)**
- **The AL58263Q is suitable for automotive applications requiring specific change control; this part is AEC-Q100 qualified, PPAP capable, and manufactured in IATF16949 certified facilities.**
  https://www.diodes.com/quality/product-definitions/

Pin Assignments

(3D Photo – Not to Scale)



(Top View – Not to Scale)



W-QFN4040-24/SWP (Type A1)

Applications

- Automotive clusters
- Automotive local dimming displays
- Automotive front and back faceplates
- Automotive center stack displays
- Automotive interior and RGB lightings
- Automotive HVAC control panels
- Automotive gear shifter indicators
- Automotive exterior lightings

Notes:
1. No purposely added lead. Fully EU Directive 2002/95/EC (RoHS), 2011/65/EU (RoHS 2) & 2015/863/EU (RoHS 3) compliant.
2. See https://www.diodes.com/quality/lead-free/ for more information about Diodes Incorporated's definitions of Halogen- and Antimony-free, "Green" and Lead-free.
3. Halogen- and Antimony-free "Green" products are defined as those which contain <900ppm bromine, <900ppm chlorine (<1500ppm total Br + Cl) and <1000ppm antimony compounds.

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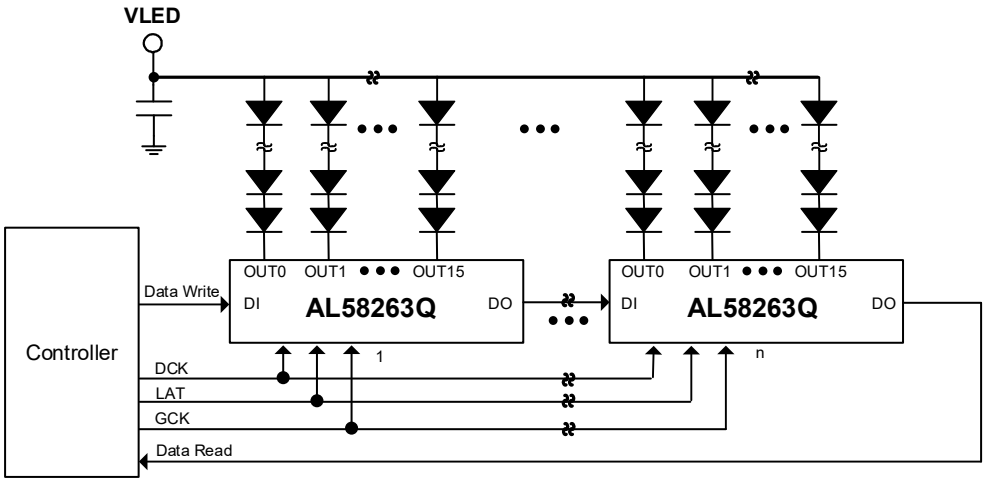
Typical Applications Circuit

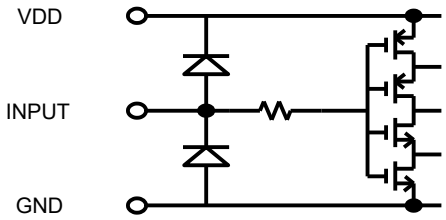


Pin Descriptions

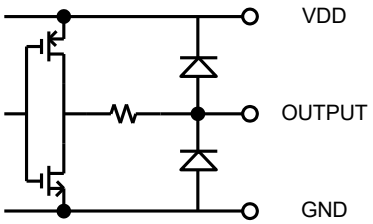
Pin Name	Pin Number W-QFN4040-24/SWP (Type A1)	Description
LAT	1	Input terminal of data strobe and mode setting. Combine DCK with LAT signal to execute the mode control.
OUT0 to OUT15	2 to 9 and 11 to 18	Sink constant-current outputs (open-drain).
GND	10	Ground terminal.
DO	19	Serial data output terminal.
GCK	20	External double-edge grayscale clock input for APDM operations.
REXT	21	External resistors connected between REXT and GND for output current value setting.
VDD	22	Supply voltage terminal.
DI	23	Serial data input terminal.
DCK	24	Synchronous clock input terminal for serial data transfer. Data is sampled at the rising edge of DCK.

Equivalent Circuit of Inputs and Outputs

1. DCK, DI, LAT, GCK Terminals



2. DO Terminal



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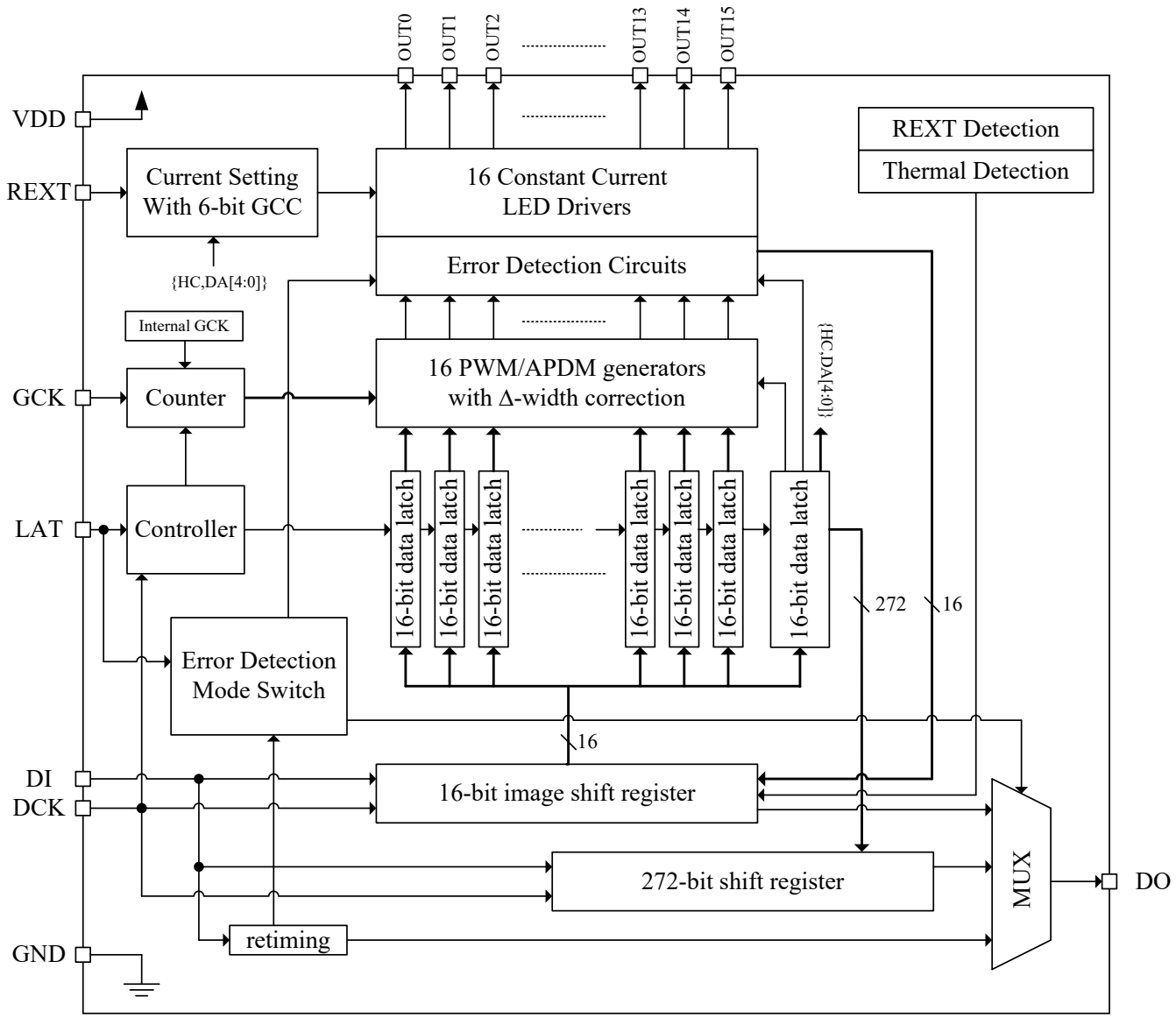
Functional Block Diagram



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Absolute Maximum Ratings (Notes 4 & 5)

Symbol	Parameters	Ratings	Unit
V_{DD}	Supply Voltage	-0.3 to 7.0	V
V_{DI}, V_{DCK}, V_{GCK}, V_{LAT}	Input Voltage	-0.3 to V_{DD}+0.3	V
I_{OUT}	Output Current	60	mA
V_{OUT}	Output Voltage	-0.3 to 16	V
f_{DCK}	Input Clock Frequency	25	MHz
f_{GCK}	Input Grayscale Frequency	16	MHz
I_{GND}	GND Terminal Current	960	mA

Notes: 4. Stresses greater than those listed under *Absolute Maximum Ratings* can cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions* is not implied. Exposure to *Absolute Maximum Ratings* for extended periods can affect device reliability.
5. All voltage values are with respect to ground terminal.

ESD Ratings

Symbol	Parameter	Value	Unit
V_{ESD}	Human Body Model (HBM)	2000	V
	Charged Device Model (CDM)	750	V

Package Thermal Data (Note 6)

Symbol	Parameter	Value	Unit
$R_{\Theta JA}$	Junction-to-Ambient Thermal Resistance	31.16	°C/W
$R_{\Theta JC(top)}$	Junction-to-Case (Top) Thermal Resistance	17.25	°C/W
$R_{\Theta JB}$	Junction-to-Board Thermal Resistance	9.34	°C/W
Ψ_{JT}	Junction-to-Top Characterization Parameter	0.41	°C/W
Ψ_{JB}	Junction-to-Board Characterization Parameter	9.14	°C/W
$R_{\Theta JC(bot)}$	Junction-to-Case (Bottom) Thermal Resistance	3.33	°C/W

Note: 6. Measured on EIA/JESD51-7, 4-layer PCB. For better thermal performance, larger copper pad for heatsink is needed.

Recommended Operating Conditions

Symbol	Parameter	Min	Typ	Max	Unit
V_{DD}	Operating Supply Voltage	3.0	3.3	5.0	V
I_{OUT}	Output Current (Note 7)	2	—	55	mA
V_{OUT}	Output Voltage	1	—	15	V
T_A	Ambient Temperature (Note 7)	-40	—	+125	°C
T_J	Junction Temperature	-40	—	+150	°C
T_{STG}	Storage Temperature	-55	—	+150	°C

Note: 7. Dependent on ambient temperature, LED voltage, package thermal limitation, and PCB layout.

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Electrical Characteristics (V_{DD} = 5.0V @T_A = -40°C to +125°C, unless otherwise specified.)

Characteristic	Symbol	Condition	Min	Typ	Max	Unit
Input Voltage "H" Level	V_{IH}	CMOS logic level	0.7V_{DD}	—	V_{DD}	V
Input Voltage "L" Level	V_{IL}	CMOS logic level	GND	—	0.3V_{DD}	
Output Leakage Current	I_{LK}	V_{OUT} = 15V	—	—	0.2	µA
Driving Current (DO)	I_{OL}	V_{OL} = 0.4V	1	3.4	5	mA
	I_{OH}	V_{OH} = V_{DD}-0.4	-5	-3.4	-1	
Output Current Skew (Channel-to-Channel) (Note 8)	dI_{OUT1}	V_{OUT} = 1.0 V R_{REXT} = 560Ω GCC = 101011 T_J = +25°C	—	±1.5	±3.5	%
Output Current Skew (Chip-to-Chip) (Note 9)	dI_{OUT2}		—	±3	±6	%
Output Voltage Regulation (Note 10)	% / V_{OUT}	R_{REXT} = 560Ω V_{OUT} = 1V to 3V	—	±0.1	±1	% / V
Supply Voltage Regulation (Note 11)	% / V_{DD}	R_{REXT} = 560Ω V_{DD} = 3V to 5.0V	—	±0.6	±1	
Supply Current (Note 12)	$I_{DD1(off)}$	R_{REXT} = 560Ω All outputs turn off	1	5.5	9.7	mA
	$I_{DD2(on)}$	R_{REXT} = 560Ω All outputs turn on	1	5.5	9.7	
Thermal Alarm Temperature	T_{AL}	—	—	+155	—	°C
Thermal Alarm Temperature Hysteresis	T_{AL_HYS}	—	—	+15	—	°C

Notes: 8. Channel-to-channel skew is defined by the formula below:

$$\Delta(\%) = \left[\frac{Iout_n}{\frac{(Iout_0 + Iout_1 + \ldots + Iout_{15})}{16}} - 1 \right] * 100\%$$

9. Chip-to-Chip skew is defined by the formula below:

$$\Delta(\%) = \left[\frac{\frac{(Iout_0 + Iout_0 + \ldots + Iout_{15})}{16} - (\text{Ideal Current at Temperature})}{(\text{Ideal Current at Temperature})} \right] * 100\%$$

10. Output voltage regulation is defined by the formula below:

$$\Delta(\%/V) = \left[\frac{Iout_n(@Vout_n = 3V) - Iout_n(@Vout_n = 1V)}{Iout_n(@Vout_n = 3V)} \right] * \frac{100\%}{3V - 1V}$$

11. Supply voltage regulation is defined by the formula below:

$$\Delta(\%/V) = \left[\frac{Iout_n(@V_{DD} = 5.5V) - Iout_n(@V_{DD} = 3V)}{Iout_n(@Vcc = 3V)} \right] * \frac{100\%}{5.5V - 3V}$$

12. IO excluded.

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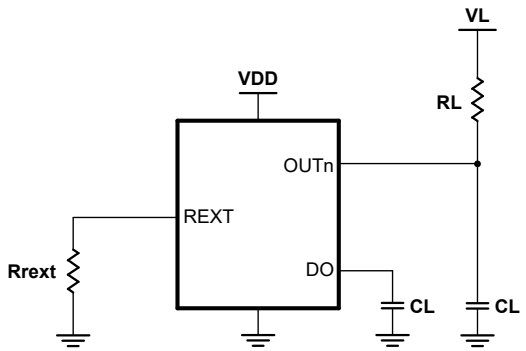
Switching Characteristics (V_{DD} = 5.0V @T_A = -40°C to +125°C, unless otherwise specified.) (Guaranteed by design)

Characteristic		Symbol	Condition	Min	Typ	Max	Unit
Propagation Delay ('L' to 'H')	DCK-DO	t_{PLH3}	$V_{IH} = V_{DD}$ V_{IL} = GND R_{REXT} = 560Ω V_L = 5.0V R_L = 150Ω C_L = 13pF	—	30	60	ns
Propagation Delay ('H' to 'L')	DCK-DO	t_{PHL3}		—	30	60	
Pulse Duration	LAT	$t_{w(LAT)}$		50	—	—	
	GCK	$t_{w(GCK)}$		20	—	—	
	DCK	$t_{w(DCK)}$		20	—	—	
Setup Time	LAT	$t_{su(LAT)}$		20	—	—	
	DI	$t_{su(D)}$		5	—	—	
Hold Time	LAT	$t_{h(LAT)}$		20	—	—	
	DI	$t_{h(D)}$		5	—	—	
Hold Time of Instruction		$t_{h(CM)}$		20	—	—	
LED Error Detection Time		terr1		500	—	—	
Short-to-Ground Detection Time		terr3		500	—	—	
Interval Between Two Command Pulses		tpls		230	250	—	
Wake-up Time from Sleep or 0-Data Mode		twake		—	—	4000	μs
Data Clock Frequency		f_{DCK}		—	—	25	MHz
Grayscale Clock Frequency (Double-Edge)		f_{GCK}		—	—	16	

Switching Characteristics Test Circuit



Switching Characteristics Test Circuit

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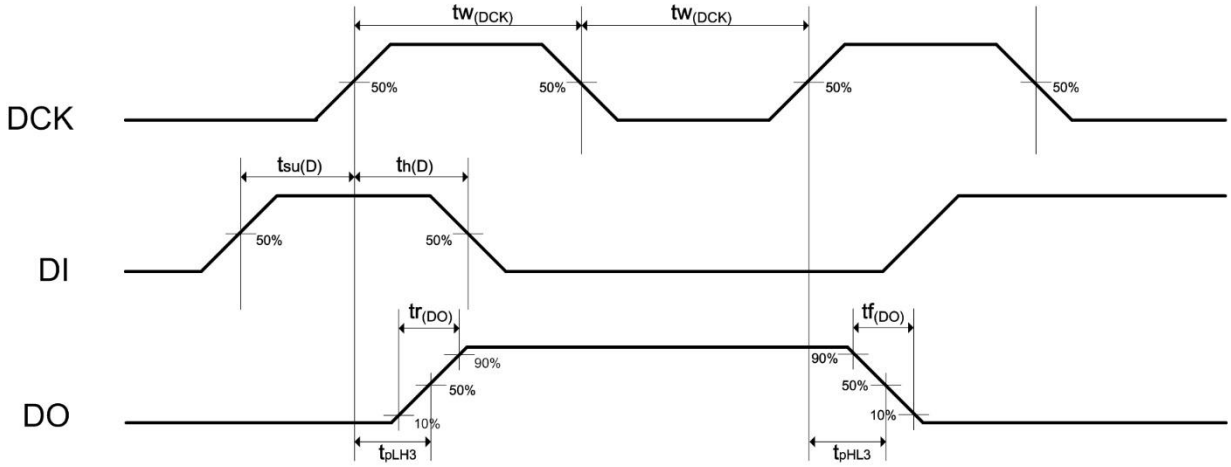
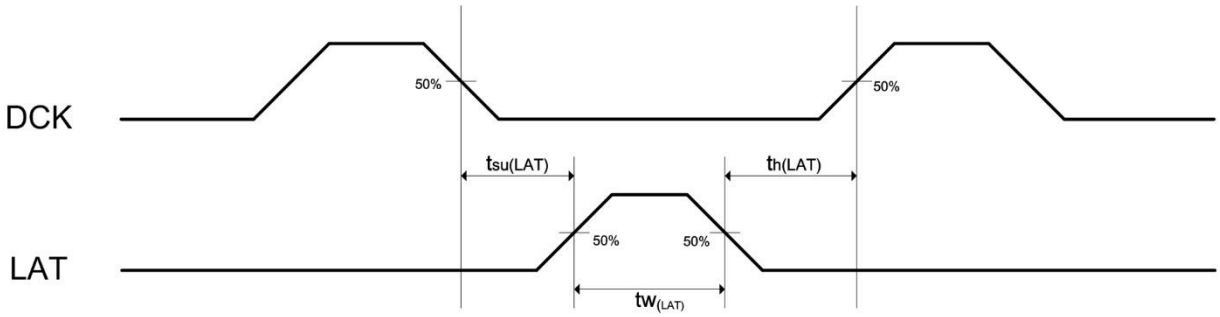
Timing Characteristics

Timing Diagram

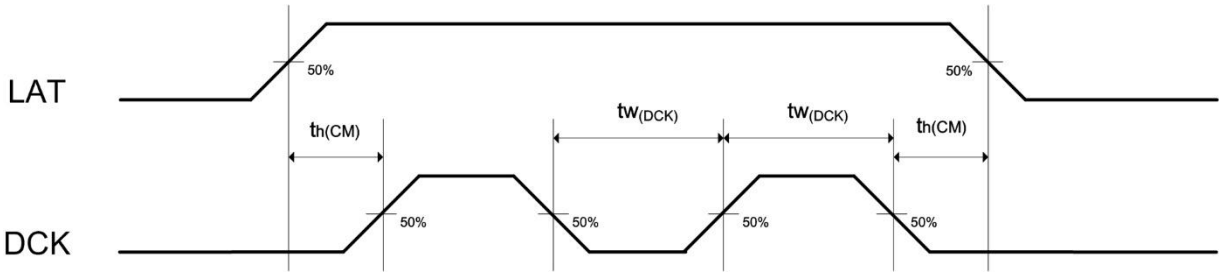
1. DCKI-DI, DO



2. GCK-LAT



3. LAT-DCK (Instruction)



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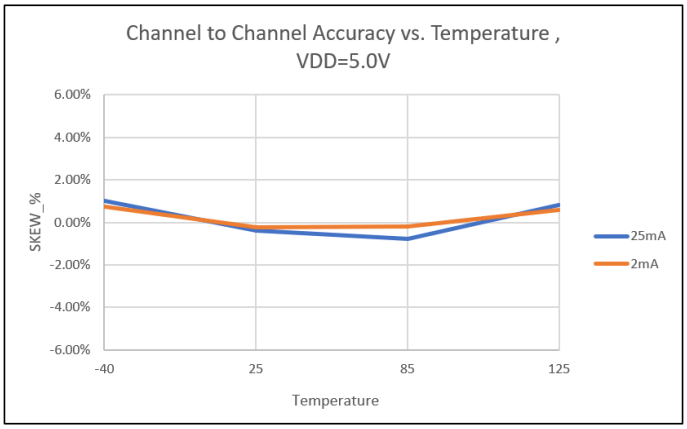
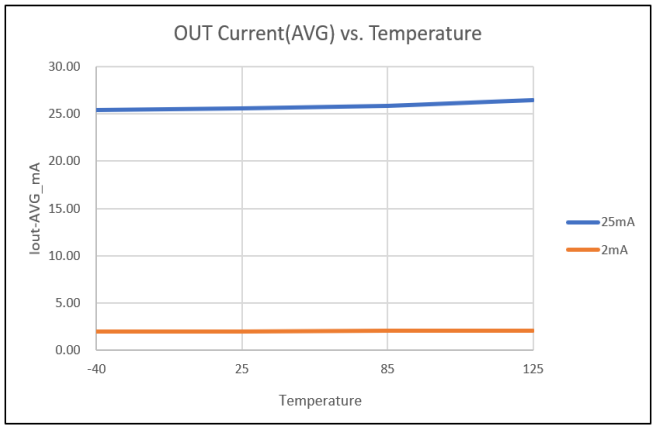
Typical Performance Characteristics (V_{DD} = 5V, -40°C < T_A < +125°C, unless otherwise specified.)



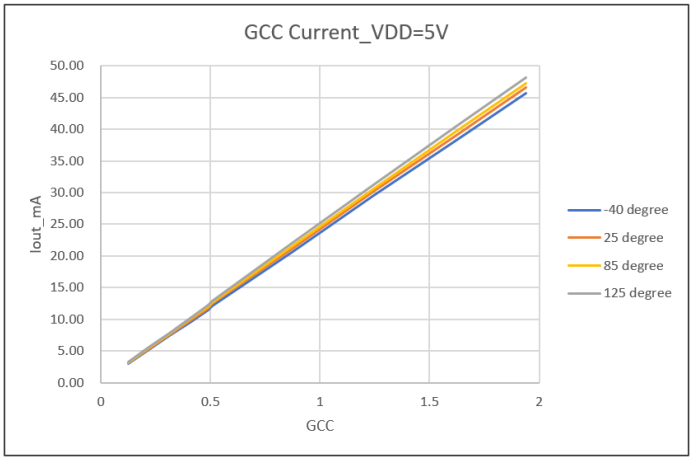
V_{DD} = 5V, I_{OUT} = 25mA, 2mA

Figure 1. Channel to Channel Accuracy vs. Temperature



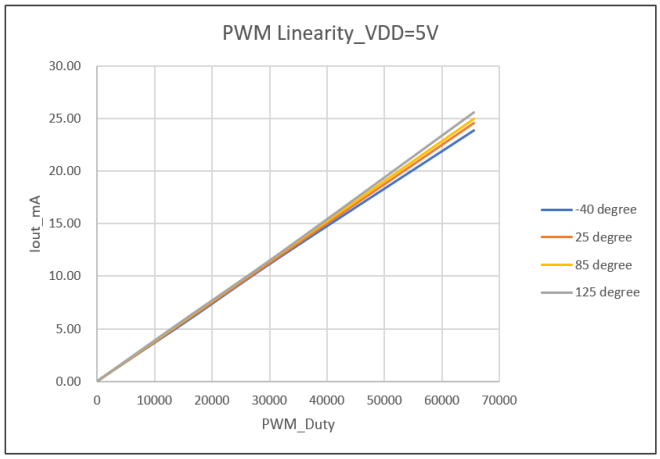
V_{DD} = 5V, I_{OUT} = 25mA, 2mA

Figure 2. Output Current (AVG) vs. Temperature



V_{DD} = 5V, I_{OUT} = 25mA

Figure 3. Gain Control Current vs. Temperature



V_{DD} = 5V, I_{OUT} = 25mA

Figure 4. PWM Linearity vs. Temperature

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Functional Descriptions

Fast Transient Response

The AL58263Q supports the fast transient response to make high image resolution possible. The GCK period of 50ns is enough to get a complete V_{OUT} waveform.

Stagger Outputs Delay

Large inrush currents will be induced when the system activates all the outputs at once. To reduce this interference of EMI, the AL58263Q is designed to have a constant length of delay time (around 16ns) between two output groups. The first group is OUT2n and the second group is OUT2n+1 (n = 0 to 7).

Global Current Control (GCC)

The AL58263Q provides 6bits global current control (GCC) which could adjust the output current by 64 steps.

The GCC bits are included in the command data defined as follows:

F	E	D	C	B	A	9	8	7	6	5	4	3	2	1	0
—	—	—	—	—	—	HC	DA4	DA3	DA2	DA1	DA0	—	—	—	—

The relationship between the Gain value and GCC bits is described below:

HC = 1, Gain ≒ (3 x D + 33) / 65 x (1-0.001 x D), the gain range is from 0.508 to 1.878

HC = 0, Gain ≒ (3 x D + 32) / 256 x (1-0.0006 x D), the gain range is from 0.125 to 0.479

Where $D = DA4 \times 2^4 + DA3 \times 2^3 + DA2 \times 2^2 + DA1 \times 2^1 + DA0 \times 2^0$

For example, HC = 1 and DA[4:0] = 11000

$D = 1 \times 2^4 + 1 \times 2^3 + 0 \times 2^2 + 0 \times 2^1 + 0 \times 2^0 = 24$

Gain ≒ (3 x 24 + 33) / 65 x (1-0.001 x 24) ≒1.577

Reference Resistor

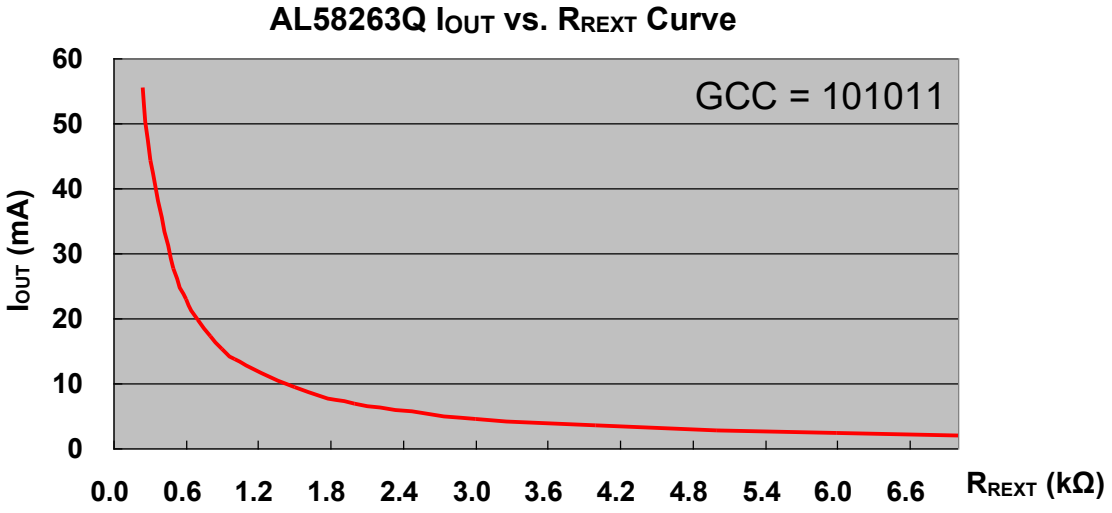
The constant current values are determined by an external resistor placed between REXT pin and GND pin. The following formula is utilized to calculate the current value:

$$I_{OUT}\ (mA) \fallingdotseq 13.45 / R_{REXT}(k\Omega) \times Gain$$

This 13.45 constant center at 10mA may need to be adjusted slightly based on users' application and test conditions.

Where R_{REXT} is a resistor placed between REXT and GND.

For example, I_{OUT} is around 24.12mA when R_{REXT} = 560Ω and with GCC = 101011



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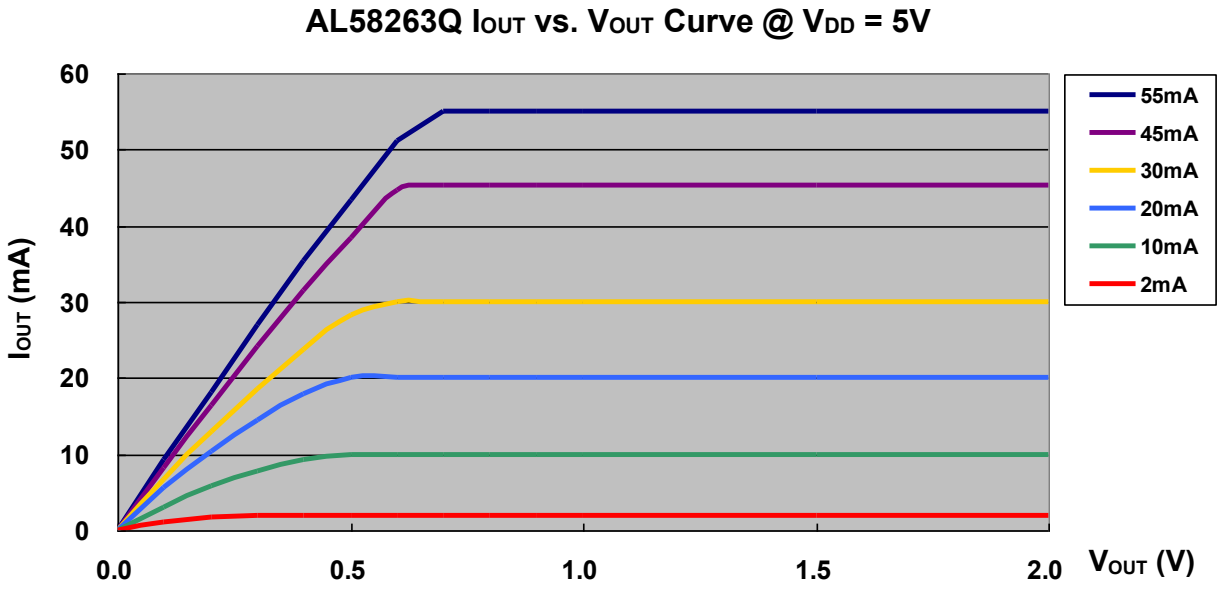
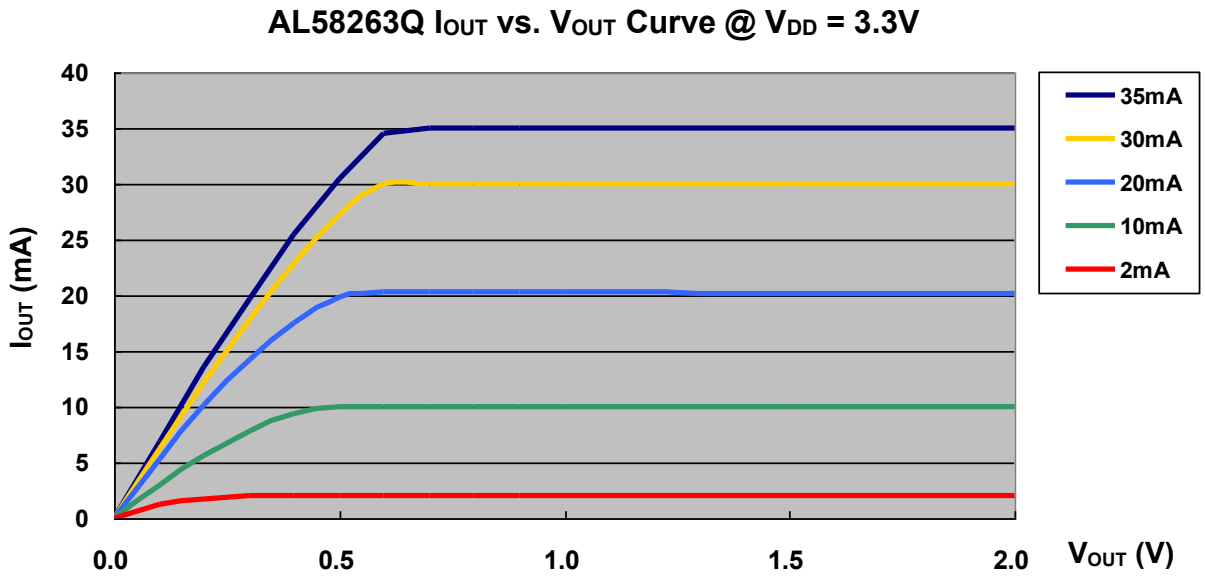
Functional Descriptions (continued)

Constant-Current Output

The current characteristics could maintain invariable in the influence of loading voltage. Therefore, the AL58263Q could minimize the interference of different LED forward voltages and produce the constant current. The following figures illustrating the suitable output voltage should be determined in order to keep an excellent performance.





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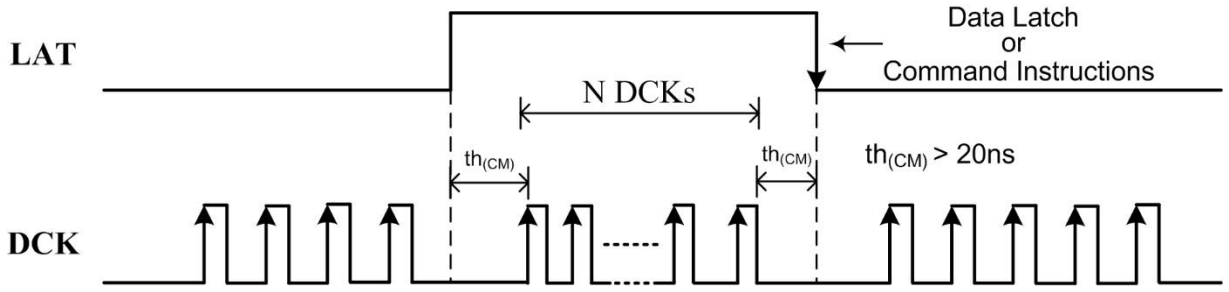
Functional Descriptions (continued)

Control Instructions



Instruction Name	Number of DCK Pulses when LAT is at High	Function Description
Data Latch	0 or 1	Strobes image data into temporary registers. In this time, constant current outputs are not updated to a new frame data.
Global Latch	2 or 3	Strobes image data from temporary registers into an APDM/PWM generator. In this time, constant current outputs are updated to a new frame data.
Reading Image Data and Command Data	6 or 7	Read out image data and command data from the latch cell to the 272bits shift registers. And the read data could shift out from DO pin by serial DCK pulses.
Return to Normal Mode	8 or 9	Switch Back from the reading data mode to the normal operating mode.
Writing Command	10 or 11	Strobes command data from the 16bits shift register into the command latch cell.
Reset APDM/PWM Counter	12 or 13	This instruction will reset APDM/PWM counter to synchronize a new frame if CMD[11] = ”H”.

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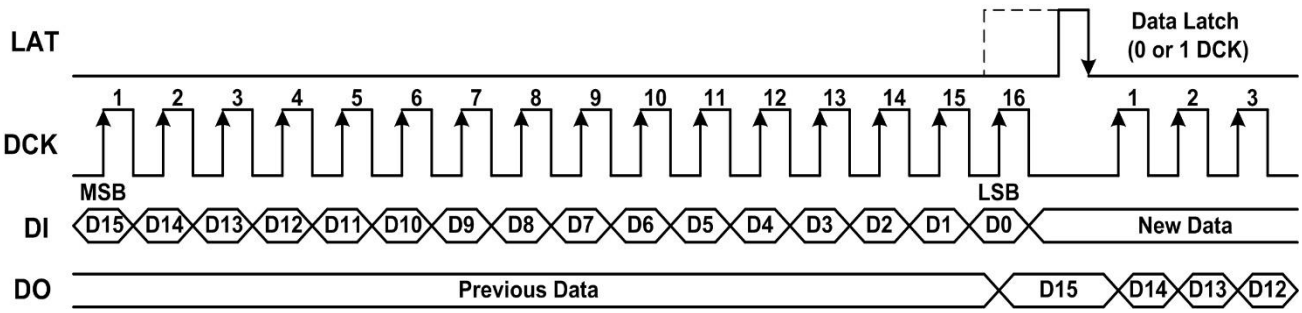
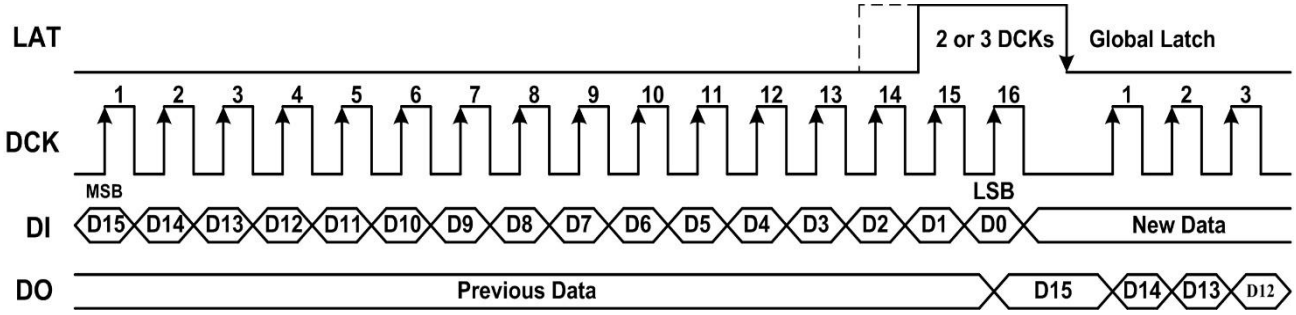
Functional Descriptions (continued)

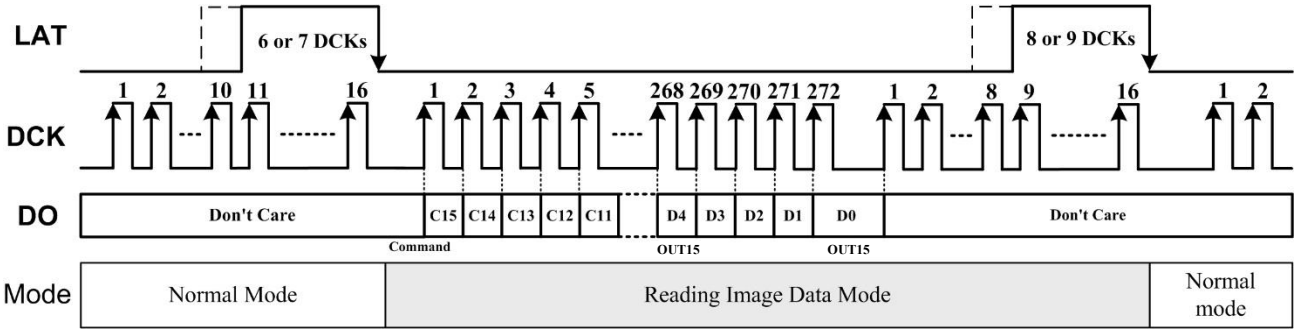
Data Latch



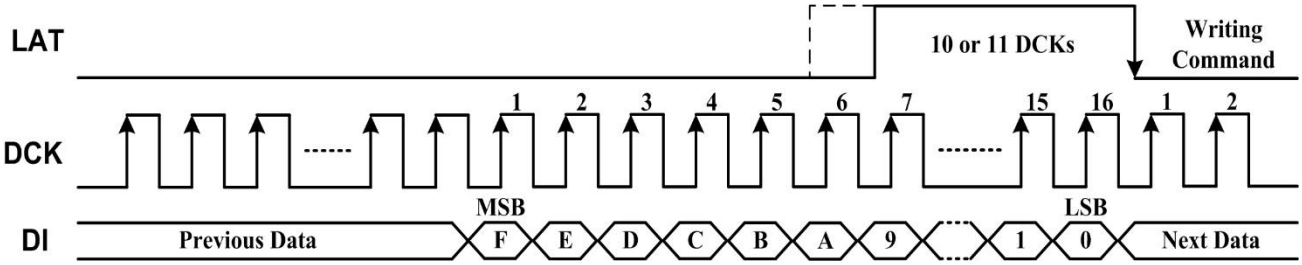
Global Latch



Reading Image Data and Command Data



Writing Command



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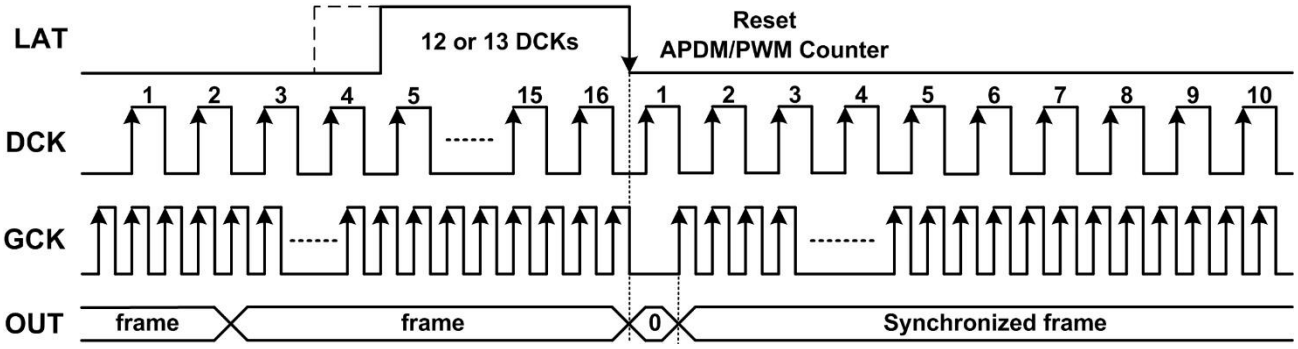
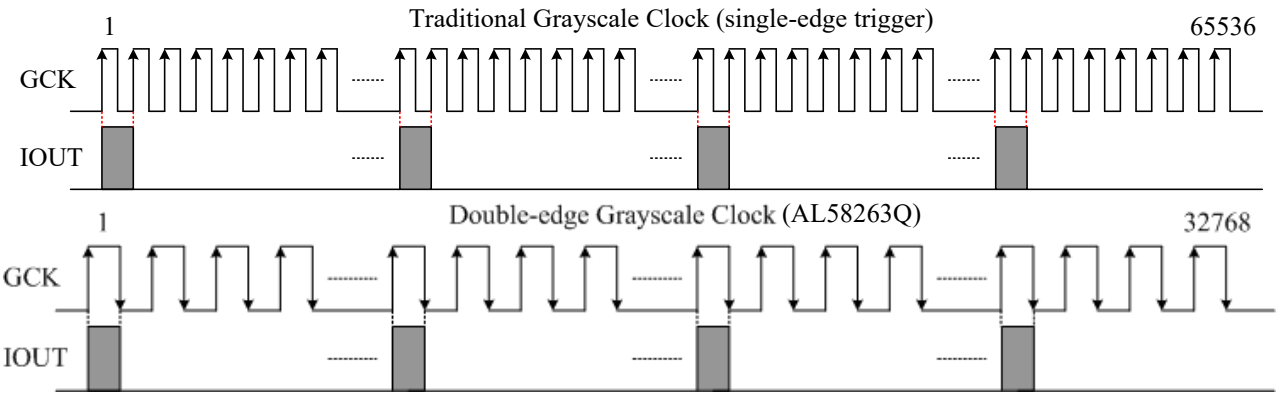
Functional Descriptions (continued)

Reset APDM/PWM Counter (Set CMD[11] = ”1”)



EMI Reduction Grayscale Clock (Double-Edge Grayscale Clock)



A whole period of 16bits resolution must be composed by 65536 traditional grayscale clocks because constant current outputs only are triggered at the rising edge of clocks. Therefore, a controller has to transmit fast grayscale clocks in order to accomplish high refresh rate when users adopt traditional PWM chips. The AL58263Q supports a specific mode of double-edge grayscale clocks which trigger both at rising and falling edges of clocks. By this approach, a whole period of 16bits resolution is composed by only 32768 double-edge grayscale clocks and the electromagnetic interference would be decreased substantially due to slow grayscale clocks.

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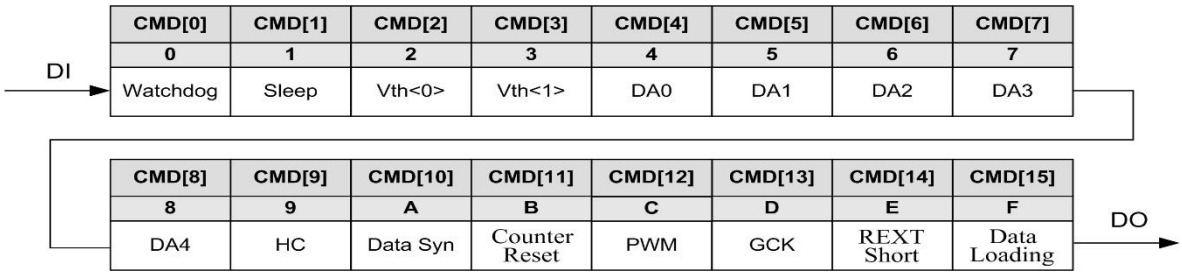
Functional Descriptions (continued)

Command Data Format



CMD Bit	Initial Value	Value	Function	Description
CMD[15]	1'b0	1'b0	Mode0	Data transmitting format: 15 times of data latch + one global latch
		1'b1	Mode1	Data transmitting format: 16 times of data latch + one global latch
CMD[14]	1'b0	1'b0	Enable	When the voltage of REXT is below 0.15V, all outputs will be forced off.
		1'b1	Disable	Disable
CMD[13]	1'b0	1'b0	External GCK	The GCK signal stems from an external source.
		1'b1	Internal GCK	The GCK signal stems from an internal oscillator, typ 1.7MHz at 3.3V and 2.8MHz at 5V (When CMD[13] = "1", please set CMD[0] = "0")
CMD[12]	1'b0	1'b0	APDM Mode	Enter the PWM mode to abate the transient loss when AL58263Q is as a PWM generator. when CMD[12] = 1'b0 => APDM mode when CMD[12] = 1'b1 => PWM mode
		1'b1	PWM Mode	
CMD[11]	1'b0	1'b0	Disable	Disable
		1'b1	Enable	Execute counter reset by inserting 12 or 13 DCKs (rising edge) when LAT keeps at high.
CMD[10]	1'b0	1'b0	Auto Synchronization	When the device receives a latch signal, the new frame is updated until the end of old frame.
		1'b1	Manual Synchronization	When the device receives a latch signal, the new frame is updated immediately
CMD[9:4]	6'b101011	6'b000000 to 6'b111111	G.C.C	6bits DA data for global current control (Allow 64-step programmable current gain)
CMD[3:2]	2'b00	2'b00 2'b01 2'b10 2'b11	2.0V 3.0V 4.0V 4.5V	Threshold voltage for LED short detection (Both at V_{DD} = 5V and 3.3V)
CMD[1]	1'b0	1'b0	Disable	Enter 0-data power saving mode when 16bits PWM data of 16ch are all zeros.
		1'b1	Enable	
CMD[0]	1'b0	1'b0	Disable	GCK watchdog All IOUTs will be turned off automatically when GCK keeps high or low level over 30ms. (Result can be read out by "Thermal Detection Mode" or "Rext Detection Mode")
		1'b1	Enable	

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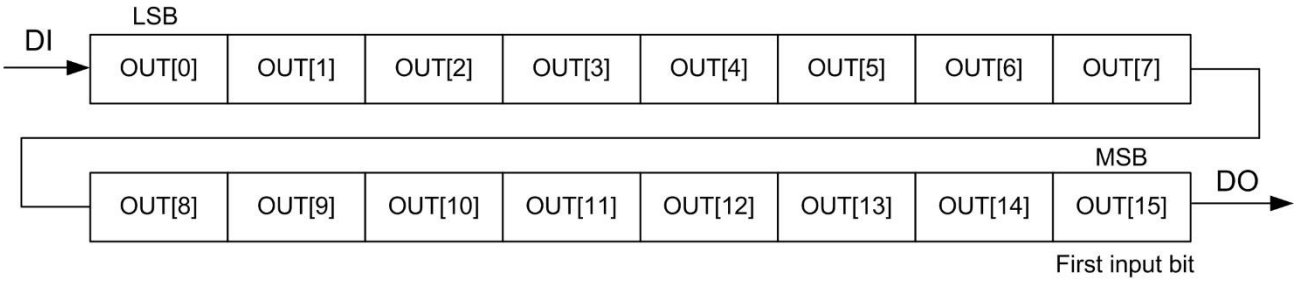
Functional Descriptions (continued)

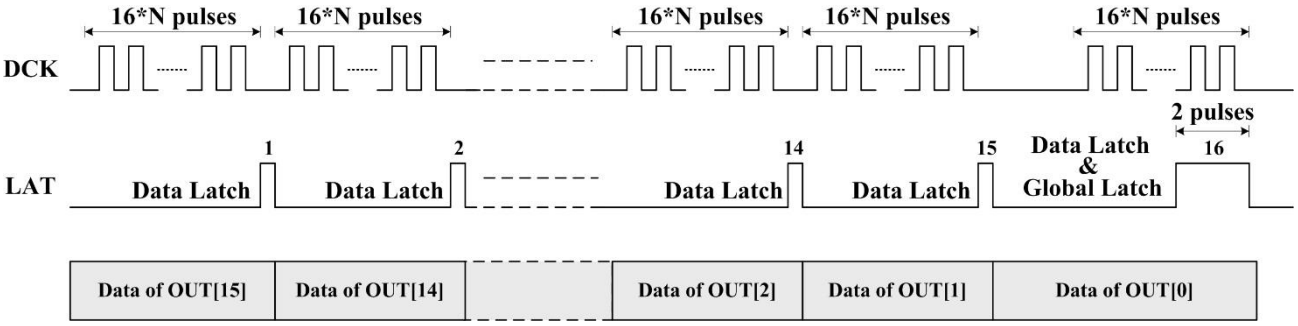
Image Data Format



16bits APDM/PWM data are transmitted into the 16bits shift register according to the format illustrated above. The first input bit is the most significant bit of each channel.

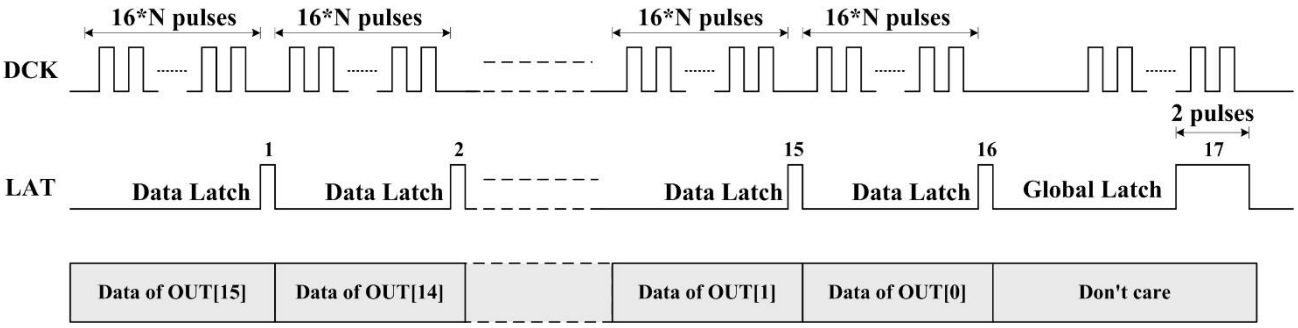
Data Transmitting Protocol

MODE0 (CMD[15] = “0”)



This data transmitting mode is comprised of 15 data latches and one global latch. The first data latch strobes image data for OUT[15]. And the last global latch strobes image data for OUT[0] and loads all image data of 16 channels into the APDM/PWM generator. N is the number of devices in series.

MODE1 (CMD[15] = “1”)



This data transmitting mode is comprised of 16 data latches and one global latch. The first data latch strobes image data for OUT[15]. And the last global latch loads all image data of 16 channels into the APDM/PWM generator but doesn’t strobe any image data for output channels. N is the number of devices in series.

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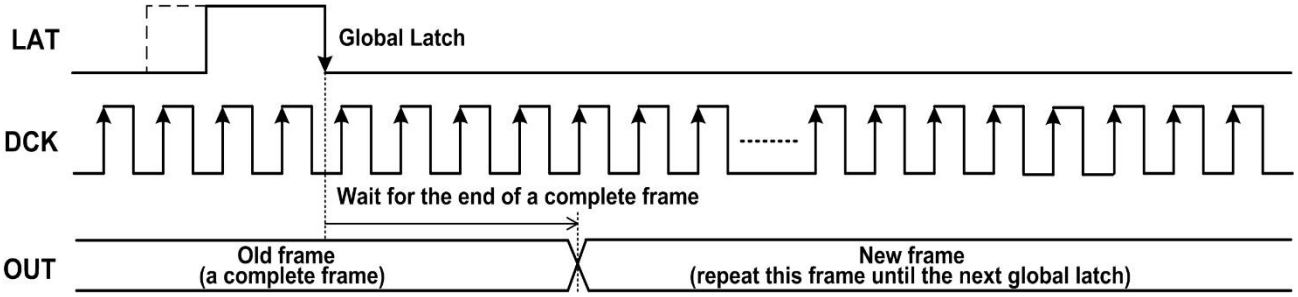
Functional Descriptions (continued)

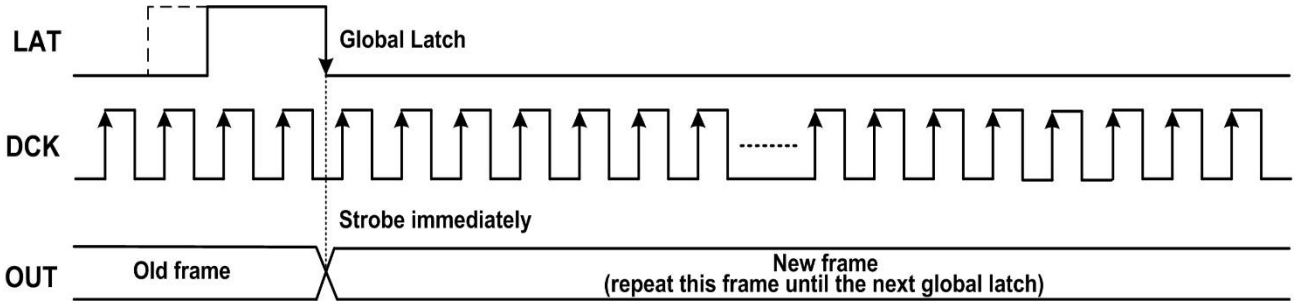
Data Synchronization

Auto Synchronization (CMD[10] = “0”)



The AL58263Q could abate the grayscale loss during the renewal of frame by this approach of auto synchronization. When the command bit CMD[10] is set to ”0”, this function could be executed automatically. After a global latch, all OUTs would accomplish a complete frame of old data and then update new frame data. Therefore, each frame maintains the fixed time and the assigned grayscale. A controller just provides a free-running GCK for grayscale display in this mode.

Manual Synchronization (CMD[10] = “1”)



When the command bit CMD[10] is set to ”1”, the new frame data would be updated immediately. The old frame loses probably a little grayscale due to a non-complete frame time. In this mode, a controller must calculate carefully the number of GCKs in order to synchronize a frame.

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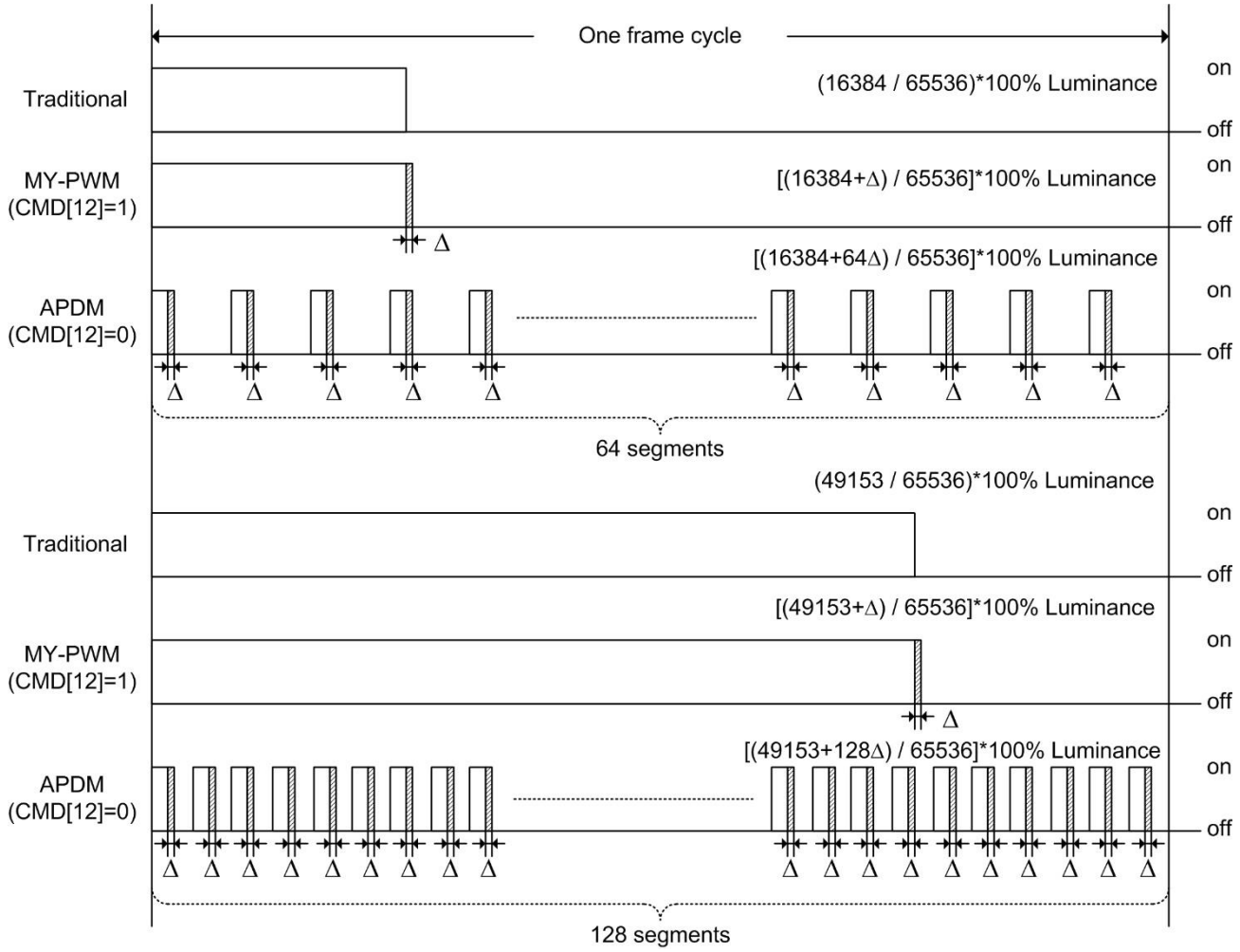
Functional Descriptions (continued)

Adaptive Pulse Density Modulation with Δ-Width Correction



Adaptive Pulse Density Modulation (APDM) is a technique to improve output current waveform distortion and increase visual refresh rate. The adaptive output waveform is determined automatically by the grayscale value. When all outputs operate at high grayscale resolution (grayscale resolution ≥ 50%), the output waveform is divided into 128 segments to increase visual refresh rate. Otherwise, the output waveform is divided into 64 segments at low grayscale resolution to improve output current waveform distortion. And the Δ-width correction (Δ≠0) is used to compensate the non-ideal output current transient response.

When CMD[12] = ”0”, the output waveform operates according to APDM.
When CMD[12] = ”1”, the output waveform is a form of non-scrambling PWM in order to drive high power LED and decrease the transient loss.

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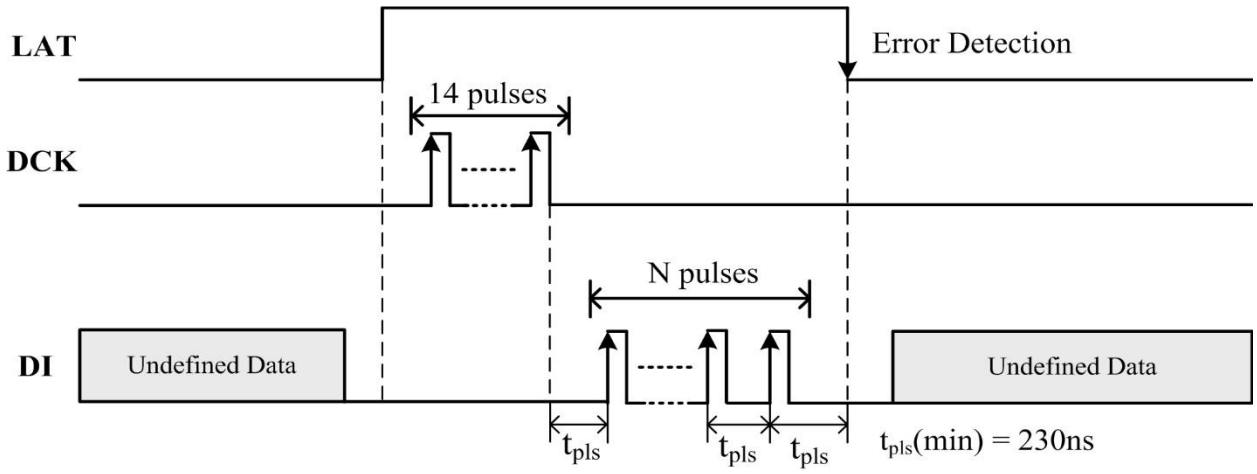
Functional Descriptions (continued)

Diagnosis and Protections

Error Detection Mode Instructions



Instruction Name	Number of DI Pulses when LAT is at High	Function Description
LED Open Detection	2	Execute the LED Open Detection no matter what the image data is. The image strobe will occur at the falling edge of LAT signal.
LED Short Detection	4	Execute the LED Short Detection no matter what the image data is. The image strobe will occur at the falling edge of LAT signal.
Short-to-GND Detection	6	Execute the Short-to-GND Detection no matter what the image data is. The device will detect each IOUT pin if short-to-ground or not. The image strobe will occur at the falling edge of LAT signal.
Thermal Detection & Watchdog Result Read Out	8	The device will load thermal detection result and watchdog detection result into the 16th and 1st image shift register by this instruction. The thermal error occurs when the junction temperature is over +155°C.
LED Smart Detection	10	Execute the LED Smart Detection no matter what the image data is. The device will detect LED Open and LED Short error simultaneously by this instruction. The image strobe will occur at the falling edge of LAT signal.
Sleep Mode	12	This instruction forces the device into Sleep Mode at the falling edge of LAT signal, then keeps GCK = high most internal circuits will shut down. The device will be activated in the following LAT signal.
REXT Pin Detection & Watchdog Result Read Out	14	The device will load REXT detection result and watchdog detection result into the 16th and 1st image shift register by this instruction. The REXT error occurs when the REXT pin is short-to-GND or above 2.5V.

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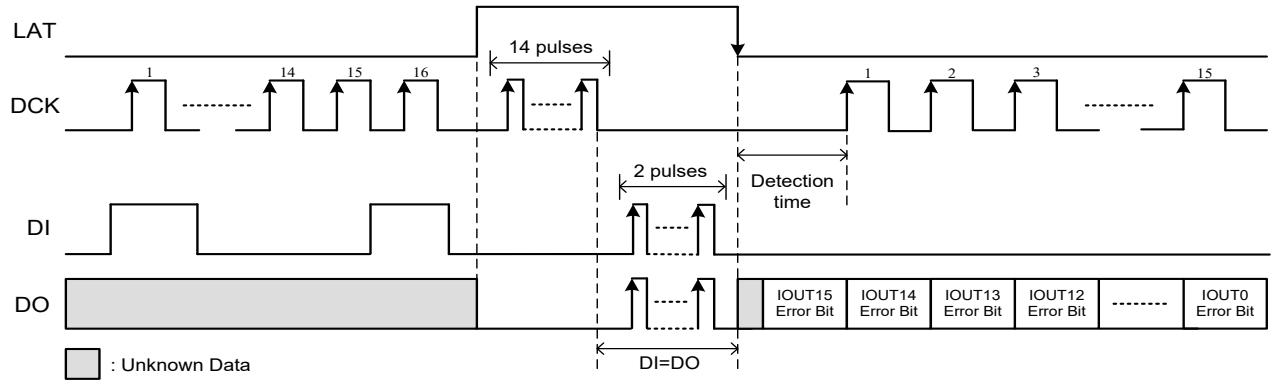
Functional Descriptions (continued)

Diagnosis and Protections (continued)

Error Bit

Error Bit	Symbol	Description
0	Error	When errors, such as open errors, short errors, short-to-GND errors, and thermal errors (PreOTP), are detected in the channel, the error bit, zero, will be loaded into the corresponding image shift register.
1	Normal	In the detecting mode, the bit, one, will be loaded into the corresponding image shift register if the device is under normal operating conditions.

LED Open Error Detection



When the LED open error detection instruction is executed, it is necessary to input two DI pulses in the Error Detection Mode. No matter what the image latch data is, the output ports of the AL58263Q will turn on with 0.1mA for error detection. The detection time is defined from the falling edge of LAT to the rising edge of following DCK.

When the voltage of IOUT pins is below 0.3V, the error bit, zero, will be loaded into the corresponding image shift register. The error bit will be shifted out from the DO pin on the synchronization of the rising edge of DCK. And a retiming DO signal, which is similar to DI signal, appears when the LAT signal stays in high level for cascading applications.

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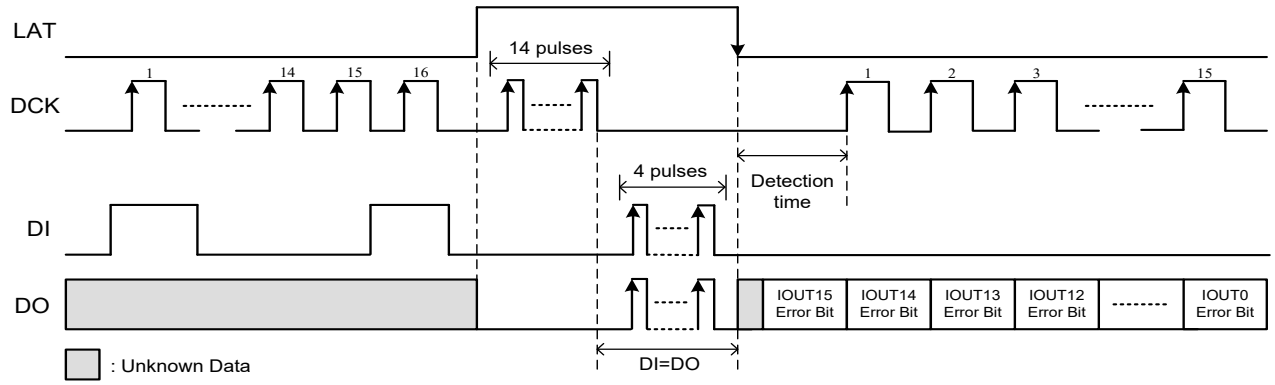
Functional Descriptions (continued)

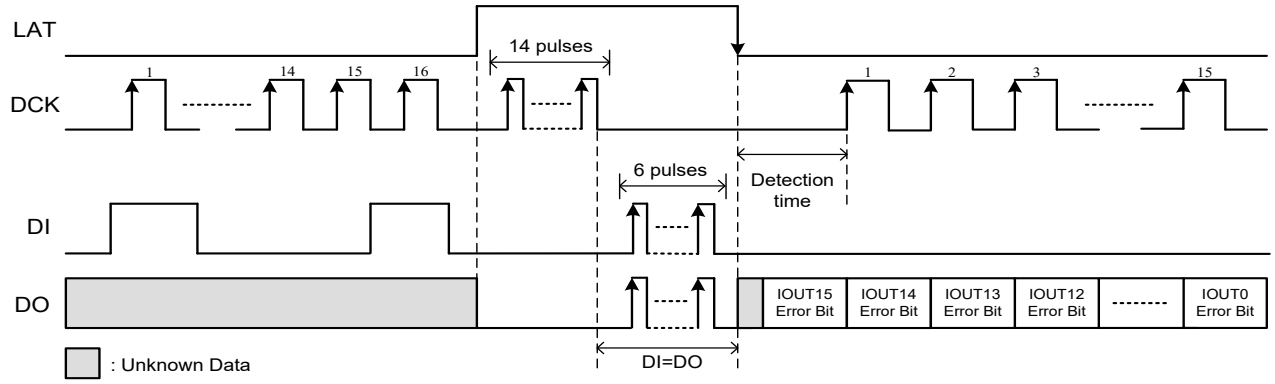
Diagnosis and Protections (continued)

LED Short Error Detection (Output Short-to-Power Included)



When the LED short error detection instruction is executed, it is necessary to input four DI pulses in the Error Detection Mode. No matter what the image latch data is, the output ports of the AL58263Q will turn on with 0.1mA for error detection. The detection time is defined from the falling edge of LAT to the rising edge of following DCK. When the voltage of IOUT pins is above the threshold voltage of LED short detection determined by CMD[14:13], the error bit, zero, will be loaded into the corresponding image shift register. The error bit will be shifted out from the DO pin on the synchronization of the rising edge of DCK. And a retiming DO signal, which is similar to DI signal, appears when the LAT signal stays in high level for cascading applications.

Short-to-GND Error Detection (Output Port Leakage Included)



When the short-to-GND error detection instruction is executed, it is necessary to input six DI pulses in the Error Detection Mode. No matter what the image latch data is, this instruction forces the output ports of the AL58263Q to turn off for error detection. The detection time is defined from the falling edge of LAT to the rising edge of following DCK.

When the voltage of IOUT pins is below 0.3V, the error bit, zero, will be loaded into the corresponding image shift register. The error bit will be shifted out from the DO pin on the synchronization of the rising edge of DCK. And a retiming DO signal, which is similar to DI signal, appears when the LAT signal stays in high level for cascading applications.

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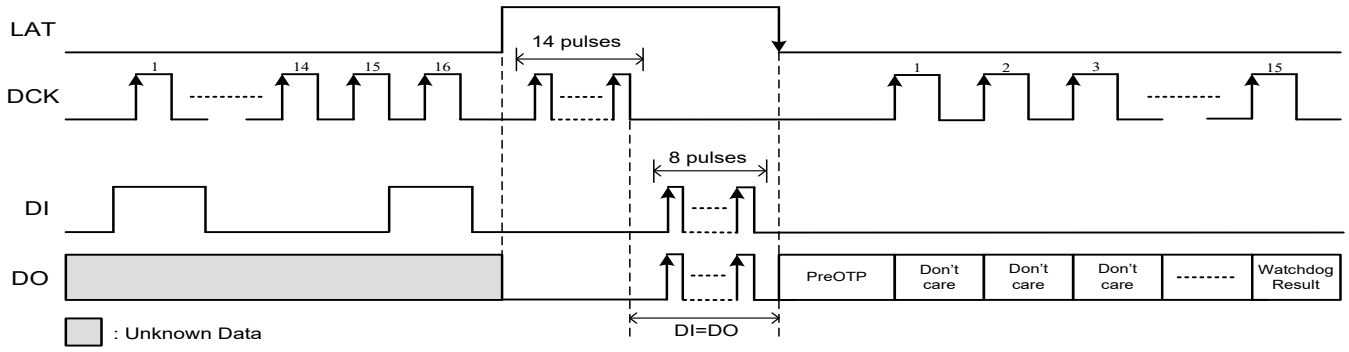
Functional Descriptions (continued)

Diagnosis and Protections (continued)

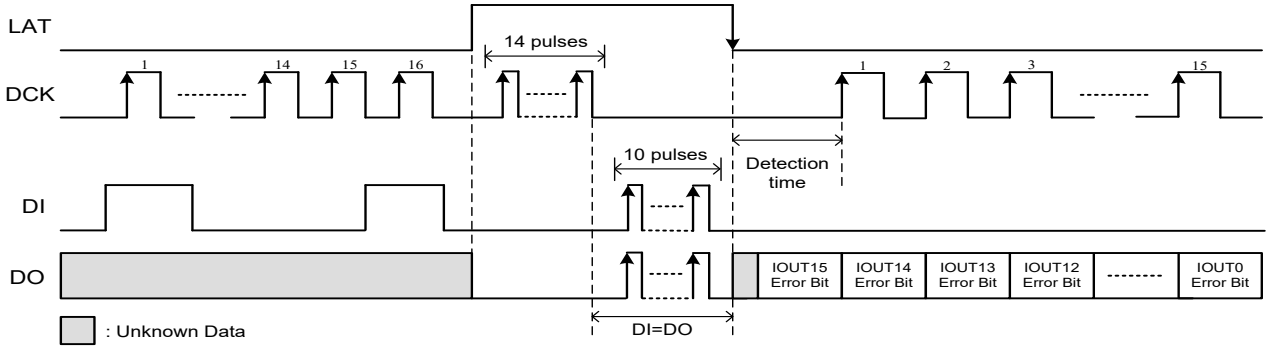
Pre-OTP Warning - Thermal Detection & Watchdog Result Read Out

The AL58263Q has pre-thermal warning threshold of +155°C (typical).



When the thermal detection instruction is executed, it is necessary to input eight DI pulses in the Error Detection Mode. AL58263Q will judge of junction temperature by the instruction. If the junction temperature is over +155°C, it will lead to thermal error. The device will load the PreOTP and watchdog result into the 16th and 1st image shift register and fill out the other image shift registers with bit code, 1. The error report will be shifted out from the DO pin on the synchronization of the rising edge of DCK. And a retiming DO signal, which is similar to DI signal, appears when the LAT signal stays in high level for cascading applications. When CMD[0] = 1 and GCK keeps low or high over 30ms, the watchdog result would be "0", otherwise it would be "1".

LED Smart Detection



When the LED smart detection instruction is executed, it is necessary to input ten DI pulses in the Error Detection Mode. No matter what the image latch data is, the output ports of the AL58263Q will turn on with 0.1mA for error detection. The detection time is defined from the falling edge of LAT to the rising edge of following DCK. When the voltage of IOUT pins is below 0.3V for LED open detection or above the threshold voltage of LED short detection determined by CMD[14:13], the error bit, zero, will be loaded into the corresponding image shift register. The error bit will be shifted out from the DO pin on the synchronization of the rising edge of DCK. And a retiming DO signal, which is similar to DI signal, appears when the LAT signal stays in high level for cascading applications.

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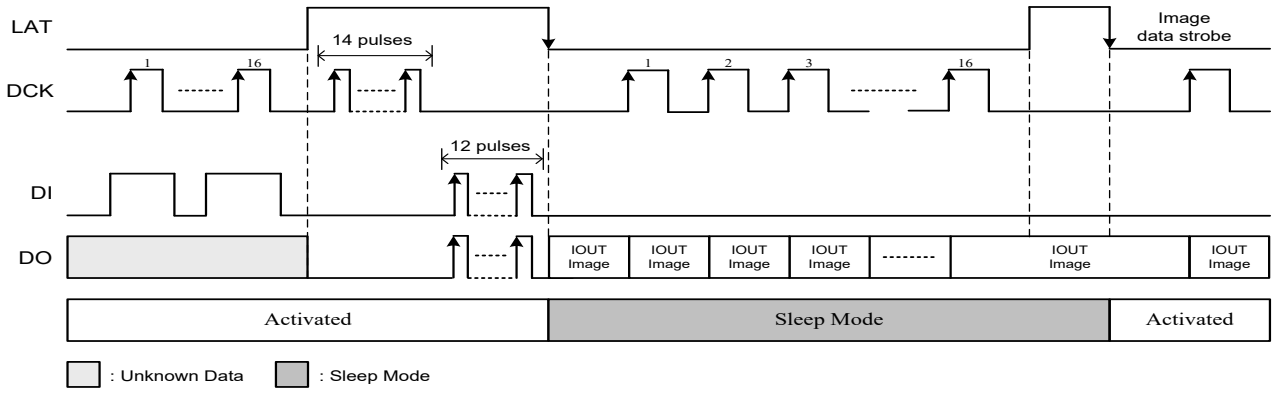
Functional Descriptions (continued)

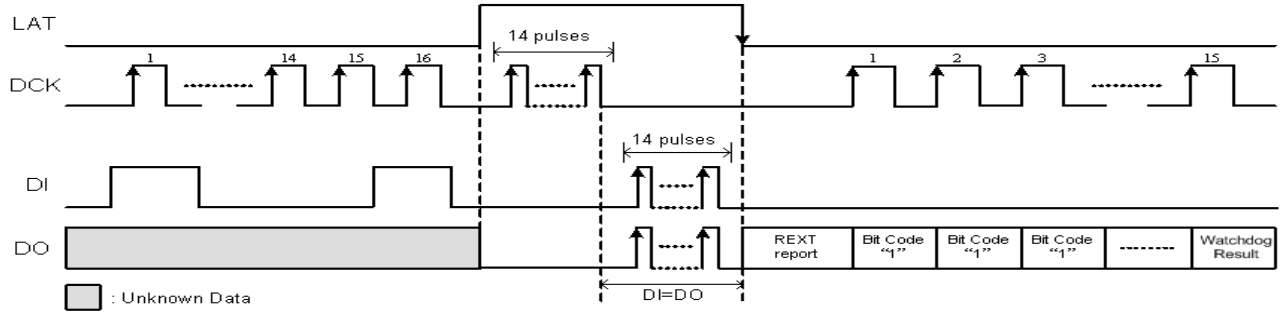
Diagnosis and Protections (continued)

Sleep Mode



For power saving, the AL58263Q supports the sleep mode to turn off most circuits. It is necessary to input twelve pulses in the Error Detection Mode to execute this instruction and then keeps GCK = high at sleep mode. In the sleep mode, the supply current maintains < 0.1mA because most analog circuits are shut down, but the digital interface is still activated in order to receive external digital data. The AL58263Q will enter sleep mode at the falling edge of this LAT signal and revive at the falling edge of following LAT signal. The serial image data will be shifted out from the DO pin on the synchronization of the rising edge of DCK. And a retiming DO signal, which is similar to DI signal, appears when the LAT signal stays in high level for cascading applications.

REXT Detection & Watchdog Result Read Out



When the REXT detection instruction is executed, it is necessary to input fourteen DI pulses in the Error Detection Mode. The AL58263Q will detect the voltage of REXT pin by the instruction. If the REXT pin is open or above 2.5V or below 0.15V, it will lead to REXT error. The device will load the REXT report and watchdog result into the 16th and 1st image shift register and fill out the other image shift registers with bit code, 1. The error report will be shifted out from the DO pin on the synchronization of the rising edge of DCK. And a retiming DO signal, which is similar to DI signal, appears when the LAT signal stays in high level for cascading applications. When CMD[0] = 1 and GCK keeps low or high over 30ms, the watchdog result would be "0", otherwise it would be "1".

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Functional Descriptions (continued)

Power Dissipation

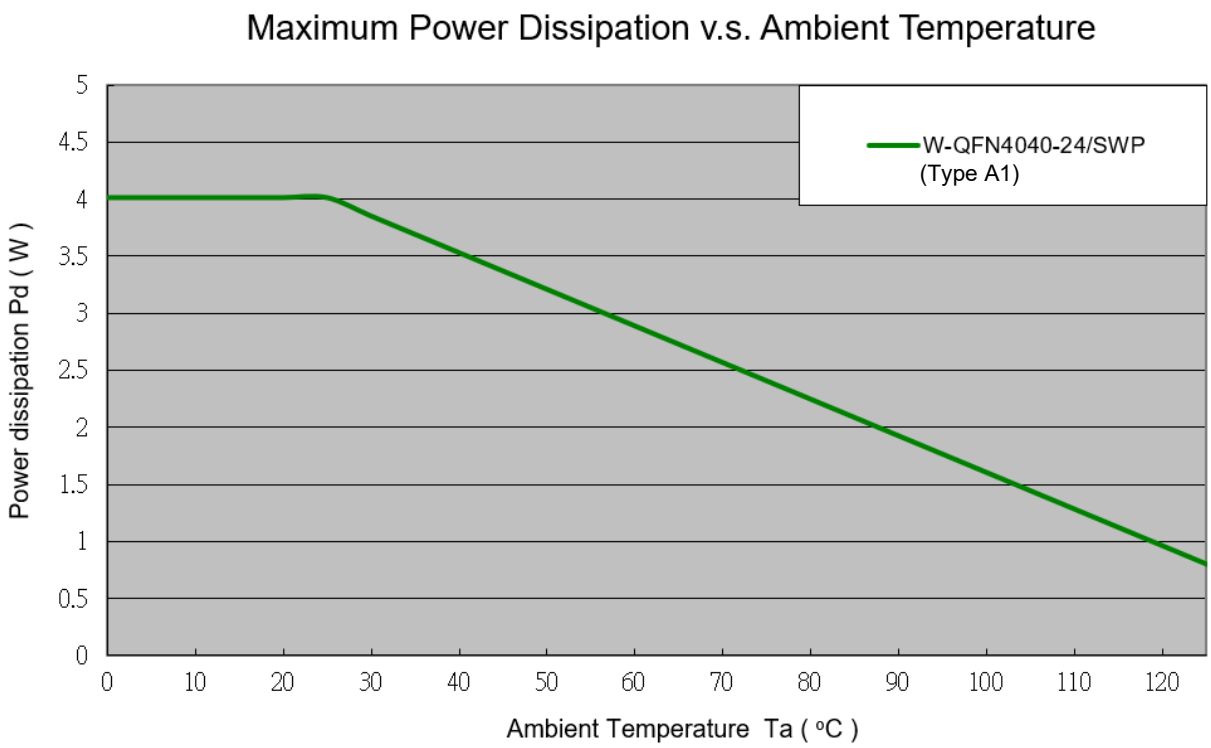
When the 16 output channels are turned on, the practical power dissipation is determined by the following equation:

$$PD\ (practical) = V_{DD} \times I_{DD} + Vout_{(0)} \times Iout_{(0)} \times Duty_{(0)} + \cdots + Vout_{(N)} \times Iout_{(N)} \times Duty_{(N)}\ ,\ where\ N=1\ to\ 15$$

In secure operating conditions, the power consumption of an integrated chip should be less than the maximum permissible power dissipation which is determined by the package types and ambient temperature. The formula for maximum power dissipation is described as follows:

$$PD\ (max) = \frac{Tj(max)(^{\circ}C) - Ta(^{\circ}C)}{Rth(j\text{-}a)(^{\circ}C/Watt)}$$

The PD(max) declines as the ambient temperature raises. Therefore, suitable operating conditions should be designed with caution according to the chosen package and the ambient temperature. The following figure illustrates the relation between the maximum power dissipation and the ambient temperature.



Design Tools (Note 13)

- AL58263Q Demo Boards
- AL58263Q Calculator
- Demo Board Gerber File for PCB Layout Reference

Note: 13. Diodes Incorporated's design tools can be found on our website at https://www.diodes.com/design/tools/.

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Ordering Information

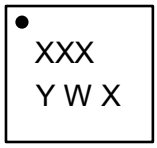
AL58263Q XXXXXX - X

- Product Name: AL58263Q
- Package: DKZW24: W-QFN4040-24/SWP (Type A1)
- Packing: 13: Tape & Reel

Orderable Part Number	Package	Packing	
		Qty.	Carrier
AL58263QDKZW24-13	W-QFN4040-24/SWP (Type A1)	3,000	Tape and Reel

Marking Information

(Top View)



XXX : Identification Code
Y : Year : 0 to 9 (ex: 4 = 2024)
W : Week : A to Z : week 1 to 26;
a to z : week 27 to 52; z represents week 52 and 53
X : Internal Code

Orderable Part Number	Package	Identification Code
AL58263QDKZW24-13	W-QFN4040-24/SWP (Type A1)	J7Q

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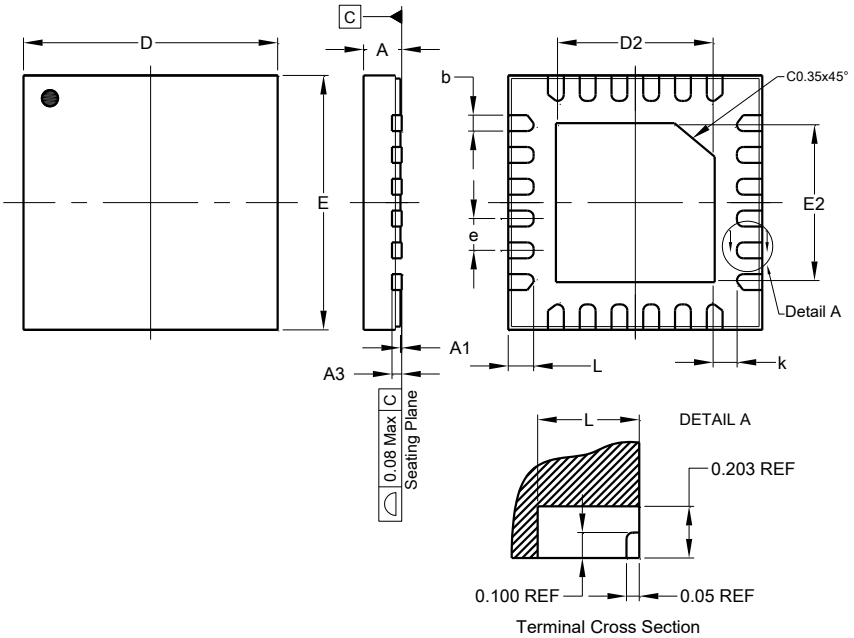
Package Outline Dimensions

Please see http://www.diodes.com/package-outlines.html for the latest version.

W-QFN4040-24/SWP (Type A1)

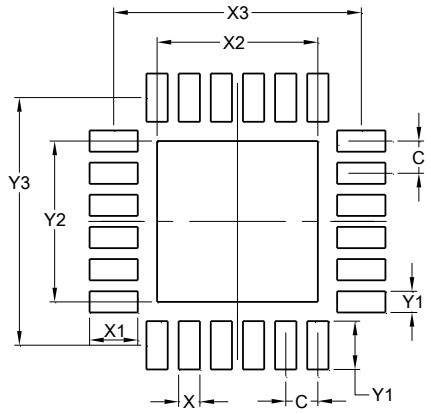


W-QFN4040-24/SWP (Type A1)			
Dim	**Min**	**Max**	**Typ**
A	0.70	0.80	0.75
A1	0.00	0.05	0.02
A3	0.203 REF		
b	0.18	0.30	0.25
D	3.90	4.10	4.00
D2	2.45	2.55	2.50
E	3.90	4.10	4.00
E2	2.45	2.55	2.50
e	0.50 BSC		
k	0.20	--	--
L	0.35	0.45	0.40
All Dimensions in mm			

Suggested Pad Layout

Please see http://www.diodes.com/package-outlines.html for the latest version.

W-QFN4040-24/SWP (Type A1)



Dimensions	Value (in mm)
C	0.500
X	0.300
X1	0.750
X2	2.500
X3	3.850
Y	0.750
Y1	0.300
Y2	2.500
Y3	3.850

Tape and Reel Information

Please see https://www.diodes.com/assets/Packaging-Support-Docs/AP02007.pdf for tape and reel details.

Mechanical Data

- Moisture Sensitivity: Level 1 per J-STD-020
- Terminals: Finish – Matte Tin Plated Leads, Solderable per JESD22-B102 e3
- Weight: 0.037 grams (Approximate)

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