

## Features

- Using external 32.768kHz quartz crystal
- Supports I<sup>2</sup>C-Bus's high speed mode(400kHz)
- Includes time (Hour/Minute/Second) and calendar (Year/Month/Date/Day) counter functions (BCD code)
- Programmable square wave output signal
- Oscillator stop flag
- Low backup current: typ. 400nA at V<sub>DD</sub>=3.0V and T<sub>A</sub>=25°C
- Operating range: 1.7V to 5.5V
- Operating Temperature Range: -40~125 °C

## Applications

- Digital still camera
- Digital video camera
- Printers
- Copy machines
- Mobile equipment
- Battery powered devices

## Description

The PCF8563T-NF serial real-time clock is a low-power clock/calendar with a programmable square-wave output.

Address and data are transferred serially via a 2-wire bidirectional bus. The clock/calendar provides seconds, minutes, hours, day, date, month, and year information. The date at the end of the month is automatically adjusted for months with fewer than 31 days, including corrections for leap year. The clock operates in the 24-hour format indicator.

Table 1 shows the basic functions of PCF8563T-NF. More details are shown in section: overview of functions.

## Ordering Information

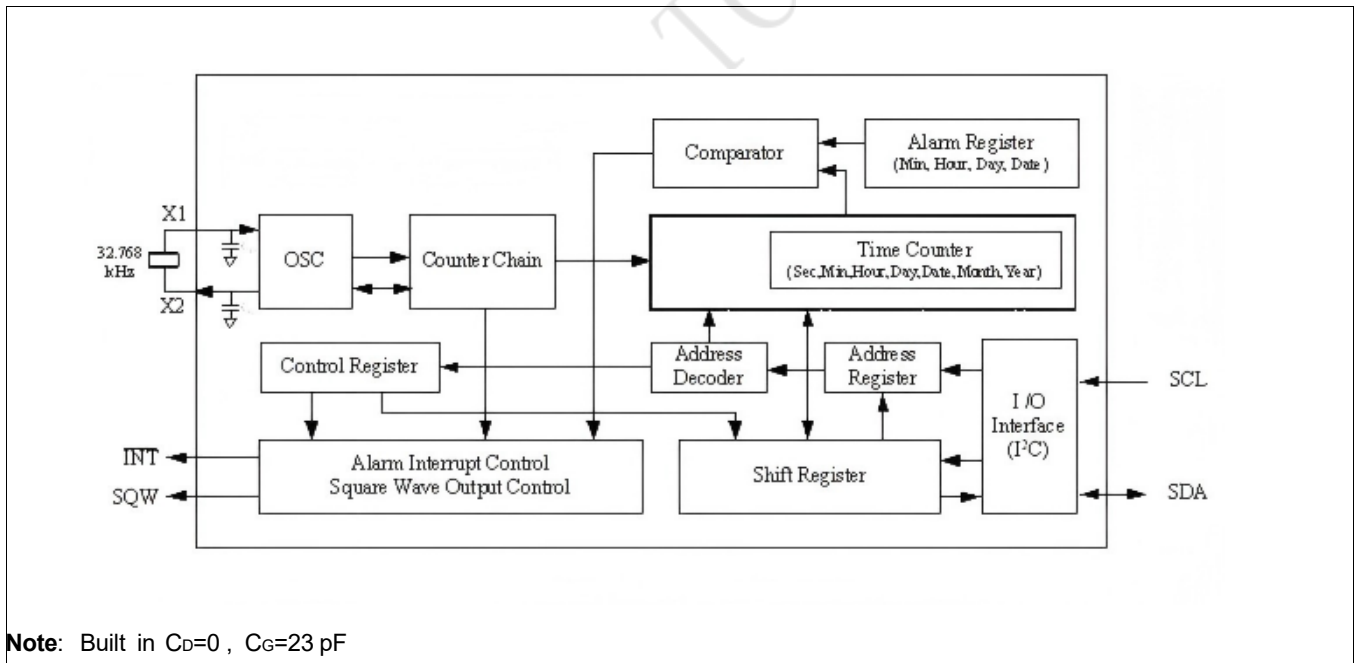
Green Package

| Part Number 1 | Package | Description | Part Number 2 |
|---------------|---------|-------------|---------------|
| FRTC8563M     |         | MSOP8       | PCF8563TS-NF  |
| FRTC8563S     |         | SOP8        | PCF8563T-NF   |

**Table 1. Basic functions of PCF8563T-NF**

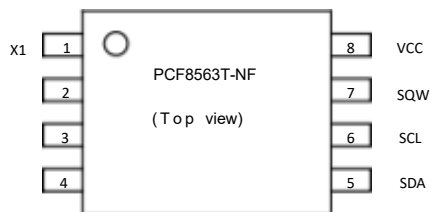
| Item | Function                             |                                 | PCF8563T-NF            |   |
|------|--------------------------------------|---------------------------------|------------------------|---|
| 1    | Oscillator                           | Source: Crystal: 32.768kHz      | √                      |   |
|      |                                      | Oscillator enable/disable       | -                      |   |
|      |                                      | Oscillator fail detect          | √                      |   |
| 2    | Time                                 | Time display                    | 12-hour                | - |
|      |                                      |                                 | 24-hour                | √ |
|      |                                      | Century bit                     |                        | √ |
|      |                                      | Time count chain enable/disable |                        | √ |
| 3    | Interrupt                            | Alarm interrupt                 |                        | √ |
| 4    | Programmable square wave output (Hz) |                                 | 1, 32, 1.024k, 32.768k |   |
| 5    | Communication                        | 2-wire I <sup>2</sup> C bus     |                        | √ |
|      |                                      | Burst mode                      |                        | - |
| 6    | Control                              | Write protection                |                        | - |
|      |                                      | External clock test mode        |                        | √ |
|      |                                      | Power-on reset override         |                        | √ |

## Function Block



**Figure 1. Function Block of PCF8563T-NF**

## Pin Configuration



## Pin Description

| Pin No. | Pin Name | Type | Description                                                                                                                                                              |
|---------|----------|------|--------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 1       | X1       | I    | <b>Oscillator Circuit Input.</b> Together with X2 , 32 .768 kHz crystal is connected between them .                                                                      |
| 2       | X2       | O    | <b>Oscillator Circuit Output.</b> Together with X1 , 32 .768kHz crystal is connected between them .                                                                      |
| 3       | / INT    | O    | <b>Interrupt Output.</b> Open drain, active low.                                                                                                                         |
| 4       | GND      | P    | <b>Ground.</b>                                                                                                                                                           |
| 5       | SDA      | I/O  | <b>Serial Data Input/output</b> SDA is the input/output pin for the 2-wire serial interface .The SDA pin is open-drain output and requires an external pull-up resistor. |
| 6       | SCL      | I    | <b>Serial Clock Input.</b> SCL is used to synchronize data movement on the I <sup>2</sup> C serial interface.                                                            |
| 7       | SQW      | O    | <b>Clock Output.</b> Open drain. Four frequencies selectable: 32.768 k , 1.024k, 32, 1Hz when SQWE bit is set to 1.                                                      |
| 8       | VCC      | P    | <b>Power.</b>                                                                                                                                                            |

## Function Description

### 1. Clock function

CPU can read or write data including the year (last two digits), month, date, day, hour, minute, and second. Any (two - digit) year that is a multiple of 4 is treated as a leap year and calculated automatically as such until the year 2100.

### 2. Alarm function

These devices have one alarm system that outputs interrupt signals from INT of PCF8563T-NF when the date, day of the week, hour, minute or second correspond to the setting.

Each of them may output interrupt signal separately at a specified time.

The alarm may be selectable between on and off for matching alarm or repeating alarm.

### 3. Programmable square wave output

A square wave output enable bit controls square wave output at pin 7. 4 frequencies are selectable: 1, 32, 1.024k, 32.768k Hz.

### 4. Interface with CPU

Data is read and written via the I<sup>2</sup>C bus interface using two signal lines: SCL (clock) and SDA (data).

Since the output of the I/O pin SDA is open drain, a pull-up resistor should be used on the circuit board if the CPU output I/O is also open drain.

The SCL's maximum clock frequency is 400 kHz, which supports the I<sup>2</sup>C bus's high-speed mode.

### 5. Oscillator fail detect

When oscillator fail, OSF bit will be set.

### 6. Oscillator enable/disable

Only time count chain can be enable or disable by STOP bit.

### 7. Reset function

The PCF8563T-NF includes an internal reset circuit which is active whenever the oscillator is stopped. In the reset state the I<sup>2</sup>C-bus logic is initialized and all registers, including the address pointer, are cleared with the exception of bits FE, OSF, TD1, TD0, TESTC and AE which are set to logic 1.

## Registers

### 001. Allocation of registers

| Addr.<br>(hex) *1 | Function (time range<br>BCD format) | Register definition |       |       |       |       |       |       |       |
|-------------------|-------------------------------------|---------------------|-------|-------|-------|-------|-------|-------|-------|
|                   |                                     | Bit 7               | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 |
| 00                | Control/status 1                    | x                   | x     | x     | x     | x     | x     | x     | x     |
| 01                | Control/ status 2                   | x                   | x     | x     | x     | AF*2  | x     | AIE*3 | x     |
| 02                | Seconds (00-59)                     | OSF*4               | S40   | S20   | S10   | S8    | S4    | S2    | S1    |
| 03                | Minutes (00-59)                     | x                   | M40   | M20   | M10   | M8    | M4    | M2    | M1    |
| 04                | Hours (00-23)                       | x                   | x     | H20   | H10   | H8    | H4    | H2    | H1    |
| 05                | Dates (01-31)                       | x                   | x     | D20   | D10   | D8    | D4    | D2    | D1    |
| 06                | Days of the week (00-06)            | x                   | x     | x     | x     | x     | W4    | W2    | W1    |
| 07                | Months (01-12)                      | x                   | x     | x     | MO10  | MO8   | MO4   | MO2   | MO1   |
| 08                | Years (00-99)                       | Y80                 | Y40   | Y20   | Y10   | Y8    | Y4    | Y2    | Y1    |
| 09                | Alarm: Minutes (00-59)              | AE*5                | M40   | M20   | M10   | M8    | M4    | M2    | M1    |
| 0A                | Alarm: Hours (01-12)                | AE*5                | x     | H20   | H10   | H8    | H4    | H2    | H1    |
| 0B                | Alarm: Dates (01-31)                | AE*5                | x     | D20   | D10   | D8    | D4    | D2    | D1    |
| 0C                | Alarm: Weekday (00-06)              | AE*5                | x     | x     | x     | x     | W4    | W2    | W1    |
| 0D                | SQW control                         | SQWE                | x     | x     | x     | x     | x     | RS1   | RS0   |

Caution points:

- \*1 . PCF8563T-NF uses 8 bits for address. For excess 0FH address, PCF8563T-NF will not respond.
- \*2 . Alarm interrupt flag bits.
- \*3 . Alarm interrupt enable bits.
- \*4 . Oscillator fail indicates. Indicate clock integrity.
- \*5 . Alarm enable bit. Alarm will be active when related time is matching if AE = 0 .
- \*6 . All bits marked with " x " are not implemented.

## Control and status register

| Addr. (hex) | Description       | D7        | D6        | D5        | D4        | D3        | D2        | D1        | D0        |
|-------------|-------------------|-----------|-----------|-----------|-----------|-----------|-----------|-----------|-----------|
| 00          | Control/ status 1 | x         | x         | x         | x         | x         | x         | x         | x         |
|             | (default)         | 0         | Undefined | 0         | Undefined | 1         | Undefined | Undefined | Undefined |
| 01          | Control/ status 2 | x         | x         | x         | x         | AF        | x         | AIE       | x         |
|             | (default)         | Undefined | Undefined | Undefined | 0         | Undefined | Undefined | 0         | 0         |
| 0D          | SQW control       | SQWE      | x         | x         | x         | x         | x         | RS1       | RS0       |
|             | (default)         | 1         | Undefined | Undefined | Undefined | Undefined | Undefined | 0         | 0         |

### a) Alarm Interrupt

- AIE:** Alarm Interrupt Enable bit.

| AIE          | Data | Description              |         |
|--------------|------|--------------------------|---------|
| Read / Write | 0    | Alarm interrupt disabled | Default |
|              | 1    | Alarm interrupt enabled  |         |

- AF:** Alarm Flag

| AF    | Data | Description                  |
|-------|------|------------------------------|
| Read  | 0    | Alarm flag inactive          |
|       | 1    | Alarm flag active            |
| Write | 0    | Alarm flag is cleared        |
|       | 1    | Alarm flag remains unchanged |

### b) SQW control

- SQWE:** SQW output clock enable bit.

| SQWE         | Data | Description                                                         |         |
|--------------|------|---------------------------------------------------------------------|---------|
| Read / Write | 0    | the SQW output is inhibited and SQW output is set to high impedance |         |
|              | 1    | the SQW output is activated                                         | Default |

- RS1 RS0:** SQW output frequency select

| RS1, RS0     | Data | SQW output freq. (Hz) |         |
|--------------|------|-----------------------|---------|
| Read / Write | 00   | 32.768k               | Default |
|              | 01   | 1.024k                |         |
|              | 10   | 32                    |         |
|              | 11   | 1                     |         |

[illegible]

## 5. Alarm Register

### PCF8563T-S-TR:

| Addr. | Description    | D7        | D6        | D5        | D4        | D3        | D2        | D1        | D0        |
|-------|----------------|-----------|-----------|-----------|-----------|-----------|-----------|-----------|-----------|
| 09    | Alarm: Minutes | AE*1      | M40       | M20       | M10       | M8        | M4        | M2        | M1        |
|       | (default)      | Undefined | Undefined | Undefined | Undefined | Undefined | Undefined | Undefined | Undefined |
| 0A    | Alarm: Hours   | AE*2      | x         | H20       | H10       | H8        | H4        | H2        | H1        |
|       | (default)      | Undefined | 0         | Undefined | Undefined | Undefined | Undefined | Undefined | Undefined |
| 0B    | Alarm: Dates   | AE*3      | x         | D20       | D10       | D8        | D4        | D2        | D1        |
|       | (default)      | Undefined | 0         | Undefined | Undefined | Undefined | Undefined | Undefined | Undefined |
| 0C    | Alarm: Weekday | AE*4      | x         | x         | x         | x         | W4        | W2        | W1        |
|       | (default)      | Undefined | 0         | 0         | 0         | 0         | Undefined | Undefined | Undefined |

\*1 Note: Minute alarm enable bit. \*2 Note: Hour alarm enable bit. \*3 Note: Date alarm enable bit.

\*4 Note: Weekday alarm enable bit.

## Alarm Function

Related register

|    | Function          | Register definition |       |       |       |       |       |       |       |
|----|-------------------|---------------------|-------|-------|-------|-------|-------|-------|-------|
|    |                   | Bit 7               | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 |
| 01 | Control/ status 2 | x                   | x     | x     | x     | AF    | x     | AIE   | x     |
| 02 | Seconds           | OSF                 | S40   | S20   | S10   | S8    | S4    | S2    | S1    |
| 03 | Minutes           | x                   | M40   | M20   | M10   | M8    | M4    | M2    | M1    |
| 04 | Hours             | x                   | x     | H20   | H10   | H8    | H4    | H2    | H1    |
| 05 | Dates             | x                   | x     | D20   | D10   | D8    | D4    | D2    | D1    |
| 06 | Days of the week  | x                   | x     | x     | x     | x     | W4    | W2    | W1    |
| 09 | Alarm: Minutes    | AE                  | M40   | M20   | M10   | M8    | M4    | M2    | M1    |
| 0A | Alarm: Hours      | AE                  | x     | H20   | H10   | H8    | H4    | H2    | H1    |
| 0B | Alarm: Dates      | AE                  | x     | D20   | D10   | D8    | D4    | D2    | D1    |
| 0C | Alarm: Weekday    | AE                  | x     | x     | x     | x     | W4    | W2    | W1    |

When one or more of these registers are loaded with a valid minute , hour, day or weekday and its corresponding bit Alarm Enable (AE) is logic 0, then that information will be compared with the current minute , hour, day and weekday. When all enabled comparisons first match, the Alarm Flag (AF) is set. AF will remain set until cleared by software .

Once AF has been cleared it will only be set again when the time increments to match the alarm condition once more . Alarm registers which have their bit AE at logic 1 will be ignored.

## I<sup>2</sup>C Bus Interface

### 1. I<sup>2</sup>C Bus Protocol

#### a) Overview of I<sup>2</sup>C- BUS

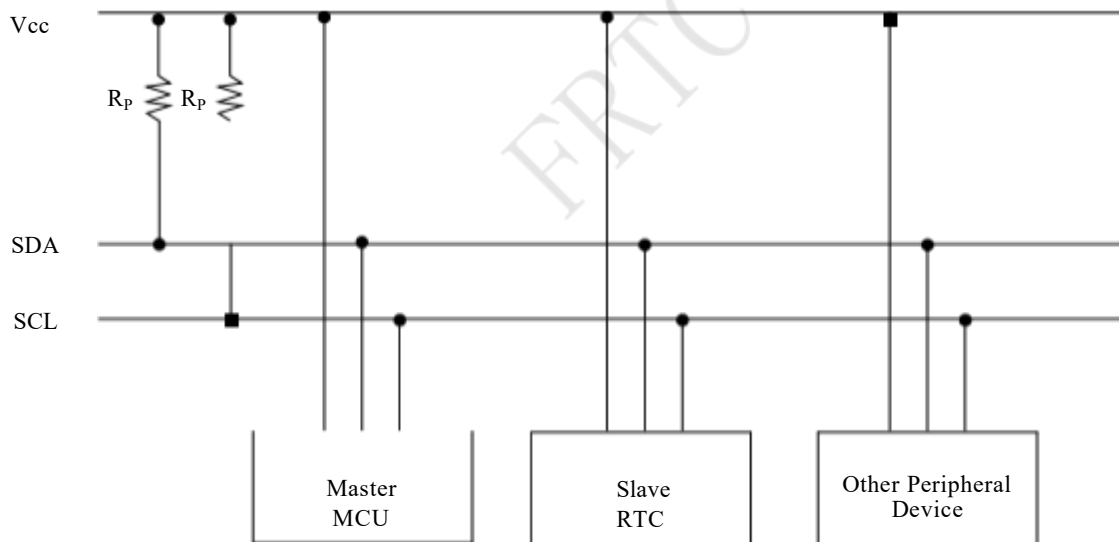
The I<sup>2</sup>C bus supports bi-directional communications via two signal lines: the SDA (data) line and SCL (clock) line. A combination of these two signals is used to transmit and receive communication start/stop signals, data signals, acknowledge signals, and so on.

Both the SCL and SDA signals are held at high level whenever communications are not being performed. The starting and stopping of communications is controlled at the rising edge or falling edge of SDA while SCL is at high level. During data transfers, data changes that occur on the SDA line are performed while the SCL line is at low level, and on the receiving side the data is captured while the SCL line is at high level. In either case, the data is transferred via the SCL line at a rate of one bit per clock pulse. The I<sup>2</sup>C bus device does not include a chip select pin such as is found in ordinary logic devices. Instead of using a chip select pin, slave addresses are allocated to each device and the receiving device responds to communications only when its slave address matches the slave address in the received data.

#### b) System Configuration

All ports connected to the I<sup>2</sup>C bus must be either open drain or open collector ports in order to enable AND connections to multiple devices.

SCL and SDA are both connected to the VDD line via a pull-up resistance. Consequently, SCL and SDA are both held at high level when the bus is released (when communication is not being performed).



Note: When there is only one master, the MCU is ready for driving SCL to "H" and R<sub>p</sub> of SCL may not required.

Fig.1 System configuration

## c) Starting and Stopping I<sup>2</sup>C Bus Communications

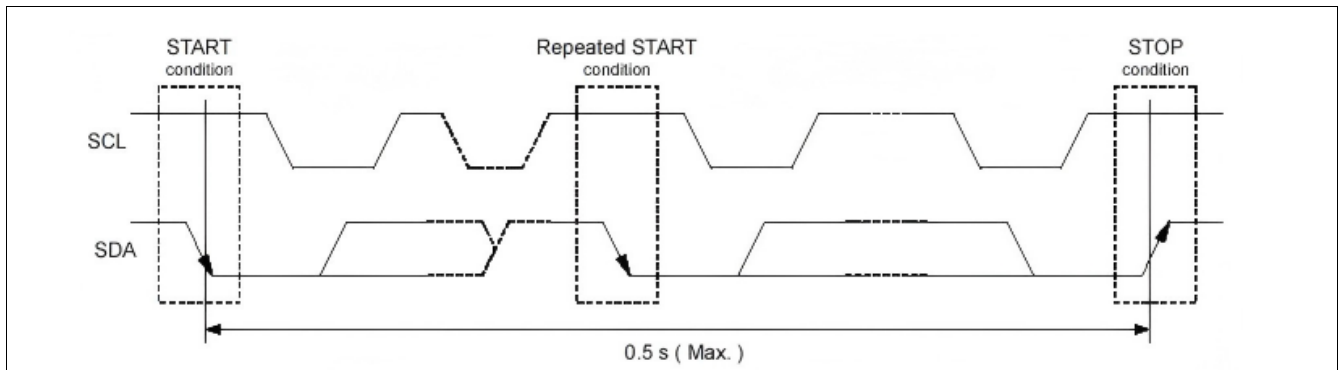


Fig.2 Starting and stopping on I<sup>2</sup>C bus

START condition ,repeated START condition ,and STOP condition

- **START condition**  
SDA level changes from high to low while SCL is at high level
- **STOP condition**  
SDA level changes from low to high while SCL is at high level
- **Repeated START condition (RESTART condition)**

In some cases, the START condition occurs between a previous START condition and the next STOP condition, in which case the second START condition is distinguished as a RESTART condition. Since the required status is the same as for the START condition, the SDA level changes from high to low while SCL is at high level.

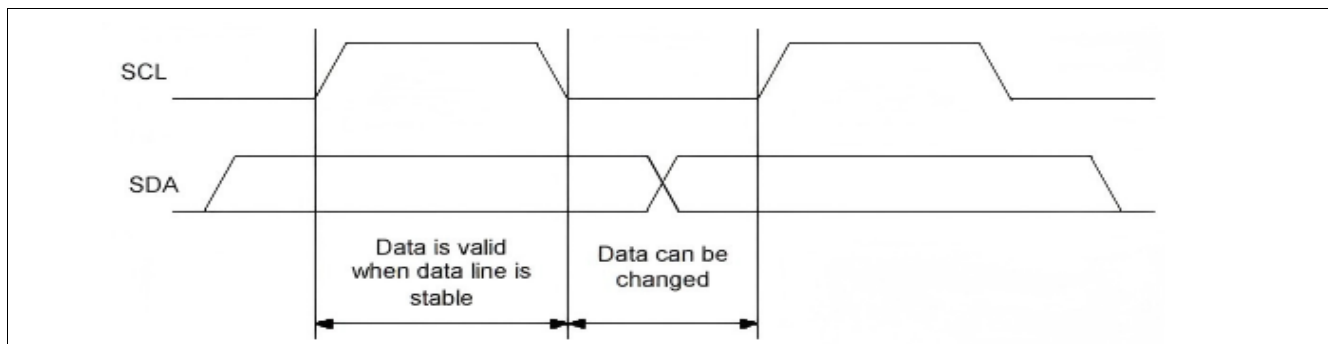
## d) Data Transfers and Acknowledge Responses during I<sup>2</sup>C-BUS Communication

### • Data transfers

Data transfers are performed in 8-bit (1 byte) units once the START condition has occurred. There is no limit on the amount (bytes) of data that are transferred between the START condition and STOP condition.

The address auto increment function operates during both write and read operations.

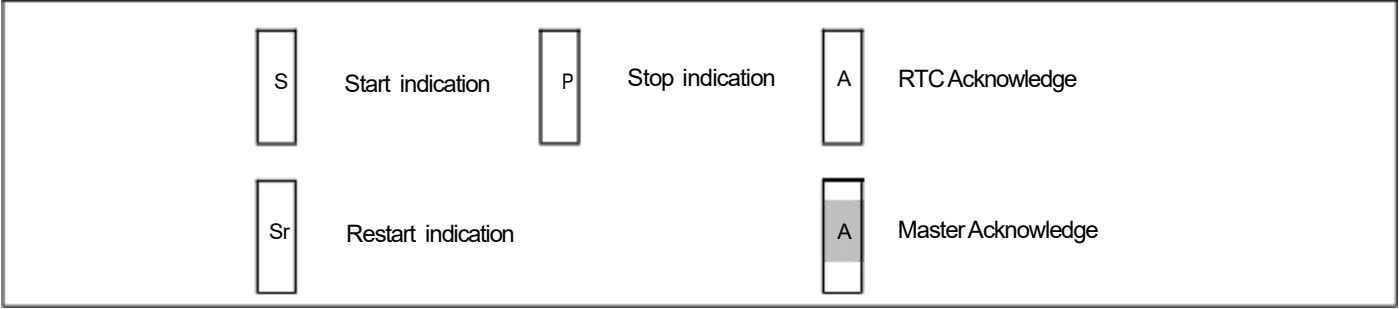
Updating of data on the transmitter (transmitting side)'s SDA line is performed while the SCL line is at low level. The receiver (receiving side) captures data while the SCL line is at high level.



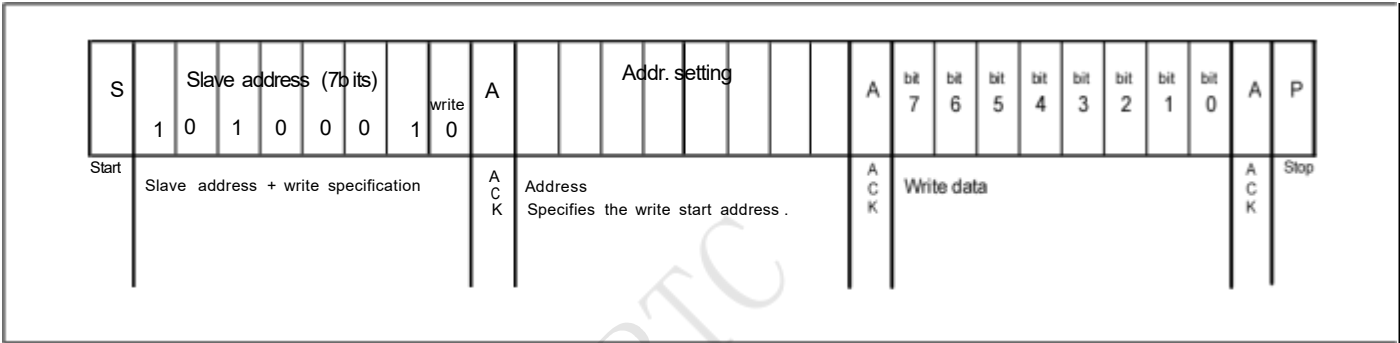
\*Note with caution that if the SDA data is changed while the SCL line is at high level, it will be treated as a START, RESTART, or STOP condition.

| Operation | Transfer data | Slave address |       |       |       |       |       |       | R / W bit  |
|-----------|---------------|---------------|-------|-------|-------|-------|-------|-------|------------|
|           |               | bit 7         | bit 6 | bit 5 | bit 4 | bit 3 | bit 2 | bit 1 | bit 0      |
| Read      | A3 h          | 1             | 0     | 1     | 0     | 0     | 0     | 1     | 1 (= Read) |
| Write     | A2 h          |               |       |       |       |       |       |       | 0(= Write) |

2. I<sup>2</sup>C Bus's Basic Transfer Format

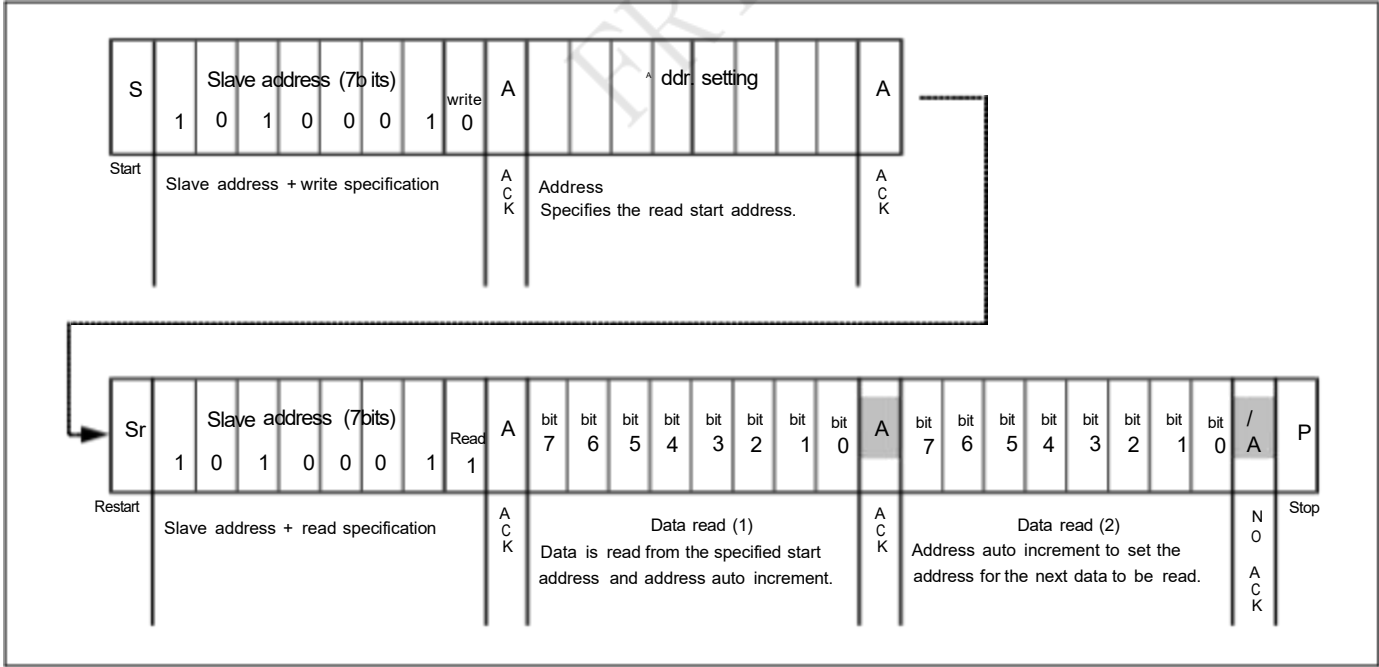


a) Write via I<sup>2</sup>C bus

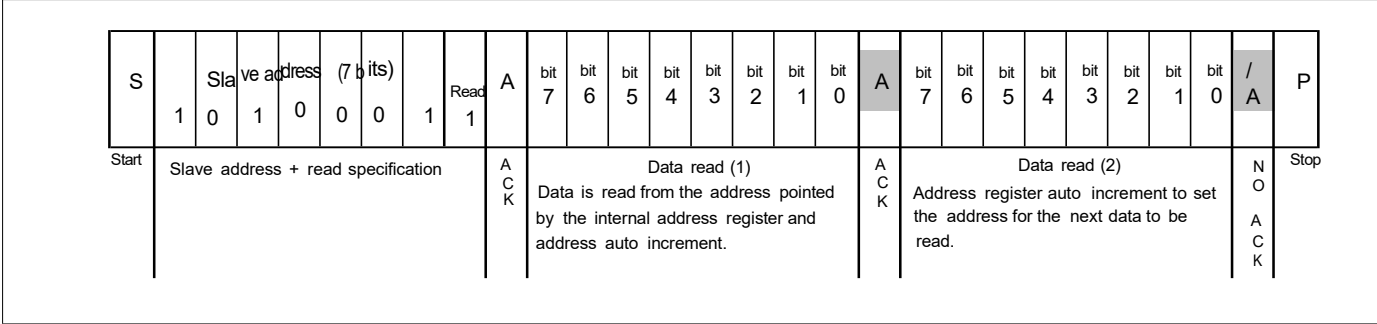


b) Read via I<sup>2</sup>C bus

• Standard read



Simplified read



- Note:**
- 1. The above steps are an example of transfers of one or two bytes only. There is no limit to the number of bytes transferred during actual communications .
  - 2 . 49 H , 4AH are used as test mode address. Customer should not use the addresses.

Absolute Maximum Ratings

|                                               |                          |
|-----------------------------------------------|--------------------------|
| Storage Temperature                           | -65oCto +150oC           |
| Ambient Temperaturewith PowerApplied          | -40oCto +125oC           |
| Supply Voltage to Ground Potential (VcctoGND) | -0.3Vto +6.5V            |
| DC Input (All Other Inputs exceptVcc& GND)    | -0.3Vto (Vcc+0.3V)       |
| DC OutputVoltage (SDA,/INTA,/INTB pins)       | -0.3Vto +6.5V            |
| Power Dissipation                             | 320mW(Depend on package) |

**Note:**  
Stresses greater than those listed under MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

Recommended Operating Conditions

| Symbol | Description           | MIN     | TYP | MAX     | Unit |
|--------|-----------------------|---------|-----|---------|------|
| Vcc    | Power voltage         | 1.7     | -   | 5.5     | V    |
| VIH    | Input high level      | 0.7 Vcc | -   | Vcc+0.3 |      |
| VIL    | Input low level       | -0.3    | -   | 0.3 Vcc |      |
| TA     | Operating temperature | -40     | -   | 125     | °C   |

## DC Electrical Characteristics

Unless otherwise specified, GND = 0V, V<sub>CC</sub> = 1.7 ~ 5.5 V, T<sub>A</sub> = -40 °C to +125 °C, f<sub>osc</sub> = 32.768kHz.

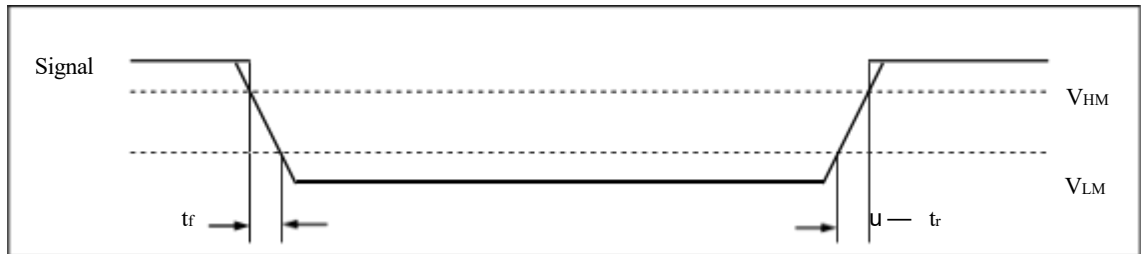
| Symbol           | Description                             | Pin             | Conditions                                                                                       |                           | MIN                | TYP | MAX                | Unit |
|------------------|-----------------------------------------|-----------------|--------------------------------------------------------------------------------------------------|---------------------------|--------------------|-----|--------------------|------|
| V <sub>CC</sub>  | Supply voltage                          | V <sub>CC</sub> | Interface inactive. T <sub>A</sub> = 25 °C 1)                                                    |                           | 1.5                | -   | 5.5                | V    |
|                  |                                         |                 | Interface active. f <sub>SCL</sub> = 400kHz 1)                                                   |                           | 1.7                | -   | 5.5                |      |
|                  | Supply voltage for clock data integrity | V <sub>CC</sub> | -                                                                                                |                           | 1.5                | -   | 5.5                |      |
| I <sub>CC</sub>  | Supply current                          | V <sub>CC</sub> | Interface active                                                                                 | f <sub>SCL</sub> = 400kHz | -                  | -   | 25                 | μA   |
|                  |                                         |                 |                                                                                                  | f <sub>SCL</sub> = 100kHz | -                  | -   | 15                 |      |
|                  |                                         |                 | Interface inactive (f <sub>SCL</sub> = 0 Hz), pin 7 disabled T <sub>A</sub> = -40~125 °C         | V <sub>CC</sub> = 5.0V    | -                  | 450 | 900                | nA   |
|                  |                                         |                 |                                                                                                  | V <sub>CC</sub> = 3.0V    | -                  | 400 | 800                |      |
|                  |                                         |                 | Interface inactive (f <sub>SCL</sub> = 0 Hz), pin 7 enabled at 32kHz T <sub>A</sub> = -40~125 °C | V <sub>CC</sub> = 5.0V    | -                  | 650 | 900                | nA   |
|                  |                                         |                 |                                                                                                  | V <sub>CC</sub> = 3.0V    | -                  | 600 | 850                |      |
| V <sub>IL1</sub> | Low-level input voltage                 | SCL             | -                                                                                                |                           | 0                  | -   | 0.3V <sub>CC</sub> | V    |
| V <sub>IH1</sub> | High-level input voltage                | SCL             | -                                                                                                |                           | 0.7V <sub>CC</sub> | -   | V <sub>CC</sub>    |      |
| I <sub>OL</sub>  | Low-level output voltage                | SDA             | V <sub>OL</sub> = 0.4V, V <sub>CC</sub> = 5V                                                     |                           | -3                 | -   | -                  | mA   |
|                  |                                         | /INT, SQW       | V <sub>OL</sub> = 0.4V, V <sub>CC</sub> = 5V                                                     |                           | -1                 | -   | -                  |      |
| I <sub>IL</sub>  | Input leakage current                   | SCL             | -                                                                                                |                           | -                  | -   | ±1                 | μA   |
| I <sub>oz</sub>  | Output current when OFF                 | -               | -                                                                                                |                           | -                  | -   | ±1                 | μA   |

Note:

1) For reliable oscillator start-up at power-up: V<sub>CC(min)power-up</sub> = V<sub>CC(min)</sub> + 0.3 V

## AC Electrical Characteristics

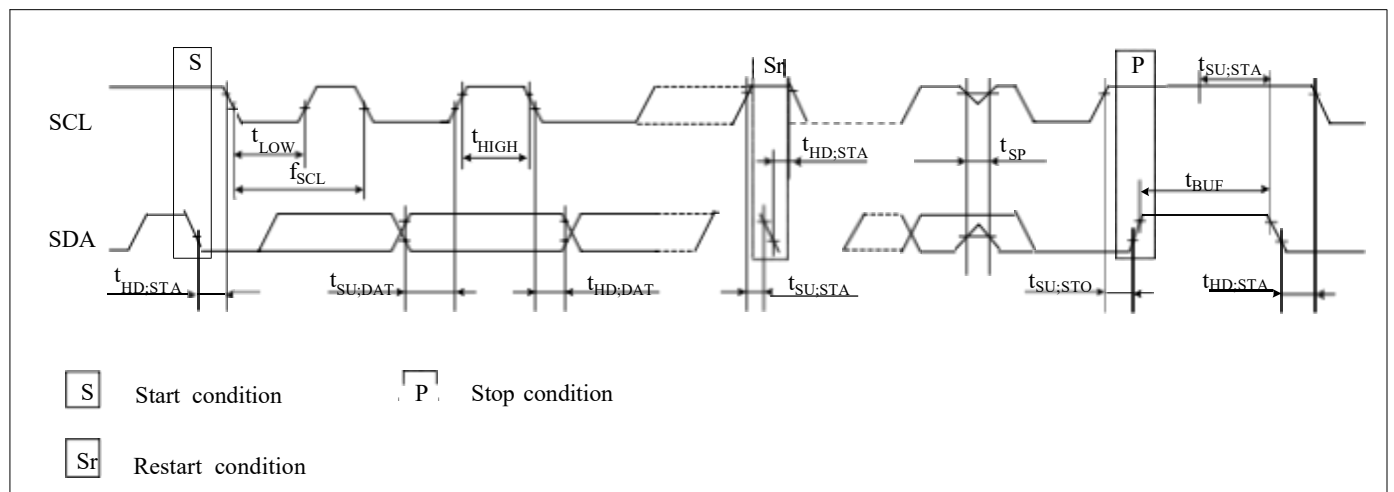
| Symbol   | Description                               | Value        | Unit |
|----------|-------------------------------------------|--------------|------|
| $V_{HM}$ | Rising and falling threshold voltage high | $0.8 V_{CC}$ | V    |
| $V_{HL}$ | Rising and falling threshold voltage low  | $0.2 V_{CC}$ | V    |



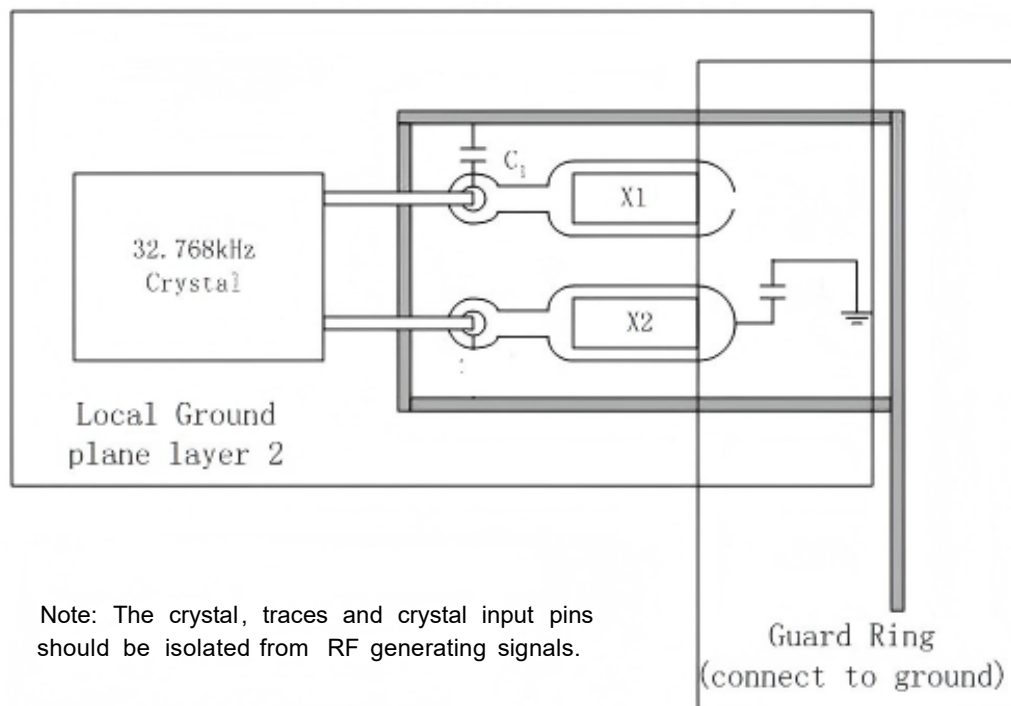
Over the operating range

| Symbol        | Description                                      | MIN | TYP | MAX | Unit    |
|---------------|--------------------------------------------------|-----|-----|-----|---------|
| $f_{SCL}$     | SCL clock frequency                              | -   | -   | 400 | kHz     |
| $t_{SU;STA}$  | START condition set-up time                      | 0.6 | -   | -   | $\mu s$ |
| $t_{HD;STA}$  | START condition hold time                        | 0.6 | -   | -   | $\mu s$ |
| $t_{SU;DAT}$  | Data set-up time (RTC read/write in Fast mode)   | 100 | -   | -   | ns      |
| $t_{HD;DAT1}$ | Data hold time (RTC write)                       | 35  | -   | -   | ns      |
| $t_{HD;DAT2}$ | Data hold time (RTC read)                        | 0   | -   | -   | $\mu s$ |
| $t_{SU;STO}$  | STOP condition setup time                        | 0.6 | -   | -   | $\mu s$ |
| $t_{BUF}$     | Bus idle time between a START and STOP condition | 1.3 | -   | -   | $\mu s$ |
| $t_{LOW}$     | When SCL = "L"                                   | 1.3 | -   | -   | $\mu s$ |
| $t_{HIGH}$    | When SCL = "H"                                   | 0.6 | -   | -   | $\mu s$ |
| $t_r$         | Rise time for SCL and SDA                        | -   | -   | 0.3 | $\mu s$ |
| $t_f$         | Fall time for SCL and SDA                        | -   | -   | 0.3 | $\mu s$ |
| $t_{SP}^*$    | Allowable spike time on bus                      | -   | -   | 50  | ns      |
| $C_B$         | Capacitance load for each bus line               | -   | -   | 400 | pF      |

\* **Note:** Only reference for design.



## Recommended Layout for Crystal



## Built-in Capacitors Specifications and Recommended External Capacitors

| Symbol | Parameter                                               |           | TYP | Unit |
|--------|---------------------------------------------------------|-----------|-----|------|
| CD     | Build-in capacitors                                     | X1 to GND | 0   | pF   |
| CG     |                                                         | X2 to GND | 23  | pF   |
| C1     | Recommended External capacitors for crystal CL= 12.5 pF | X1 to GND | 22  | pF   |
| C2     |                                                         | X2 to GND | 0   | pF   |
| C1     | Recommended External capacitors for crystal CL= 6 pF    | X1 to GND | 7   | pF   |
| C2     |                                                         | X2 to GND | 0   | pF   |

Note: The frequency of crystal can be optimized by external capacitor C1 and C2 , for frequency= 32 . 768 Hz, C1 and C2 should meet the equation as below:

$$C_{par} + \frac{[(C1+CG) \cdot (C2+CD)]}{[(C1+CG) + (C2+CD)]} = CL$$

C<sub>par</sub> is all parasitical capacitor between X1 and X2 .

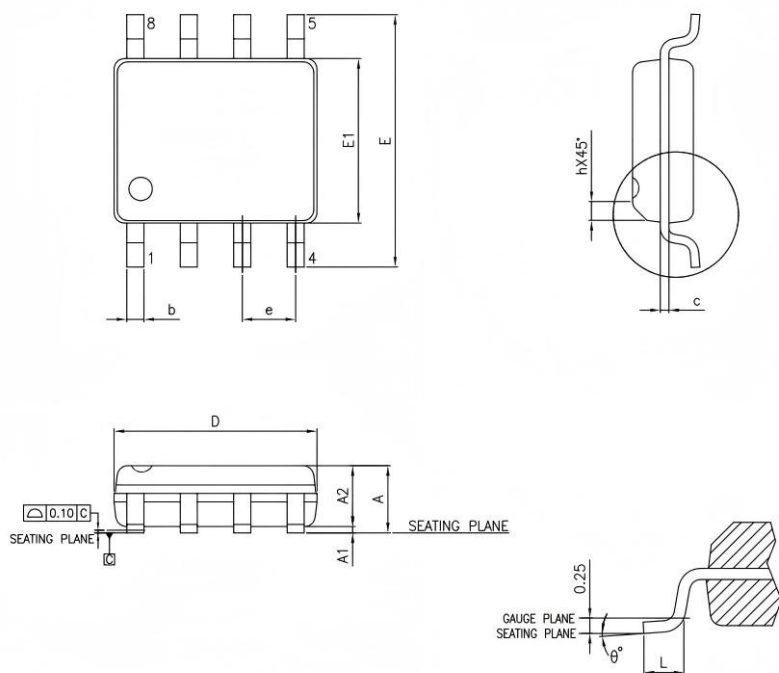
CL is crystal's load capacitance.

## Crystal Specifications

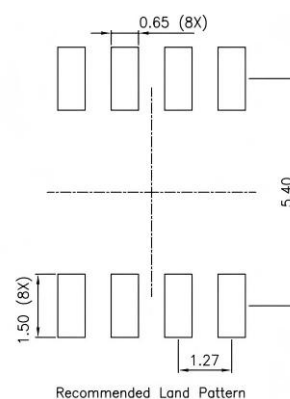
| Symbol         | Parameter         | MIN | TYP    | MAX | Unit |
|----------------|-------------------|-----|--------|-----|------|
| f <sub>o</sub> | Nominal Frequency | -   | 32.768 | -   | kHz  |
| ESR            | Series Resistance | -   | -      | 70  | kΩ   |
| CL             | Load Capacitance  | -   | 6/12.5 | -   | pF   |

## Package Information

### PCF8563T-NF (SOP8) package



| SYMBOLS | MIN.     | NOM. | MAX. |
|---------|----------|------|------|
| A       | —        | —    | 1.75 |
| A1      | 0.10     | —    | 0.25 |
| A2      | 1.25     | —    | —    |
| b       | 0.31     | —    | 0.51 |
| c       | 0.10     | —    | 0.25 |
| D       | 4.80     | 4.90 | 5.00 |
| E       | 5.80     | 6.00 | 6.20 |
| E1      | 3.80     | 3.90 | 4.00 |
| e       | 1.27 BSC |      |      |
| L       | 0.40     | —    | 1.27 |
| h       | 0.25     | —    | 0.50 |
| θ°      | 0        | —    | 8    |

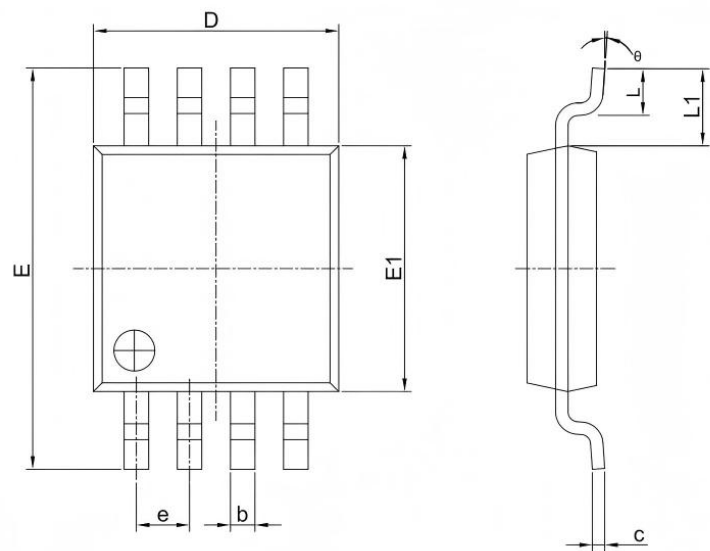


#### Note:

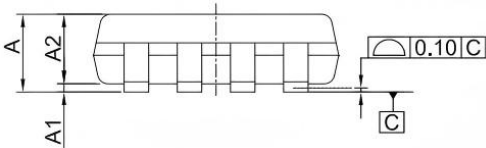
- 1.All dimensions are in mm. Angels in degrees.
- 2.Dimensions exclude burrs, mold flash or protrusions.
- 3.Refer Jedec MS-012
4. Recommended land pattern is for reference only.

SOP08 POD Rev.0

PCF8563TS-NF (MSOP-8) package



| PKG DIMENSIONS(MM) |          |      |
|--------------------|----------|------|
| SYMBOL             | Min.     | Max. |
| A                  | --       | 1.10 |
| A1                 | 0.00     | 0.15 |
| A2                 | 0.75     | 0.95 |
| b                  | 0.22     | 0.38 |
| c                  | 0.08     | 0.23 |
| D                  | 2.80     | 3.20 |
| E                  | 4.65     | 5.15 |
| E1                 | 2.80     | 3.20 |
| e                  | 0.65 BSC |      |
| L                  | 0.40     | 0.80 |
| L1                 | 0.95 REF |      |
| θ                  | 0°       | 8°   |



- Note:
- 1.All dimensions are in mm. Angels in degrees.
  - 2.Refer Jedec MO-187
  - 3.Dimensions exclude burrs, mold flash or protrusions.