CMF4N90

900V N-Channel MOSFET

General Description

This Power MOSFET is produced using Cmos's advanced planar stripe DMOS technology. This advanced technology has been especially tailored to minimize on-state resistance, provide superior switching performance, and withstand high energy pulse in the avalanche and commutation mode. These devices are well suited for high efficiency switched mode power supplies, active power factor correction based on half bridge topology

Product Summary

BVDSS	RDSON	ID
900V	4Ω	4A

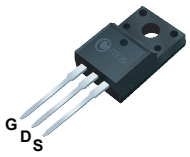
Applications

- Switching application
- Switch mode power supply (SMPS)
- AC adaptors

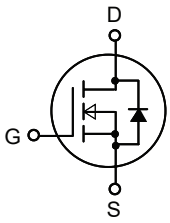
Features

- R_{DS}(ON)<4Ω @ V_{GS}=10V
- 100% avalanche tested
- RoHS Compliant
- Low gate charge
- Improved dv/dt capability

TO-220F Pin Configuration



TO-220F
(CMF4N90)



Absolute Maximum Ratings (Tc=25℃ unless otherwise noted)

Symbol	Parameter	Rating	Units
V_{DSS}	Drain-Source Voltage	900	V
I_D	Drain Current - Continuous (T_C = 25℃)	4	A
	- Continuous (T_C = 100℃)	2.5	A
I_{DM}	Drain Current - Pulsed	12	A
V_{GSS}	Gate-Source Voltage	±30	V
E_{AS}	Single Pulsed Avalanche Energy [1]	70	mJ
P_D	Power Dissipation (T_C = 25℃)	50	W
T_J, T_{STG}	Operating and Storage Temperature Range	-55 to +150	℃

Thermal Characteristics

Symbol	Parameter	Rating	Units
$R_{\theta JC}$	Thermal Resistance, Junction-to-Case	3.3	℃/W
$R_{\theta JA}$	Thermal Resistance, Junction-to-Ambient	65	℃/W

Electrical Characteristic (Tc=25℃ unless otherwise noted)

Symbol	Parameter	Test Conditions	Min	Typ	Max	Units
Off Characteristics						
BV_{DSS}	Drain-Source Breakdown Voltage	V_{GS} = 0 V, I_D = 250 μA	900	--	--	V
I_{DSS}	Zero Gate Voltage Drain Current	V_{DS} = 900 V, V_{GS} = 0 V	--	--	1	μA
		V_{GS} =720V, T_C = 125℃	--	--	100	nA
I_{GSSF}	Gate-Body Leakage Current, Forward	V_{GS} = 30 V, V_{DS} = 0 V	--	--	100	nA
I_{GSSR}	Gate-Body Leakage Current, Reverse	V_{GS} = -30 V, V_{DS} = 0 V	--	--	-100	nA
On Characteristics						
$V_{GS(th)}$	Gate Threshold Voltage	V_{DS} = V_{GS} , I_D = 250 μA	3	--	5	V
$R_{DS(on)}$	Static Drain-Source on-Resistance	V_{GS} = 10 V, I_D = 2A	--	3.6	4	Ω
g_{FS}	Forward Transconductance	V_{DS} = 10V, I_D = 2A	--	4	--	S
R_g	Gate Resistance	V_{DS}=0V , V_{GS}=0V , f=1MHz	--	2.3	--	Ω
Dynamic Characteristics						
C_{iss}	Input Capacitance	V_{DS} =25V, V_{GS} = 0 V f = 1.0 MHz	--	800	--	pF
C_{oss}	Output Capacitance		--	50	--	pF
C_{rss}	Reverse Transfer Capacitance		--	5.5	--	pF
Switching Characteristics						
$t_{d(on)}$	Turn-On Delay Time	V_{DS} = 450 V, I_D = 4A R_G = 25Ω ,V_{GS} = 10 V	--	22	--	ns
t_r	Turn-On Rise Time		--	45	--	ns
$t_{d(off)}$	Turn-Off Delay Time		--	43	--	ns
t_f	Turn-Off Fall Time		--	40	--	ns
Q_g	Total Gate Charge	V_{DS} = 720 V, I_D = 4A V_{GS} = 10 V	--	18.5	--	nC
Q_{gs}	Gate-Source Charge		--	4.5	--	nC
Q_{gd}	Gate-Drain Charge		--	8	--	nC
Drain-Source Diode Characteristics and Maximum Ratings						
I_S	Maximum Continuous Drain-Source Diode Forward Current		--	--	4	A
I_{SM}	Maximum Pulsed Drain-Source Diode Forward Current		--	--	12	A
V_{SD}	Drain-Source Diode Forward Voltage	V_{GS} = 0 V, I_S = 4A	--	--	1.2	V
t_{rr}	Reverse Recovery Time	I_F = 4A ,T_j = 25℃,V_{DS}=100V dI_F / dt = 100 A/μs	--	196	--	ns
Q_{rr}	Reverse Recovery Charge		--	4.05	--	μC

Note:
1. L=5mH, I_{AS}=5.5A, V_{DD}=100V, R_G=25Ω, Starting T_J=25℃

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Cmos assumes no liability for customers' product design or applications.
Cmos reserver the right to improve product design ,functions and reliability wihtout notice.

Typical Characteristics

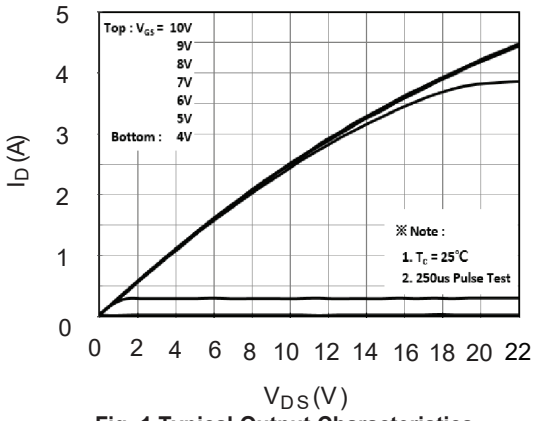

Fig. 1 Typical Output Characteristics

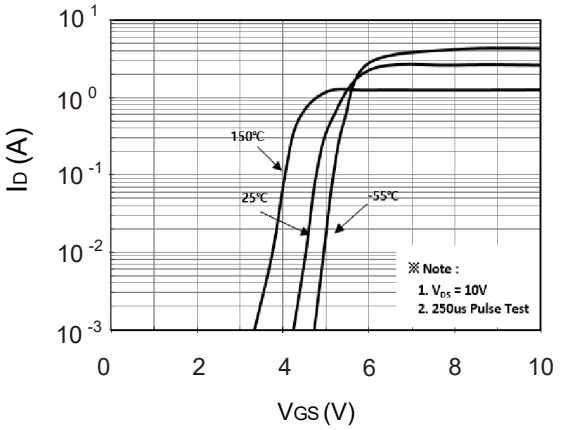

Fig. 2 Typical Transfer Characteristics

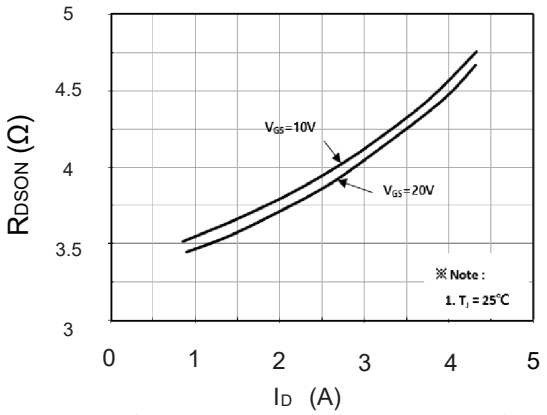

Fig.3 On-Resistance Variation with Drain Current and Gate Voltage

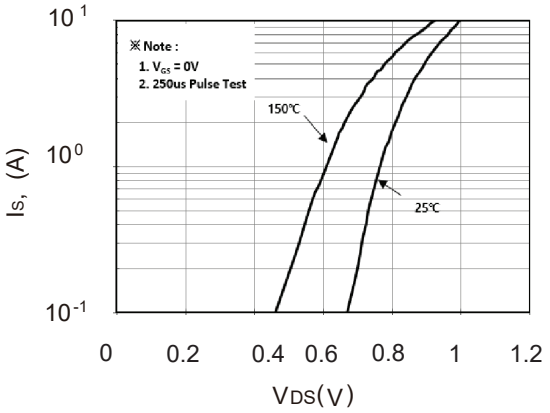

Fig. 4 Body Diode Forward Voltage Variation with Source Current

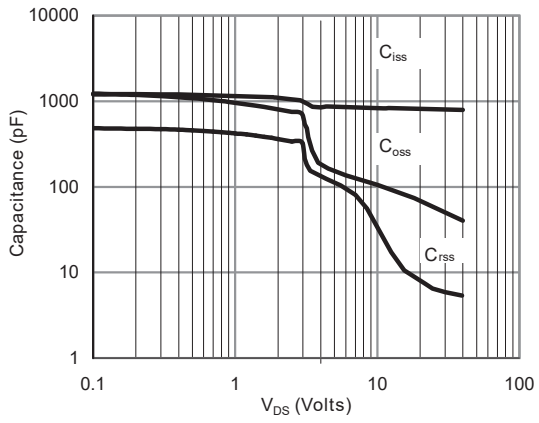

Fig. 5 Typical Capacitance Characteristics

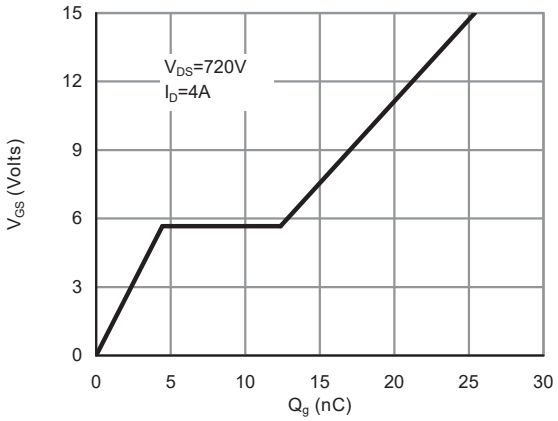

Fig. 6 Typical Total Gate Charge Characteristics

Typical Characteristics

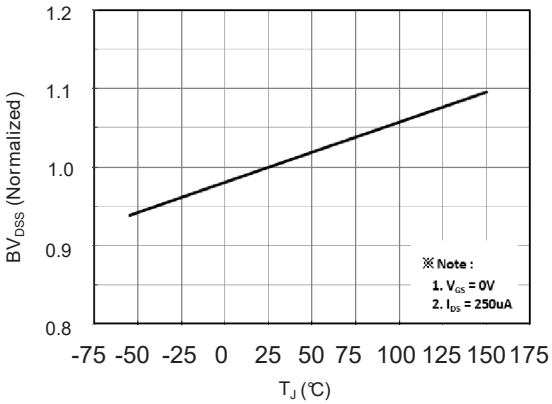

Fig. 7 Breakdown Voltage Variation vs. Temperature

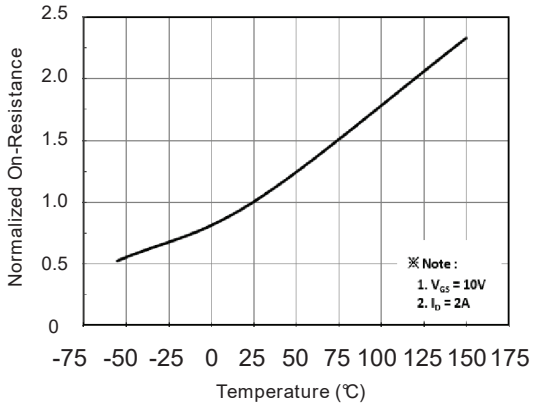

Fig. 8 On-Resistance Variation vs. Temperature

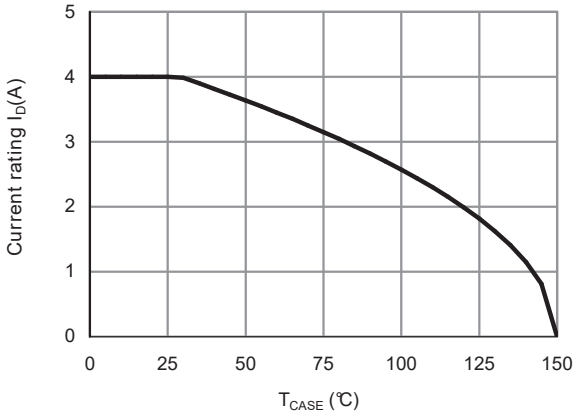

Figure 9: Current De-rating (Note B)

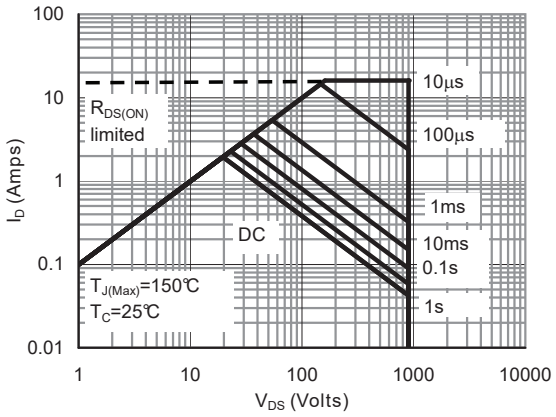

Figure 10: Maximum Forward Biased Safe Operating Area for AOTF4N90 (Note F)

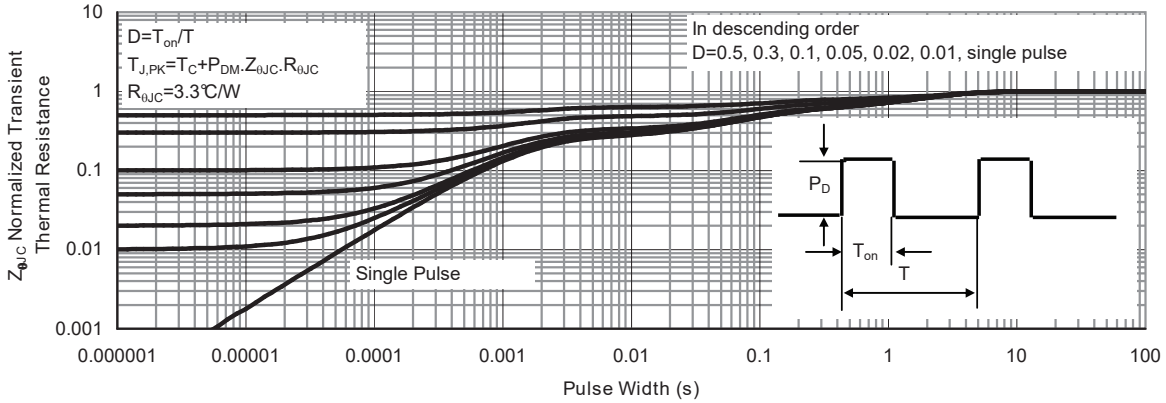

Figure 11: Normalized Maximum Transient Thermal Impedance for AOTF4N90 (Note F)