

Product Overview

The SP201AW1 devices are high reliability dual-channel digital isolators. The SP201AW1 device is safety certified by UL1577 support 5kVrms insulation withstand voltage, while providing high electromagnetic immunity and low emissions at low power consumption. The data rate of the SP201AW1 is up to 100Mbps, and the common-mode transient immunity (CMTI) is up to 250kV/us. The SP201AW1 device provides digital channel direction configuration and the default output level configuration when the input power is lost. Wide supply voltage of the SP201AW1 device support connection to most digital interface directly, easy to do the level shift. High system level EMC performance enhance reliability and stability of use.

Key Features

- Up to 5000V_{rms} Insulation voltage
- Data rate: DC to 100Mbps
- Power supply voltage: 2.5V to 5.5V
- High CMTI: 250kV/us
- Chip level ESD: HBM: ±8kV
- Robust EMC Reinforced Dual-Channel Digital Isolators for SOW8 wide body
- Default output high level or low level option
- Isolation surge voltage: >10kV
- Low power consumption: 1.5mA/ch (1 Mbps)
- Low propagation delay: <18ns
- Operation temperature: -55°C~125°C
- RoHS-compliant packages:
SOW8 wide body

Safety Regulatory Approvals

- UL recognition: up to 5000V_{rms} for 1 minute per UL1577
- CQC certification per GB4943.1
- CSA component notice 5A
- DIN EN IEC 60747-17 (VDE 0884-17)

Applications

- Industrial automation system
- Isolated SPI, RS232, RS485
- General-purpose multichannel isolation
- Motor control

Device Information

Part Number	Package	Body Size
SP201AW1-DSWVR	SOW8	5.85mm × 7.50mm

Functional Block Diagrams

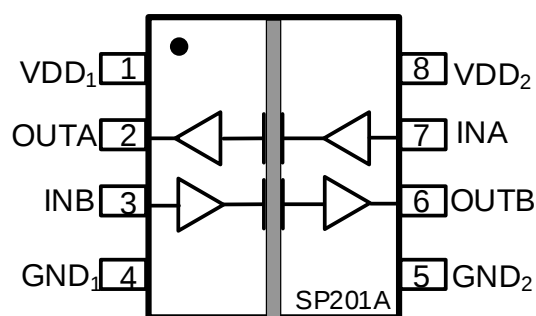


Figure 1. SP201AW1 SOW8 Block Diagram

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1. Pin Configuration and Functions

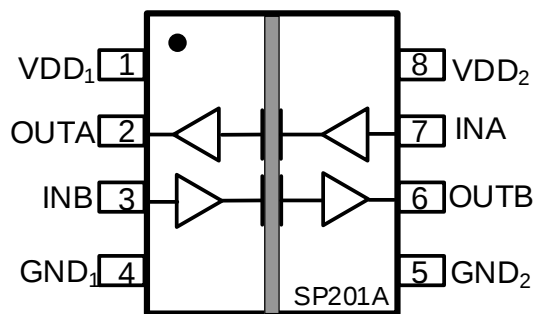


Figure 1.1 SP201AW1 SOW8 Package

Table1.1 SP201AW1 SOW8 Pin Configuration and Description

SP201A W1 SOW8 PIN NO.	SYMBOL	FUNCTION
1	VDD1	Power Supply for Isolator Side 1
7	INA	Logic Input A
3	INB	Logic Input B
4	GND1	Ground 1, the ground reference for Isolator Side 1
5	GND2	Ground 2, the ground reference for Isolator Side 2
6	OUTB	Logic Output B
2	OUTA	Logic Output A
8	VDD2	Power Supply for Isolator Side 2

2. Absolute Maximum Ratings

Parameters	Symbol	Min	Typ	Max	Unit	Comments
Power Supply Voltage	VDD1, VDD2	-0.5		6.5	V	
Maximum Input Voltage	V _{INA} , V _{INB}	-0.4		VDD+0.4	V	The maximum voltage must not exceed 6.5V
Maximum Output Voltage	V _{OUTA} , V _{OUTB}	-0.4		VDD+0.4	V	The maximum voltage must not exceed 6.5V
Maximum Input/Output Pulse Voltage	V _{INA} , V _{INB} , V _{OUTA} , V _{OUTB}	-0.8		VDD+0.8	V	Pulse width should be less than 100ns, and the duty cycle should be less than 10%
Output current	I _o	-15		15	mA	
Operating Temperature	T _{opr}	-55		125	°C	
Junction Temperature	T _j			150	°C	
Storage Temperature	T _{stg}	-65		150	°C	

- (1) Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under Recommended Operating conditions. Exposure to Absolute Maximum Rated conditions for extended periods may affect device reliability.
- (2) Power supply voltage and input/output voltage are respect to the local ground terminal (GND1 or GND2) voltage values.

3. ESD Ratings

Parameters	Ratings	Value	Unit
Electrostatic discharge (ESD)	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001 ⁽²⁾	±8000	V
	Charged device model (CDM), per JEDEC specification JESD22-C101 ⁽³⁾	±2000	V

- (1) Though this device features proprietary protection circuitry, proper ESD precautions should be considered to avoid performance degradation of damage due to high energy ESD event. Charged devices and circuit boards may discharge without detection.
- (2) Safe manufacturing requires 500-V HBM and standard ESD precautions, per JEDEC document JEP155.
- (3) Safe manufacturing requires 250-V CDM and standard ESD precautions, per JEDEC document JEP157.

4. Recommended Operating Conditions

Parameters	Symbol	min	typ	max	unit
Power Supply Voltage	VDD1, VDD2	2.5		5.5	V
Operating Temperature	T _{opr}	-55		125	°C

High Level Input Voltage	V _{IH}	0.7*VDD			V
Low Level Input Voltage	V _{IL}			0.3*VDD	V
Data rate	DR			100	Mbps

5. Thermal Characteristics

Parameters	Symbol	SOW8	Unit
IC Junction-to-Air Thermal Resistance	R _{θJA}	84.3	°C/W
Junction-to-case (top) thermal resistance	R _{θJC (top)}	36.3	°C/W
Junction-to-board thermal resistance	R _{θJB}	47.0	°C/W
Junction-to-top characterization parameter	Ψ _{JT}	9.6	°C/W
Junction-to-board characterization parameter	Ψ _{JB}	29.2	°C/W

6. Specifications

6.1. Electrical Characteristics

(VDD1=2.5V~5.5V, VDD2=2.5V~5.5V, Ta=-55°C to 125°C. Unless otherwise noted, Typical values are at VDD1 = 5V, VDD2 = 5V, Ta = 25°C)

Parameters	Symbol	Min	Typ	Max	Unit	Comments
Power on Reset	VDD _{POR}	2	2.2	2.4	V	POR threshold as during power-up
	VDD _{HYS}		0.1		V	POR threshold Hysteresis
Rising input switching threshold	V _{IT+}		0.6*VDD	0.7*VDD	V	
Falling input switching threshold	V _{IT-}	0.3*VDD	0.4*VDD		V	
Input threshold voltage hysteresis	V _{I(HYS)}		0.2*VDD		V	
High Level Output Voltage	V _{OH}	VDD-0.4			V	I _{OH} ≤ 4mA
Low Level Output Voltage	V _{OL}			0.4	V	I _{OL} ≤ 4mA
Output Impedance	R _{out}		50		ohm	
Input Pull high or low Current	I _{pull}		5	10	μA	
Start Up Time after POR	tr _{bs}		22	32	μs	
Common Mode Transient Immunity	CMTI	±200	±250		kV/μs	See Figure 6.6

6.2. Supply Current Characteristics – 5V Supply

(VDD1=5V± 10%, VDD2=5V± 10%, Ta=-55°C to 125°C. Unless otherwise noted, Typical values are at **VDD1 = 5V, VDD2 = 5V**, Ta = 25°C)

Parameters	Symbol	Min	Typ	Max	Unit	Comments
Supply current	SP201AW1					
	I _{DD1} (Q0)		1.55	2.12	mA	All Input at supply for SP201AW1
	I _{DD2} (Q0)		1.55	2.12	mA	
	I _{DD1} (Q1)		2.88	3.83	mA	All Input 0V at supply for SP201AW1
	I _{DD2} (Q1)		2.88	3.83	mA	
	I _{DD1} (1M)		2.28	2.98	mA	All Input with 1Mbps, C _L =15pF
	I _{DD2} (1M)		2.28	2.98	mA	
	I _{DD1} (10M)		2.84	3.77	mA	All Input with 10Mbps, C _L =15pF
	I _{DD2} (10M)		2.84	3.77	mA	
	I _{DD1} (100M)		8.29	10.94	mA	All Input with 100Mbps, C _L = 15pF
	I _{DD2} (100M)		8.29	10.94	mA	

6.3. Supply Current Characteristics –3.3V Supply

(VDD1=3.3V± 10%, VDD2=3.3V± 10%, Ta=-55°C to 125°C. Unless otherwise noted, Typical values are at **VDD1 = 3.3V, VDD2 = 3.3V, Ta = 25°C**)

Parameters	Symbol	Min	Typ	Max	Unit	Comments
Supply current	SP201AW1					
	I _{DD1} (Q0)		1.50	1.98	mA	All Input at supply for SP201AW1
	I _{DD2} (Q0)		1.50	1.98	mA	
	I _{DD1} (Q1)		2.82	3.78	mA	All Input 0V at supply for SP201AW1
	I _{DD2} (Q1)		2.82	3.78	mA	
	I _{DD1} (1M)		2.20	2.94	mA	All Input with 1Mbps, C _L = 15pF
	I _{DD2} (1M)		2.20	2.94	mA	
	I _{DD1} (10M)		2.57	3.44	mA	All Input with 10Mbps, C _L = 15pF
	I _{DD2} (10M)		2.57	3.44	mA	
	I _{DD1} (100M)		6.11	8.25	mA	All Input with 100Mbps, C _L = 15pF
	I _{DD2} (100M)		6.11	8.25	mA	

6.4. Supply Current Characteristics–2.5V Supply

(VDD1=2.5V± 10%, VDD2=2.5V± 10%, Ta=-55°C to 125°C. Unless otherwise noted, Typical values are at **VDD1 = 2.5V**, **VDD2 = 2.5V**, Ta = 25°C)

Parameters	Symbol	Min	Typ	Max	Unit	Comments
Supply current	SP201AW1					
	I _{DD1} (Q0)		1.46	1.93	mA	All Input at supply for SP201AW1
	I _{DD2} (Q0)		1.46	1.93	mA	
	I _{DD1} (Q1)		2.76	3.67	mA	All Input 0V at supply for SP201AW1
	I _{DD2} (Q1)		2.76	3.67	mA	
	I _{DD1} (1M)		2.14	2.85	mA	All Input with 1Mbps, C _L = 15pF
	I _{DD2} (1M)		2.14	2.85	mA	
	I _{DD1} (10M)		2.42	3.22	mA	All Input with 10Mbps, C _L = 15pF
	I _{DD2} (10M)		2.42	3.22	mA	
	I _{DD1} (100M)		5.14	6.81	mA	All Input with 100Mbps, C _L = 15pF
	I _{DD2} (100M)		5.14	6.81	mA	

6.5. Switching Characteristics - 5V Supply

(VDD1=5V± 10%, VDD2=5V± 10%, Ta=-55°C to 125°C. Unless otherwise noted, Typical values are at **VDD1 = 5V, VDD2 = 5V**, Ta = 25°C)

Parameters	Symbol	Min	Typ	Max	Unit	Comments
SP201AW1						
Data Rate	DR	0		100	Mbps	
Minimum Pulse Width	PW			8.3	ns	
Propagation Delay	t _{PLH}		12.5	18	ns	See Figure 6.5 , C _L = 15pF
	t _{PHL}		12.1	18	ns	See Figure 6.5 , C _L = 15pF
Pulse Width Distortion t _{PHL} – t _{PLH}	PWD			5.0	ns	See Figure 6.5 , C _L = 15pF
Rising Time	t _r			5.0	ns	See Figure 6.5 , C _L = 15pF
Falling Time	t _f			5.0	ns	See Figure 6.5 , C _L = 15pF
Peak Eye Diagram Jitter	t _{JIT} (PK)		2.5		ns	
Channel-to-Channel Delay Skew	t _{SK} (c2c)			2.5	ns	
Part-to-Part Delay Skew	t _{SK} (p2p)			5.0	ns	

6.6. Switching Characteristics - 3.3V Supply

(VDD1=3.3V± 10%, VDD2=3.3V± 10%, Ta=-55°C to 125°C. Unless otherwise noted, Typical values are at **VDD1 = 3.3V, VDD2 = 3.3V**, Ta = 25°C)

Parameters	Symbol	Min	Typ	Max	Unit	Comments
SP201AW1						
Data Rate	DR	0		100	Mbps	
Minimum Pulse Width	PW			8.3	ns	
Propagation Delay	t _{PLH}		13.0	19	ns	See Figure 6.5 , C _L = 15pF
	t _{PHL}		12.5	19	ns	See Figure 6.5 , C _L = 15pF
Pulse Width Distortion t _{PHL} – t _{PLH}	PWD			5.0	ns	See Figure 6.5 , C _L = 15pF
Rising Time	t _r			5.0	ns	See Figure 6.5 , C _L = 15pF
Falling Time	t _f			5.0	ns	See Figure 6.5 , C _L = 15pF

Peak Eye Diagram Jitter	$t_{JIT}(PK)$		2.5		ns	
Channel-to-Channel Delay Skew	$t_{SK}(c2c)$			2.5	ns	
Part-to-Part Delay Skew	$t_{SK}(p2p)$			5.0	ns	

6.7. Switching Characteristics - 2.5V Supply

(VDD1=2.5V± 10%, VDD2=2.5V± 10%, Ta=-55°C to 125°C. Unless otherwise noted, Typical values are at **VDD1 = 2.5V**, **VDD2 = 2.5V**, Ta = 25°C)

Parameters	Symbol	Min	Typ	Max	Unit	Comments
	SP201AW1					
Data Rate	DR	0		100	Mbps	
Minimum Pulse Width	PW			8.3	ns	
Propagation Delay	t_{PLH}		14.2	20	ns	See Figure 6.5 , $C_L = 15pF$
	t_{PHL}		13.5	20	ns	See Figure 6.5 , $C_L = 15pF$
Pulse Width Distortion $ t_{PHL} - t_{PLH} $	PWD			5.0	ns	See Figure 6.5 , $C_L = 15pF$
Rising Time	t_r			5.0	ns	See Figure 6.5 , $C_L = 15pF$
Falling Time	t_f			5.0	ns	See Figure 6.5 , $C_L = 15pF$
Peak Eye Diagram Jitter	$t_{JIT}(PK)$		2.5		ns	
Channel-to-Channel Delay Skew	$t_{SK}(c2c)$			2.5	ns	
Part-to-Part Delay Skew	$t_{SK}(p2p)$			5.0	ns	

6.8. Typical Performance Characteristics

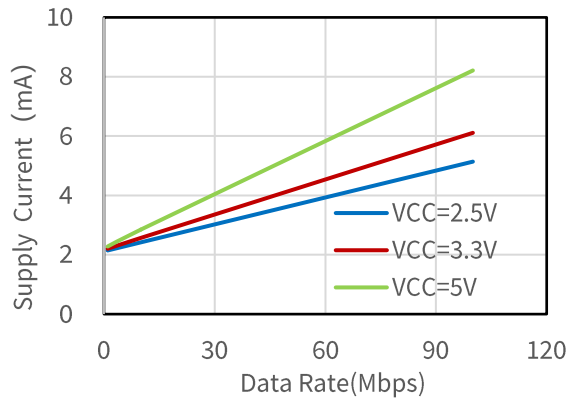


Figure 6.1 SP201AW1 VDD1 Supply Current vs Data Rate

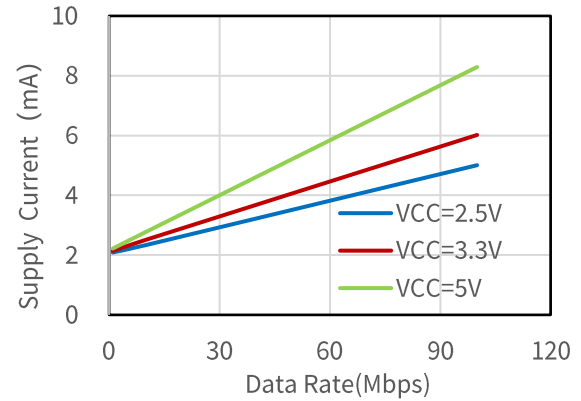


Figure 6.2 SP201AW1 VDD2 Supply Current vs Data Rate

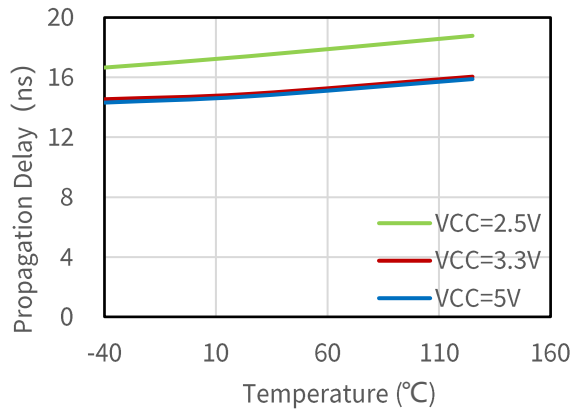


Figure 6.3 SP201AW1 Rising Edge Propagation Delay Vs Temp

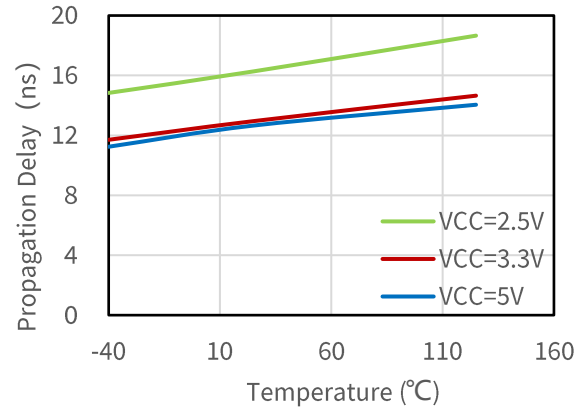
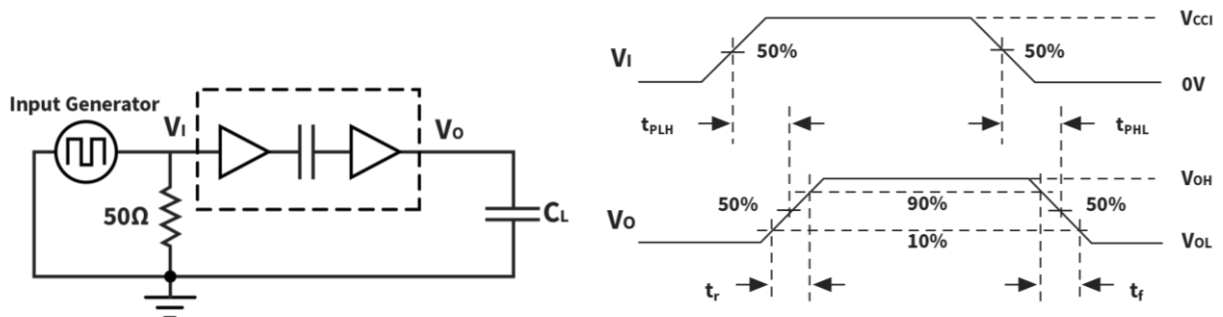


Figure 6.4 SP201AW1 Falling Edge Propagation Delay Vs Temp

6.9. Parameter Measurement Information



(1) Input Generator Characteristics : PRR $\leq$ 50kHz, $t_r \leq 3$ ns, $t_f \leq 3$ ns, Duty cycle = 50%, $Z_o = 50 \Omega$.

Figure 6.5 Switching Characteristics Test Circuit and Waveform

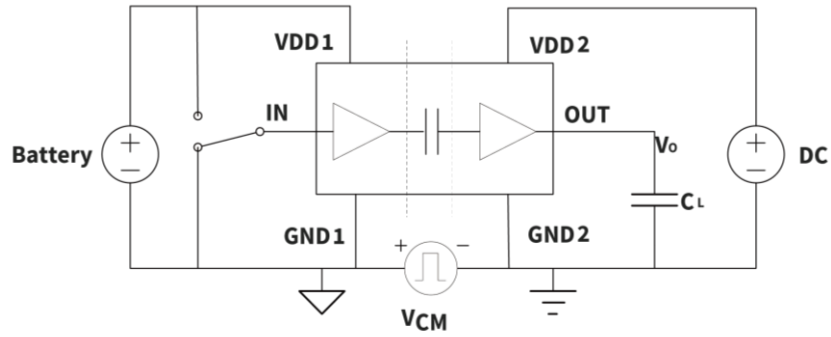


Figure 6.6 Common-Mode Transient Immunity Test Circuit

7. High Voltage Feature Description

7.1. Insulation and Safety Related Specifications

<i>Parameters</i>	<i>Symbol</i>	<i>Value</i> SOW8	<i>Unit</i>	<i>Comments</i>
Minimum External Clearance	CLR	8.0	mm	IEC 60664-1
Minimum External Creepage	CPG	8.0	mm	IEC 60664-1
Distance Through Insulation	DTI	24	μm	
Tracking Resistance (Comparative Tracking Index)	CTI	>600	V	DIN EN 60112 (VDE 0303-11); IEC 60112
Material Group		I		IEC 60664-1

<i>Description</i>	<i>Test Condition</i>	<i>Value</i> SOW8
Overvoltage Category per IEC60664-1	For Rated Mains Voltage $\leq$ 150Vrms	I to IV
	For Rated Mains Voltage $\leq$ 300Vrms	I to IV
	For Rated Mains Voltage $\leq$ 600Vrms	I to IV
	For Rated Mains Voltage $\leq$ 1000Vrms	I to III
Climatic Classification		40/125/21
Pollution Degree per DIN VDE 0110,		2

7.2. Insulation Characteristics

<i>Description</i>	<i>Test Condition</i>	<i>Symbol</i>	<i>SOW8</i>	<i>Unit</i>
Maximum repetitive isolation voltage		V_{IORM}	2121	V_{PEAK}
Maximum Working Isolation Voltage	AC voltage	V_{IOWM}	1500	V_{RMS}
	DC voltage		2121	V_{DC}

Description	Test Condition	Symbol	SOW8	Unit
Apparent Charge	Method a, after Input/output safety test subgroup 2/3, $V_{ini}=V_{IOTM}$, $t_{ini}=60s$, $V_{pd(m)}=1.2 \cdot V_{IORM}$, $t_m=10s$.	q_{pd}	<5	pC
	Method a, after environmental tests subgroup 1, $V_{ini}=V_{IOTM}$, $t_{ini}=60s$, $V_{pd(m)}=1.6 \cdot V_{IORM}$, $t_m=10s$			pC
	Method b, routine test (100% production) and preconditioning (type test); $V_{ini}=1.2 \cdot V_{IOTM}$, $t_{ini}=1s$ $V_{pd(m)}=1.875 \cdot V_{IORM}$, $t_m=1s$ (method b1) or $V_{pd(m)}=V_{ini}$, $t_m=t_{ini}$ (method b2)			pC
Maximum transient isolation voltage	$t = 60 \text{ sec}$	V_{IOTM}	8000	V_{PEAK}
Maximum impulse voltage	Tested in air, 1.2/50us waveform per IEC62368-1	V_{IMP}	6250	V_{PEAK}
Maximum Surge Isolation Voltage	Test method per IEC60065, 1.2/50us waveform, $V_{IOSM} \geq V_{IMP} \times 1.3$	V_{IOSM}	10000	V_{PEAK}
Isolation resistance	$V_{IO}=500V$, $T_{amb}=25^{\circ}C$	R_{IO}	$>10^{12}$	Ω
	$V_{IO}=500V$, $100^{\circ}C \leq T_{amb} \leq 125^{\circ}C$		$>10^{11}$	Ω
	$V_{IO}=500V$, $T_{amb}=T_s$		$>10^9$	Ω
Isolation capacitance	$f = 1MHz$	C_{IO}	0.6	pF
Withstand Isolation Voltage	$V_{TEST} = V_{ISO}$, $t = 60s$ (qualification), $V_{TEST} = 1.2 \times V_{ISO}$, $t = 1s$ (100% production test)	V_{ISO}	5000	V_{RMS}

7.3. Safety-Limiting Values

Reinforced isolation safety-limiting values as outlined in VDE-0884-17 of SP201AW1-DSWVR SOW8(300mil)

Description	Test Condition	Symbol	Value	Unit
Safety Supply Power	$R_{\theta JA} = 84.3 \text{ }^{\circ}\text{C/W}^{(1)}$, $V_I = 5.5 \text{ V}$, $T_J = 150 \text{ }^{\circ}\text{C}$, $T_A = 25 \text{ }^{\circ}\text{C}$		1483	mW
Safety Supply Current	$R_{\theta JA} = 84.3 \text{ }^{\circ}\text{C/W}^{(1)}$, $T_J = 150 \text{ }^{\circ}\text{C}$, $T_A = 25 \text{ }^{\circ}\text{C}$		269.6	mA
Safety Temperature ²⁾		T_S	150	$^{\circ}\text{C}$

- 1) Calculate with the junction-to-air thermal resistance, $R_{\theta JA}$, of SOW8(300mil) package ([Thermal Information Table](#)) which is that of a device installed on a low effective thermal conductivity test board (1s) according to JESD51-3.
- 2) The maximum safety temperature has the same value as the maximum junction temperature (T_J) specified for the device.

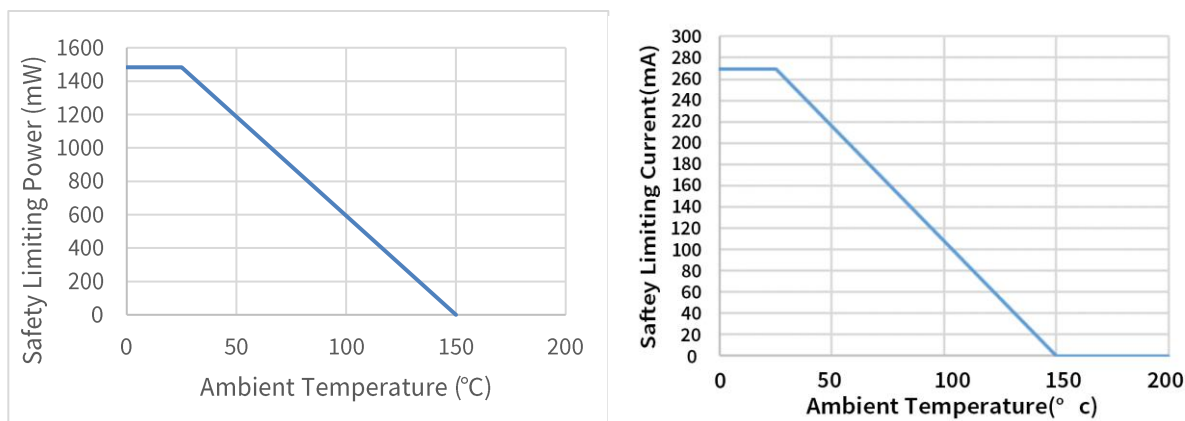


Figure 7.1 SP201AW1-DSWVR Thermal Derating Curve, Dependence of Safety Limiting Values with Case Temperature per DIN VDE V 0884-17

7.4. Regulatory Information

The SP201AW1-DSWVR are approved by the organizations listed in table.

<i>CUL</i>		<i>VDE</i>	<i>CQC</i>	<i>TUV</i>
UL 1577 Component Recognition Program	Approved under CSA Component Acceptance Notice 5A	DIN EN IEC 60747-17 (VDE 0884-17)	Certified according to GB4943.1	Certified According to EN IEC 62368-1
Single Protection, 5000V _{rms} Isolation voltage	Single Protection, 5000V _{rms} Isolation voltage	Reinforced Insulation V _{IORM} =2121V _{peak} V _{IOTM} =8000V _{peak} V _{IOSM} =10000V _{peak}	Reinforced insulation	5000Vrms for 1min
E500602	E500602	40052820	CQC20001264938	R50574061

8. Function Description

8.1. Overview

The SP201AW1 is a Dual-channel digital isolator based on a capacitive isolation barrier technique. The digital signal is modulated with RF carrier generated by the internal oscillator at the Transmitter side. Then it is transferred through the capacitive isolation barrier and demodulated at the Receiver side.

The SP201AW1 devices are high reliability dual-channel digital isolator. The SP201AW1 device is safety certified by UL1577 support 5kV_{rms} insulation withstand voltages, while providing high electromagnetic immunity and low emissions at low power consumption. The data rate of the SP201AW1 is up to 100Mbps, and the common-mode transient immunity (CMTI) is up to 250kV/us. The SP201AW1 device provides digital channel direction configuration and the default output level configuration when the input power is lost. Wide supply voltage of the SP201AW1 device support to connect with most digital interface directly, easy to do the level shift. High system level EMC performance enhance reliability and stability of use.

The SP201AW1 has a default output status when VDD_{IN} is unready and VDD_{OUT} is ready as shown in Table 7.1, which helps for diagnosis when power is missing at the transmitter side. The output B follows the same status with the input A within 60us after powering up.

Table 8.1 Output status vs. power status

Input ¹	VDD _{IN} status	VDD _{OUT} status	Output	Comment
H	Ready	Ready	H	Normal operation.
L	Ready	Ready	L	
X	Unready	Ready	H	The output follows the same status with the input within 60us after input side VDD _{IN} is powered on.
X	Ready	Unready	Undetermined	The output follows the same status with the input within 60us after output side VDD _{OUT} is powered on.
Note: H=Logic high; L=Logic low; X=Logic low or logic high; Z=High impedance. VDD _{IN} is input side power; VDD _{OUT} is output side power. (1) There is a protection diode between the input and the VDD _{IN} . When the VDD _{IN} is floating, the strong drive signal through the input pin will put the VDD _{IN} in an indeterminate state.				

8.2. OOK Modulation

SP201AW1 is based on a capacitive isolation barrier technique and the digital signal is modulated with RF carrier generated by the internal oscillator at the transmitter side, as shown in Figure 8.1, then it is transferred through the capacitive isolation barrier and demodulated at the receiver side. The modulation uses OOK modulation technique with key benefits of high noise immunity and low radiation EMI.

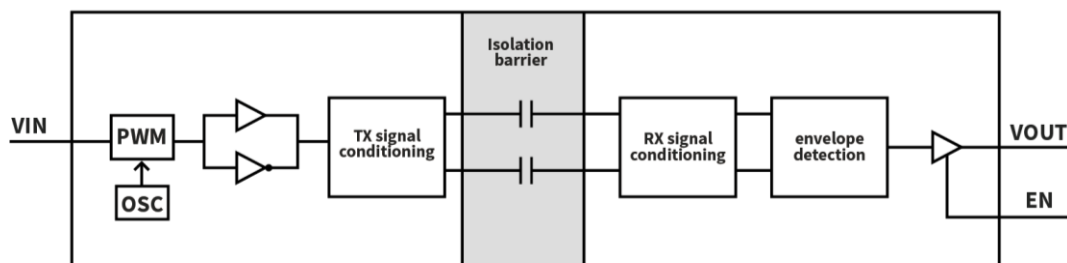


Figure 8.1 Single Channel Function Block Diagram

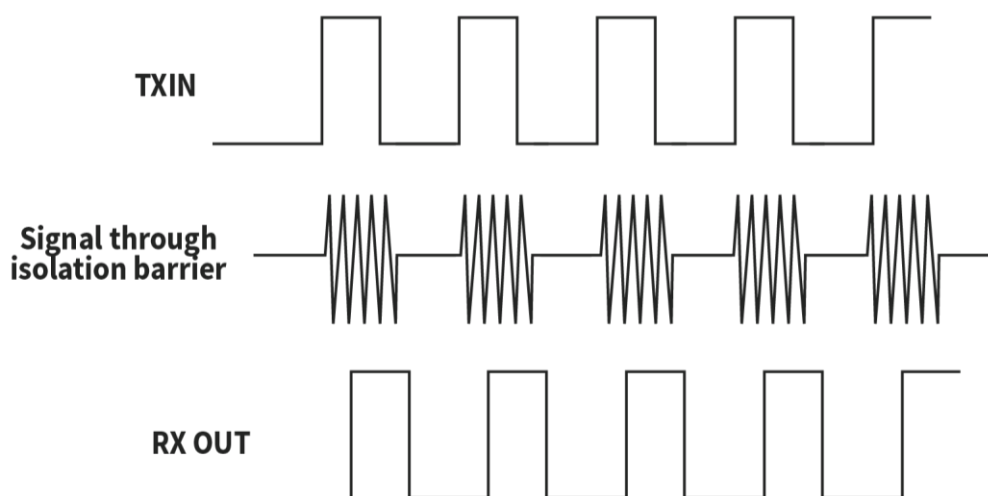


Figure 8.2 OOK Modulation

9. Application Note

9.1. Typical Application Circuit

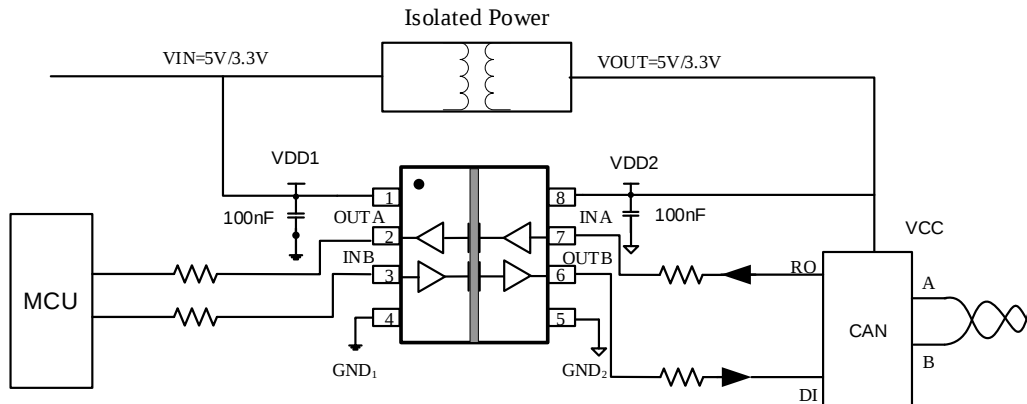


Figure 9.1 Typical SCH for ISO CAN Interface

9.2. PCB Layout

The SP201AW1 requires a 0.1 μF bypass capacitor between VDD1 and GND1, VDD2 and GND2. The capacitor should be placed as close as possible to the package. Figure 9.2 to Figure 9.3 show the recommended PCB layout, make sure the space under the chip should keep free from planes, traces, pads and via. To enhance the robustness of a design, the user may also include resistors (50–300 Ω) in series with the inputs and outputs if the system is excessively noisy. The series resistors also improve the system reliability such as latch-up immunity.

The typical output impedance of an isolator driver channel is approximately 50 Ω , $\pm 40\%$. When driving loads where transmission line effects will be a factor, output pins should be appropriately terminated with controlled impedance PCB traces.

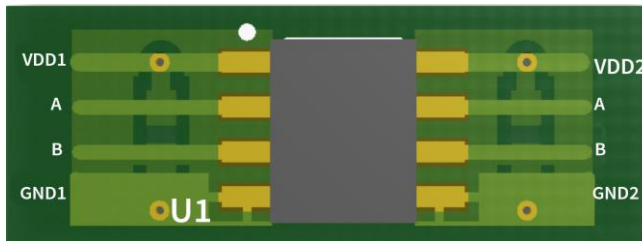


Figure9.2 Recommended PCB Layout — Top Layer



Figure9.3 Recommended PCB Layout — Bottom Layer

9.3. High Speed Performance

Figure 9.4 shows the eye diagram of SP201AW1 at 50Mbps data rate output. The result shows a typical measurement on SP201AW1 with low jitter and wide open eye characteristics.

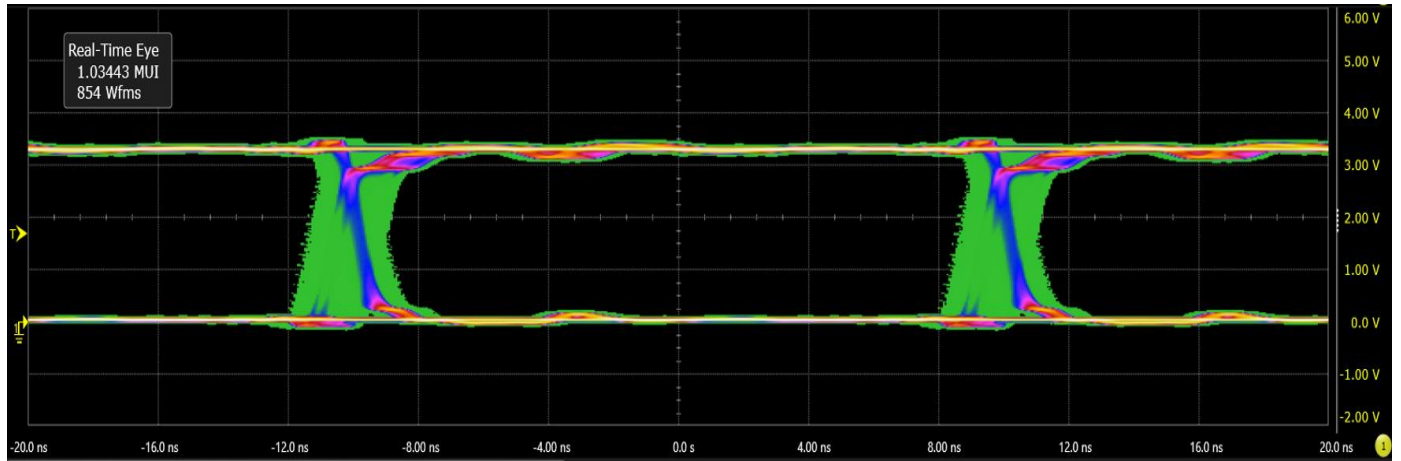
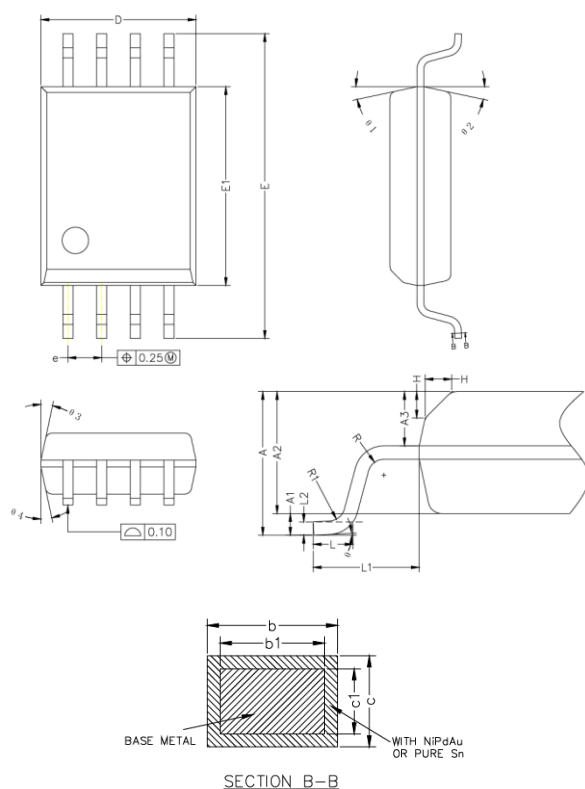


Figure9.4 Eye Diagram at 50Mbps PRBS $2^{16}-1$, 2.5V and 25°C

10. Package Information



COMMON DIMENSIONS
(UNITS OF MEASURE=MILLIMETER)

SYMBOL	MIN	NOM	MAX
A	—	—	2.85
A1	0.31	0.41	0.51
A2	2.20	2.30	2.40
A3	0.97	1.02	1.07
b PURE Sn	0.33	—	0.47
NiPdAu	0.31	—	0.51
b1	0.29	—	0.43
c PURE Sn	0.22	—	0.35
NiPdAu	0.13	—	0.33
c1	0.11	—	0.31
D	5.75	5.85	5.95
E	11.25	11.50	11.75
E1	7.40	7.50	7.60
e	1.27BSC		
H	0.50REF		
L	0.50	—	1.00
L1	2.00REF		
L2	0.25BSC		
R	0.07REF		
R1	0.07REF		
θ	0°	—	8°
θ 1	12°REF		
θ 2	12°REF		
θ 3	12°REF		
θ 4	12°REF		

NOTES:

1. ALL DIMENSIONS DO NOT INCLUDE MOLD FLASH OR PROTRUSIONS.

NOTE: This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm, per side.

Figure 10.1 SOW8 Package Shape and Dimension in millimeters

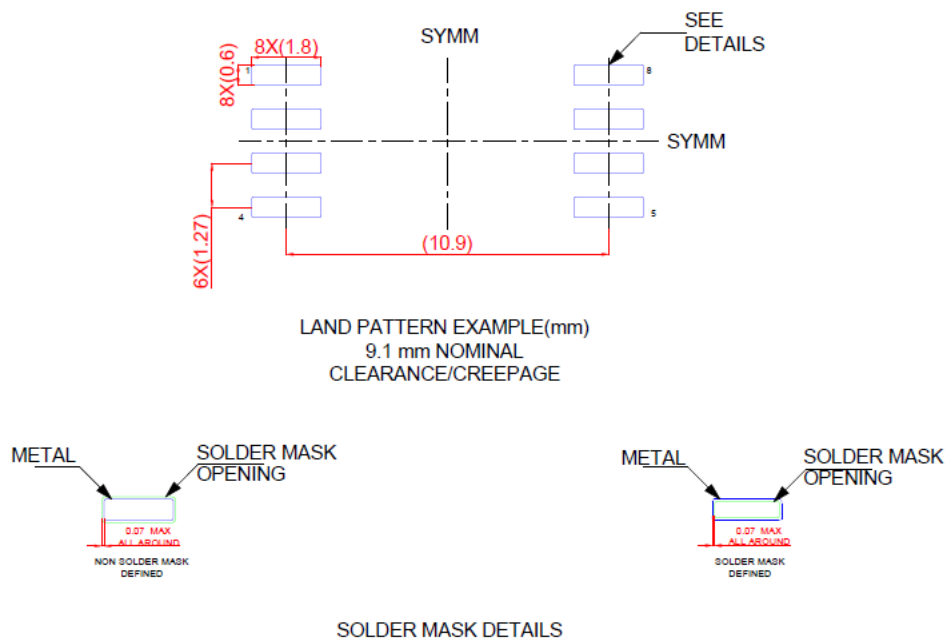


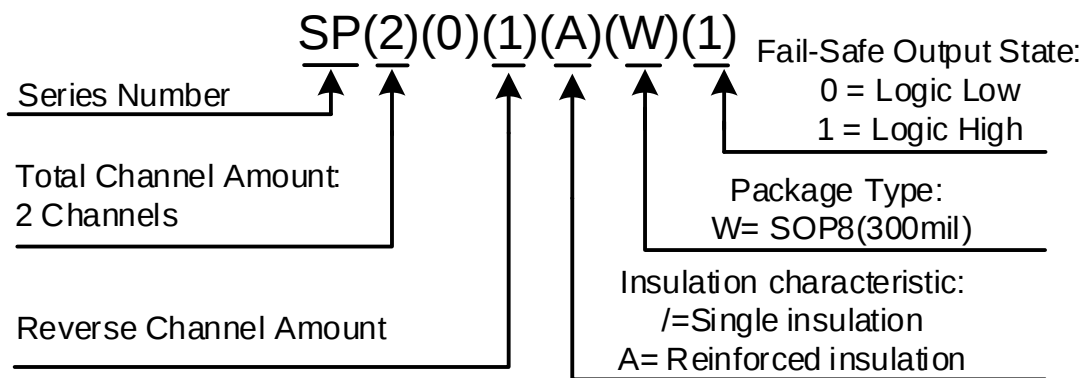
Figure 10.2 SOW8 Package Board Layout Example

11. Order Information

Part Number	Isolation Rating (kV)	Number of side 1 inputs	Number of side 2 inputs	Max Data Rate (Mbps)	Default Output State	Temperature	MSL	Package Type	Package Drawing	SPQ
SP201AW1-DSWVR	5	1	1	100	High	-55 to 125°C	3	SOW8 (300mil)	SOW8	1000

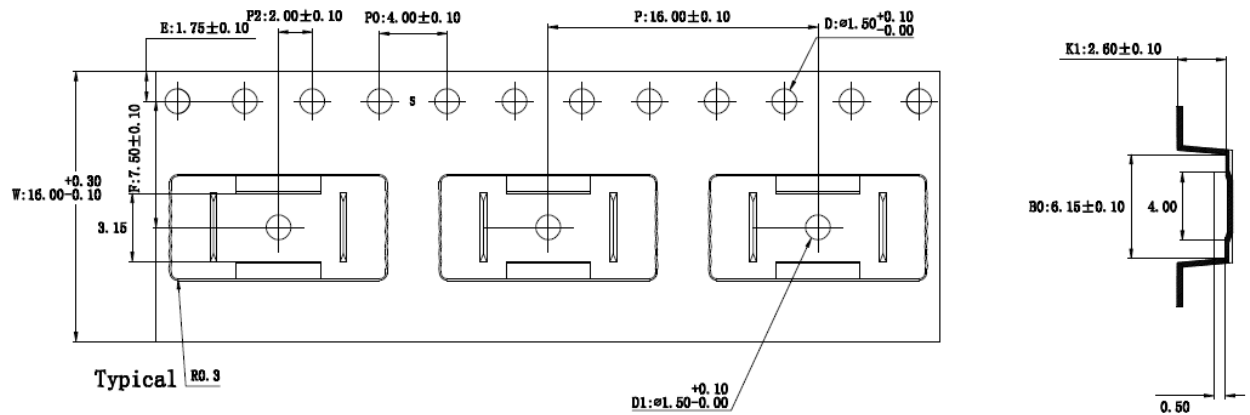
NOTE: All packages are RoHS-compliant with peak reflow temperatures of 260 °C according to the JEDEC industry standard classifications and peak solder temperatures.

Part Number Rule:



12. Documentation Support

Part Number	Product Folder	Datasheet	Technical Documents	Isolator selection guide
SP201AW1	tbd	tbd	tbd	tbd

**技术要求:****Technical Requirements:**

- 每10个料带链孔直径累计公差为 ± 0.20 毫米。
10 sprocket hole pitch cumulative toleran ± 0.20 mm
- 料带弯曲每250毫米不可超过1毫米。
Carrier camber is within 1 mm in 250 mm
- 所有尺寸符合EIA-481-D标准要求。
All dimensions meet EIA-481-D requirements

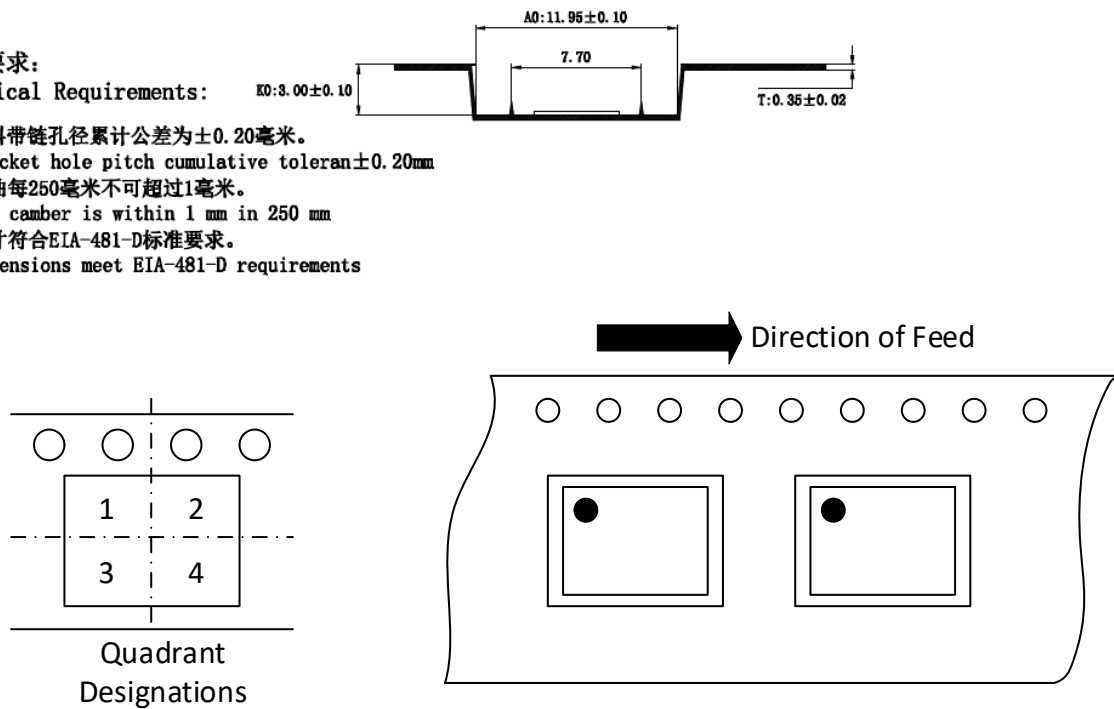


Figure 13.2 Tape Information of SOW8

14. Revision History

<i>Revision</i>	<i>Description</i>	<i>Date</i>
1.0	Initial version	2023/4/23
2.0	Update electrical characteristics of SOW8 products. Update supply current characteristics at 2.5V/3.3V/5V. Update switching characteristics at 2.5V/3.3V/5V. Add AMR description. Add ESD ratings description. Add Ψ_{JT} and Ψ_{JB} into thermal information. Update eye diagram. Update package information of SOW8 products. Delete typical supply current equations. Add part number rule.	2026/1/25

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