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Date : 2026/05/18

APPROVAL SHEET

Product Name : Vertical Stacked Capacitors

Part No. : VE3HN993J102LGLM

Description : Size 2220, C0G, 99nF, ±5%, 1000Vdc

PREPARED BY	APPROVED BY

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SPECIFICATION

FOR

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Part No. : VE3HN993J102LGLM

Description : Size 2220, C0G, 99nF, $\pm 5\%$, 1000Vdc

SPEC. No. : VE-018-001-01

DATE : 2026/05/18

DRAWN BY	CHECEKED BY	APPROVED BY
<i>Daisy Shen</i>	<i>Yvens Chou</i>	<i>Hank chiang</i>

1. INTRODUCTION

VE Series green type capacitors are manufactured by using green materials without lead and cadmium. These capacitors to achieve a unique structure of high reliability. The use of metal lead frame, can absorb the heat and mechanical stress. ESR (equivalent series resistance), ESL (equivalent series inductance) is small, the most suitable for high frequency operation of the rectifier power supply.

2. FEATURES

- High reliability and stability.
- Higher mechanical endurance.
- Anti thermal stress and mechanical stress.
- Improved vibration performance.
- More capacitance without changing footprint.
- RoHS Compliant.

3. APPLICATIONS

- DC to DC converter.
- High voltage coupling/DC blocking.
- Back-lighting inverters.
- Snubbers in high frequency power converters.
- Power supplies.
- Surge protection.
- Filtering, smoothing, and decoupling application.

4. HOW TO ORDER

<u>VE</u>	<u>3H</u>	<u>N</u>	<u>993</u>	<u>J</u>	<u>102</u>	<u>L</u>	<u>G</u>	<u>L</u>	<u>M</u>
PDC Family	Size	Dielectric	Capacitance	Tolerance	Rated Voltage	Packaging	Thickness	Control Code	Control Code-2
Table 1	Table 2	Table 3	Table 4	Table 5	Table 6	Table 7	Table 8	Table 9	Table 10

Table 1	PDC Family
Code	Description
VE	Vertical Stacked Capacitors Series

Table 2	Stack chip quantity and chip size
The first digit : # of chips in stack	
Second digit code : chip size (below)	
Code	Description
H	2220 (5750)

Table 3	Dielectric Material Characteristics
Code	Description
N	C0G
T	X7T

Table 4	Capacitance Rule Code
Code	Description
R47	0.47pF
0R5	0.5pF
100	100=10x10 ⁰ =10pF

Table 5	Tolerance
Code	Description
A	±0.05 pF
B	±0.10 pF
C	±0.25 pF
D	±0.50 pF
F	±1 %
G	±2 %
H	±3 %

Table 6	Rated Voltage
Code	Description
250	25Vdc
500	50Vdc
101	100Vdc

Table 7	Packaging Type
Code	Description
B	Bulk
L	Tape and 13" Reel, Embossed Tape

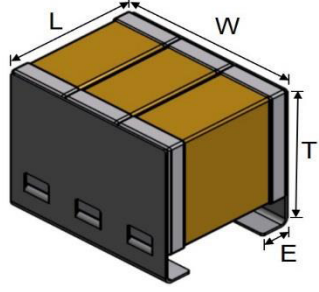
Table 8	Thickness Description
Code	Description
A	3.00±0.35 mm
B	3.60±0.35 mm
C	4.20±0.35 mm
D	4.80±0.35 mm
E	5.40±0.35 mm
F	6.00±0.35 mm
G	6.60±0.35 mm
H	7.20±0.35 mm

Table 9	Special Control Code
Code	Description
M	M type lead
L	L type lead

Table 10	Special Control Code-2
Code	Description
Blank	General products
M	Automotive

5. EXTERNAL DIMENSIONS

VE3H

Size Inch (mm)	2220 (5750)	
L (mm)	6.00±0.50	
W (mm)	7.50±0.50	
Code / T (mm)	G/6.60±0.35	
E (mm)	1.20±0.15	
		Fig. 5.1 The outline of Vertical Stacked Capacitors

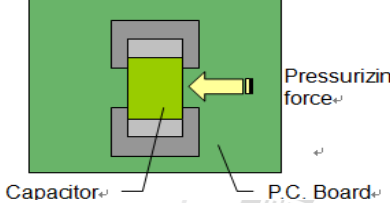
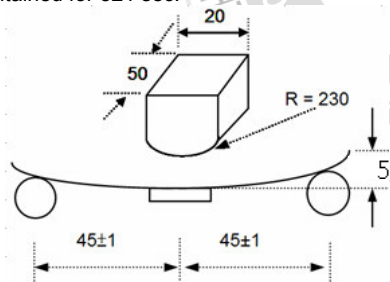
6. GENERAL ELECTRICAL DATA

Dielectric	C0G		
Size	2220		
Rated voltage (WVDC)	1000V		
Capacitance range	99nF		
Capacitance tolerance	±5%		
Tan δ	Cap. Range	Q Spec.	
	Cap.≥30pF	Q≥1000	
Capacitance & Tan δ Test condition	Measured at the condition of 30~70% related humidity		
	For 25°C at ambient temperature		
	Cap. Range	Test Condition	
	Cap.≥1000pF	1.0±0.2Vrms, 1.0KHz±10%	
Insulation resistance at Ur	≥10GΩ or RxC≥500Ω-F, whichever is smaller		
Operating temperature	-55 to +125°C		
Capacitance characteristic	±30ppm / °C		
Termination	L type lead		

7. RELIABILITY TEST CONDITIONS AND REQUIREMENTS

No.	Item	Test Condition	Requirements															
1.	Visual and Dimensions	---	* No remarkable defect. * Dimensions to confirm to individual specification sheet.															
2.	Capacitance		* Shall not exceed the limits given in the detailed spec.															
3.	Q/D.F. (Dissipation Factor)	* Class I : Cap.>1000pF, 1.0±0.2Vrms, 1KHz±10%.	<table><tr><td>Dielectric</td><td>Cap. Range</td><td>Q/D.F.</td></tr><tr><td>Class I (C0G)</td><td>Cap.≥30pF</td><td>Q≥1000</td></tr></table>	Dielectric	Cap. Range	Q/D.F.	Class I (C0G)	Cap.≥30pF	Q≥1000									
Dielectric	Cap. Range	Q/D.F.																
Class I (C0G)	Cap.≥30pF	Q≥1000																
4.	Temperature Coefficient	* With no electrical load. <table><tr><td>T.C.</td><td>Operating Temp.</td></tr><tr><td>C0G</td><td>-55~125°C at 25°C</td></tr></table>	T.C.	Operating Temp.	C0G	-55~125°C at 25°C	<table><tr><td>T.C.</td><td>Capacitance Change</td></tr><tr><td>C0G</td><td>Within ±30ppm/°C</td></tr></table>	T.C.	Capacitance Change	C0G	Within ±30ppm/°C							
T.C.	Operating Temp.																	
C0G	-55~125°C at 25°C																	
T.C.	Capacitance Change																	
C0G	Within ±30ppm/°C																	
5.	Insulation Resistance	<table><tr><td>Rated Vol. (V)</td><td>Apply Voltage</td><td>Test Time</td></tr><tr><td>>500</td><td>500Vdc</td><td>60 sec.</td></tr></table>	Rated Vol. (V)	Apply Voltage	Test Time	>500	500Vdc	60 sec.	<table><tr><td>Dielectric</td><td>Requirements</td></tr><tr><td>Class I</td><td>≥10GΩ or RxC≥500Ω-F, whichever is</td></tr></table>	Dielectric	Requirements	Class I	≥10GΩ or RxC≥500Ω-F, whichever is					
Rated Vol. (V)	Apply Voltage	Test Time																
>500	500Vdc	60 sec.																
Dielectric	Requirements																	
Class I	≥10GΩ or RxC≥500Ω-F, whichever is																	
6.	Dielectric Strength	<table><tr><td>Rated Voltage</td><td>Condition</td></tr><tr><td>630≤V≤3000V</td><td>1.2 times of U_R</td></tr></table> * Duration : 1 to 5 sec. * Charge and discharge current less than 50mA.	Rated Voltage	Condition	630≤V≤3000V	1.2 times of U _R	* No evidence of damage or flash over during test.											
Rated Voltage	Condition																	
630≤V≤3000V	1.2 times of U _R																	
7.	Temperature Cycle	* Conduct the 100 cycles according to the temperatures and time. <table><tr><td>Step</td><td>Temp.(°C)</td><td>Time(min.)</td></tr><tr><td>1</td><td>Min. operating temp. +0/-3</td><td>30±3</td></tr><tr><td>2</td><td>Room temp.</td><td>2~3</td></tr><tr><td>3</td><td>Max. operating temp. +3/-0</td><td>30±3</td></tr><tr><td>4</td><td>Room temp.</td><td>2~3</td></tr></table> * Before initial measurement : To apply de-aging at 150°C for 1hr then set for 24±2 hrs at room temp. * Measurement to be made after keeping at room temp. for 24±2 hrs (Class I) or 48±4 hrs (Class II).	Step	Temp.(°C)	Time(min.)	1	Min. operating temp. +0/-3	30±3	2	Room temp.	2~3	3	Max. operating temp. +3/-0	30±3	4	Room temp.	2~3	* No remarkable damage. * Cap. change : C0G Within ±2.5% or ±0.25pF, whichever is larger. * Q/D.F. : C0G : Q≥100% of initial requirement. * I.R. : To meet the initial requirement.
Step	Temp.(°C)	Time(min.)																
1	Min. operating temp. +0/-3	30±3																
2	Room temp.	2~3																
3	Max. operating temp. +3/-0	30±3																
4	Room temp.	2~3																
8.	Humidity (Damp Heat) Steady State	* Test temp. : 40±2°C. * Humidity : 90~95%RH. * Test time : 500 +24/-0hrs. * Before initial measurement : To apply de-aging at 150°C for 1hr then set for 24±2 hrs at room temp. * Measurement to be made after keeping at room temp. for 24±2 hrs (Class I) or 48±4 hrs (Class II).	* No remarkable damage. * Cap. change : C0G Within ±5.0% or ±0.5pF, whichever is larger. * Q/D.F. : C0G : Q≥350. * I.R. (Class I) : ≥1GΩ or RxC≥50Ω-F, whichever is smaller.															
9.	Humidity (Damp Heat) Load	* Test temp. : 40±2°C. * Humidity : 90~95%RH. * Test time : 500 +24/-0hrs. * To apply voltage : Rated voltage (500V max.). * Before initial measurement : To apply de-aging at 150°C for 1hr then set for 24±2 hrs at room temp. * Measurement to be made after keeping at room temp. for 24±2 hrs (Class I) or 48±4 hrs (Class II).	* No remarkable damage. * Cap. change : C0G Within ±7.5% or ±0.75pF, whichever is larger. * Q/D.F. : C0G : Q≥200. * I.R. : ≥500MΩ or RxC≥25Ω-F, whichever is smaller.															

7. RELIABILITY TEST CONDITIONS AND REQUIREMENTS

No.	Item	Test Condition	Requirements						
10.	High Temperature Load (Endurance)	* Test temp. : 125±3°C. * To apply voltage : <table><tr><th>Dielectric</th><th>Rated Vol.(V)</th><th>Apply Voltage</th></tr><tr><td>C0G</td><td>≥1000</td><td>1.0 times of U_R</td></tr></table> * Test time : 1000 +24/-0 hrs. * Before initial measurement : To apply de-aging at 150°C for 1hr then set for 24±2 hrs at room temp. * Measurement to be made after keeping at room temp. for 24±2 hrs (Class I) or 48±4 hrs (Class II).	Dielectric	Rated Vol.(V)	Apply Voltage	C0G	≥1000	1.0 times of U _R	* No remarkable damage. * Cap. change : C0G Within ±3.0% or ±0.3pF, whichever is larger. * Q/D.F. : C0G : Q≥350. * I.R. (Class I) : ≥1GΩ or RxC≥50Ω-F, whichever is smaller.
Dielectric	Rated Vol.(V)	Apply Voltage							
C0G	≥1000	1.0 times of U _R							
11.	Adhesive Strength of Termination	* Capacitors mounted on a substrate. A force of 10N applied perpendicular to the place of substrate and parallel the line joining the center of terminations for 10±1 second. 	* No remarkable damage or removal of the terminations.						
12.	Resistance to Flexure of Substrate	* The middle part of substrate shall be pressurized by means of the pressurizing rod at a rate of about 1mm per second until the deflection becomes 5mm and then the pressure shall be maintained for 5±1 sec.  Unit : mm	* No remarkable damage. <table><tr><th>Dielectric</th><th>Cap. Change</th></tr><tr><td>C0G</td><td>Within ±3.0% or ±2.0pF, whichever is larger</td></tr></table> (This capacitance change means the change of capacitance under specified flexure of substrate from the capacitance measured before the test)	Dielectric	Cap. Change	C0G	Within ±3.0% or ±2.0pF, whichever is larger		
Dielectric	Cap. Change								
C0G	Within ±3.0% or ±2.0pF, whichever is larger								
13.	Vibration Resistance	* Vibration frequency : 10~55 Hz/min. * Total amplitude : 1.5mm. * Test time : 6 hrs. (Two hrs each in three mutually perpendicular directions) * Before initial measurement : To apply de-aging at 150°C for 1hr then set for 24±2 hrs at room temp. * Measurement to be made after keeping at room temp. for 24±2 hrs (Class I) or 48±4 hrs (Class II).	* No remarkable damage. * Cap. change and D.F. : To meet initial spec.						
14.	Resistance to Soldering Heat	* Reflow soldering : Peak 260±5°C. * Preheating : 120 to 150°C for 1 minute before immerse the capacitor in a eutectic solder. * Before initial measurement : Perform 150 +0/-10°C for 1 hr and then set for 48±4 hrs at room temp. * Measurement to be made after keeping at room temp. for 24±2 hrs (Class I) or 48±4 hrs (Class II).	* No remarkable damage. * Cap. Change : C0G : Within ±2.5% or ±0.25pF, whichever is larger. * Q/D.F. & I.R. : To meet the initial requirement.						

8. PACKAGE DIMENSION AND QUANTITY

8.1. PACKAGE QUANTITY

PDC Family & Size	Thickness (mm)	Plastic tape
		13" reel
VE2H	ALL	0.5k
VE3H	ALL	0.4k
For other chip size, please contact the liaison		

8.2. EMBOSSED TAPE DIMENSIONS

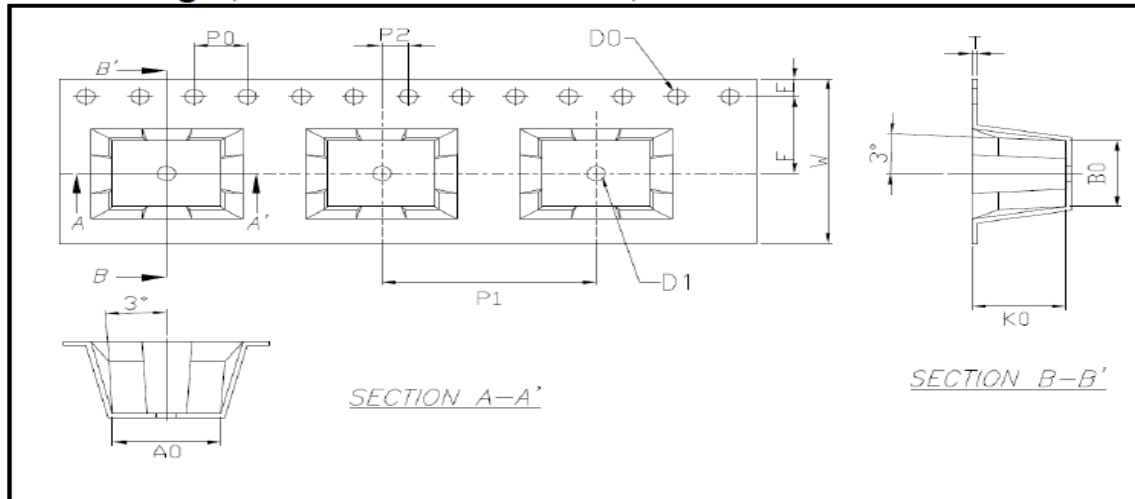


Fig. 8.1 The dimension of plastic tape

Size	VE2H	VE3H
Chip Thickness	6.40±0.50	6.60±0.35
W	16.00±0.30	16.00±0.30
E	1.75±0.10	1.75±0.10
F	7.50±0.10	7.50±0.10
P_1	16.00±0.10	16.00±0.10
P_0	4.00±0.10	4.00±0.10
10x P_0	40.00±0.20	40.00±0.20
P_2	2.00±0.10	2.00±0.10
D_0	Ø1.50 +0.10/-0	Ø1.50 +0.10/-0
T	0.40±0.05	0.40±0.05
A_0	5.75±0.10	8.05±0.10
B_0	6.50±0.10	6.40±0.10
K_0	6.85±0.10	7.00±0.10
Unit :	mm	mm

* For other chip size, please contact the liaison.

8. PACKAGE DIMENSION AND QUANTITY

8.3. REEL DIMENSIONS

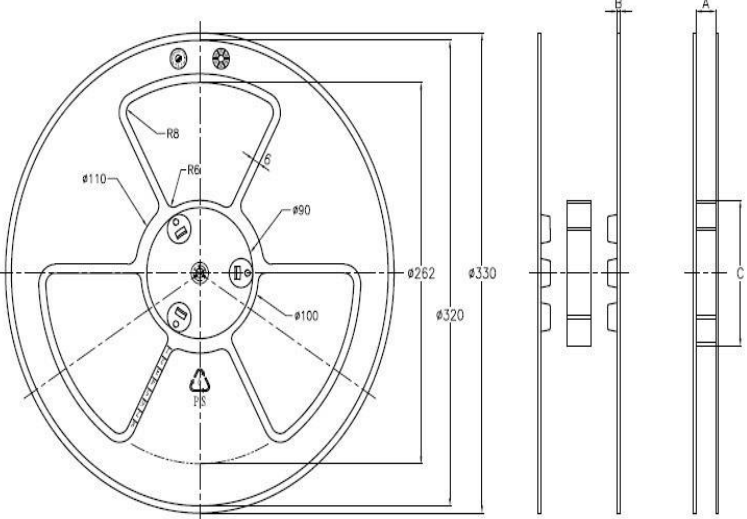
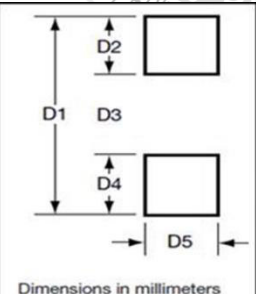
Reel size	13"	
A	16.50±0.10mm	
B	2.30±0.10mm	
C	100.00±0.10mm	

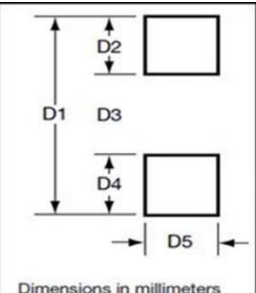
Fig. 8.2 The dimension of reel

9. FOOTPRINT DIMENSIONS

VE2H

Size	2220	Fig. 9.1 Illustration of Footprint
D1	7.3~8.7	
D2	1.5~2.0	
D3	4.3~4.7	
D4	1.5~2.0	
D5	5.2~5.7	

VE3H

Size	2220	Fig. 9.2 Illustration of Footprint
D1	7.3~8.7	
D2	1.5~2.0	
D3	4.3~4.7	
D4	1.5~2.0	
D5	7.9~8.4	

10. APPLICATION NOTES

STORAGE

To prevent the damage of solderability of terminations, the following storage conditions are recommended :

Indoors under 5 ~ 40°C and 20% ~ 70% RH.

No harmful gases containing sulfuric acid, ammonia, hydrogen sulfide or chlorine.

Packaging should not be opened until the capacitors are required for use. If opened, the pack should be re-sealed as soon as is practicable. Taped product should be stored out of direct sunlight, which might promote deterioration in tape or adhesion performance. The product is recommended to be used within 12 months after shipment and checked the solderability before use.

HANDLING

Chip capacitors are dense, hard, brittle, and abrasive materials. They are liable to suffer mechanical damage, in the form of cracks or chips. Chip Capacitors should be handled with care to avoid contamination or damage. To use vacuum or plastic tweezers to pick up or plastic tweezers is recommended for manual placement. Tape and reeled packages are suitable for automatic pick and placement machine.

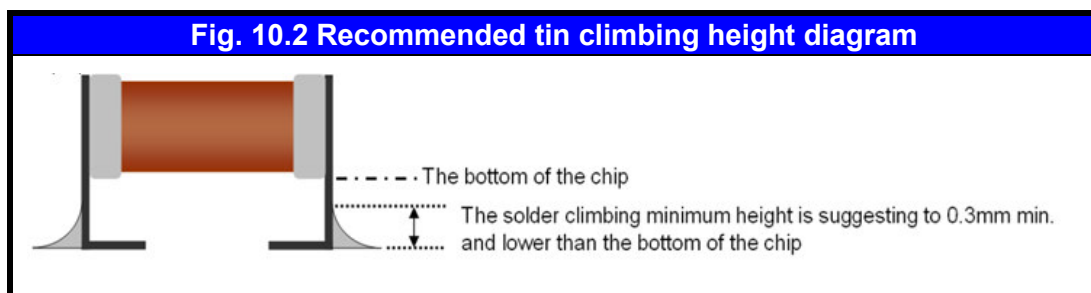
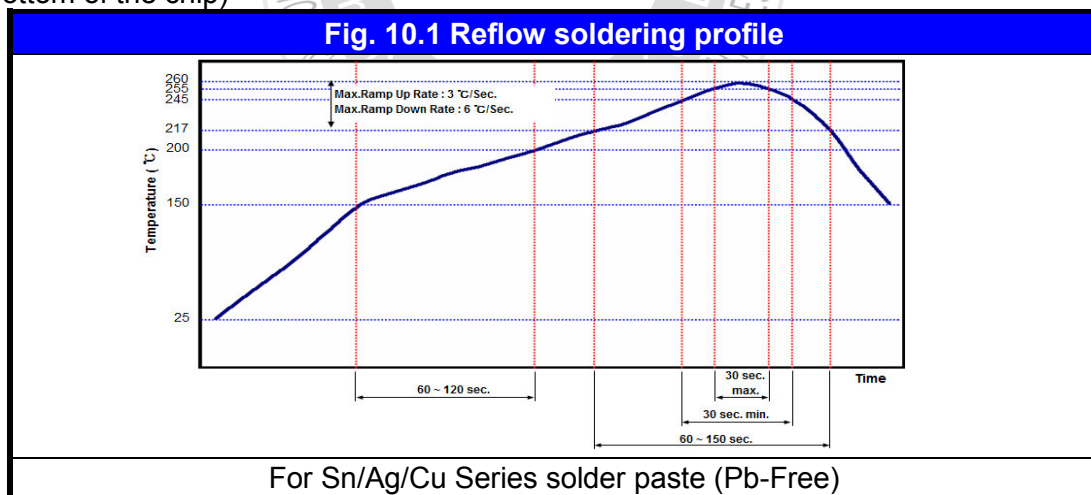
PREHEAT

In order to minimize the risk of thermal shock during soldering, a carefully controlled preheat is required. The rate of preheat should not exceed 3°C per second.

SOLDERING

Use mildly activated rosin fluxes do not use activated flux. The amount of solder in each solder joint should be controlled to prevent the damage of chip capacitors caused by the stress between solder, chips, and substrate.

a.) Reflow soldering : (Please make sure that solder is smoothly applied higher than 0.3mm and lower than the level of the bottom of the chip)



10. APPLICATION NOTES

COOLING

After soldering, cool the chips and the substrate gradually to room temperature. Natural cooling in air is recommended to minimize stress in the solder joint.

CLEANING

All flux residues must be removed by using suitable electronic-grade vapor-cleaning solvents to eliminate contamination that could cause electrolytic surface corrosion. Good results can be obtained by using ultrasonic cleaning of the solvent. The choice of the proper system depends upon many factors such as component mix, flux, and solder paste and assembly method. The ability of the cleaning system to remove flux residues and contamination from under the chips is very important.

