NOVOSENSE

NSI812x
High Reliability Dual-Channel Digital Isolators
Datasheet (EN) 3.0

Product Overview

The NSI812x devices are high reliability dual-channel digital isolators. The NSI812x device is safety certified by UL1577 support 3kVrms insulation withstand voltage, while providing high electromagnetic immunity and low emissions at low power consumption. The data rate of the NSI812x is up to 150Mbps, and the common-mode transient immunity (CMTI) is up to 200kV/us. The NSI812x device provides digital channel direction configuration and the default output level configuration when the input power is lost. Wide supply voltage of the NSI812x device support to connect with most digital interface directly, easy to do the level shift. High system level EMC performance enhance reliability and stability of use.

Key Features

- Up to 3000V_{rms} Insulation voltage
- Data rate: DC to 150Mbps
- Power supply voltage: 2.5V to 5.5V
- High CMTI: 200kV/us
- Chip level ESD: HBM: ±6kV
- High system level EMC performance:
  Enhanced system level ESD, EFT, Surge immunity
- Default output high level or low level option
- Low power consumption: 1.5mA/ch (1 Mbps)
- Low propagation delay: <18ns
- Operation temperature: -40℃~125℃
- RoHS-compliant packages:
  SOP8 narrow body

Safety Regulatory Approvals

- UL recognition: up to 3000V_{rms} for 1 minute per UL1577
- CQC certification per GB4943.1
- CSA component notice 5A
- DIN EN IEC 60747-17 (VDE 0884-17)

Applications

- Industrial automation system
- Isolated SPI, RS232, RS485
- General-purpose multichannel isolation
- Motor control

Device Information

Part Number	*Package*	*Body Size*
NSI812xNx	SOP8	4.90mm × 3.90mm

Functional Block Diagrams

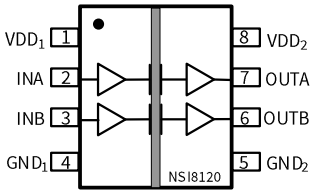

Figure 1.1 NSI8120 Block Diagram

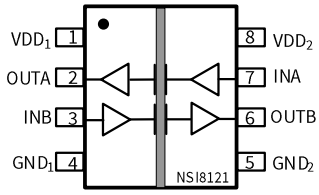

Figure 1.2 NSI8121 Block Diagram

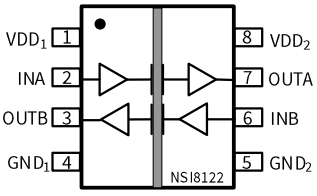

Figure 1.3 NSI8122 Block Diagram

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1. Pin Configuration and Functions

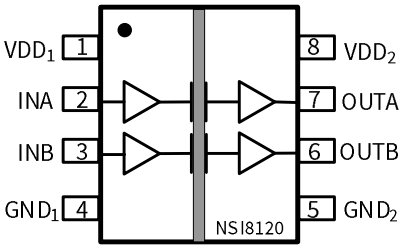


Figure 1.1 NSI8120 Package

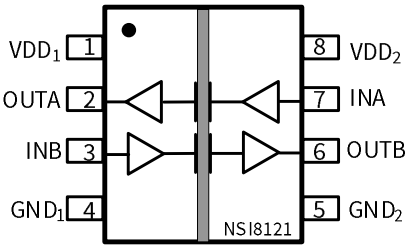


Figure 1.2 NSI8121 Package

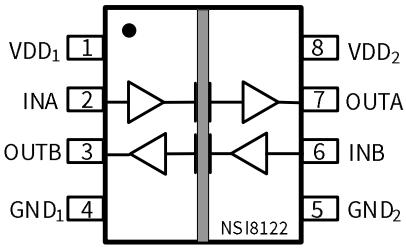


Figure 1.3 NSI8122 Package

Table1.1 NSI812x Pin Configuration and Description

NSI8120 PIN NO.	*NSI8121 PIN NO.*	*NSI8122 PIN NO.*	*SYMBOL*	*FUNCTION*
1	1	1	VDD1	Power Supply for Isolator Side 1
2	7	2	INA	Logic Input A
3	3	6	INB	Logic Input B
4	4	4	GND1	Ground 1, the ground reference for Isolator Side 1
5	5	5	GND2	Ground 2, the ground reference for Isolator Side 2
6	6	3	OUTB	Logic Output B
7	2	7	OUTA	Logic Output A
8	8	8	VDD2	Power Supply for Isolator Side 2

2. Absolute Maximum Ratings

Parameters	Symbol	Min	Typ	Max	Unit	Comments
Power Supply Voltage	VDD1, VDD2	-0.5		6.5	V	
Maximum Input Voltage	V_{INA}, V_{INB}	-0.4		VDD+0.4	V	The maximum voltage must not exceed 6.5V
Maximum Output Voltage	V_{OUTA}, V_{OUTB}	-0.4		VDD+0.4	V	The maximum voltage must not exceed 6.5V
Maximum Input/Output Pulse Voltage	V_{INA}, V_{INB}, V_{OUTA}, V_{OUTB}	-0.8		VDD+0.8	V	Pulse width should be less than 100ns, and the duty cycle should be less than 10%
Output current	Io	-15		15	mA	
Operating Temperature	Topr	-40		125	℃	
Junction Temperature	Tj			150	℃	
Storage Temperature	Tstg	-65		150	℃	

(1) Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under Recommended Operating conditions. Exposure to Absolute Maximum Rated conditions for extended periods may affect device reliability.

(2) Power supply voltage and input/output voltage are respect to the local ground terminal (GND1 or GND2) voltage values.

3. ESD Ratings

Parameters	Ratings	Value	Unit
Electrostatic discharge (ESD)	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001(2)	±6000	V
	Charged device model (CDM), per JEDEC specification JESD22-C101(3)	±2000	V

(1) Though this device features proprietary protection circuitry, proper ESD precautions should be considered to avoid performance degradation of damage due to high energy ESD event. Charged devices and circuit boards may discharge without detection.

(2) Safe manufacturing requires 500-V HBM and standard ESD precautions, per JEDEC document JEP155.

(3) Safe manufacturing requires 250-V CDM and standard ESD precautions, per JEDEC document JEP157.

4. Recommended Operating Conditions

Parameters	Symbol	min	typ	max	unit
Power Supply Voltage	VDD1, VDD2	2.5		5.5	V

Operating Temperature	Topr	-40		125	℃
High Level Input Voltage	VIH	0.7*VDD			V
Low Level Input Voltage	VIL			0.3*VDD	V
Data rate	DR			150	Mbps

5. Thermal Characteristics

Parameters	*Symbol*	*SOP8*	*Unit*
IC Junction-to-Air Thermal Resistance	θ_{JA}	137.7	℃/W
Junction-to-case (top) thermal resistance	$\theta_{JC(top)}$	54.9	℃/W
Junction-to-board thermal resistance	θ_{JB}	71.7	℃/W
Junction-to-top characterization parameter	Ψ_{JT}	7.6	℃/W
Junction-to-board characterization parameter	Ψ_{JB}	31.0	℃/W

6. Specifications

6.1. Electrical Characteristics

(VDD1=2.5V~5.5V, VDD2=2.5V~5.5V, Ta=-40℃ to 125℃. Unless otherwise noted, Typical values are at VDD1 = 5V, VDD2 = 5V, Ta = 25℃)

Parameters	*Symbol*	*Min*	*Typ*	*Max*	*Unit*	*Comments*
Power on Reset	VDD_{POR}	2	2.2	2.4	V	POR threshold as during power-up
	VDD_{HYS}		0.1		V	POR threshold Hysteresis
Rising input switching threshold	V_{IT+}		0.6*VDD	0.7*VDD	V	
Falling input switching threshold	V_{IT-}	0.3*VDD	0.4*VDD		V	
Input threshold voltage hysteresis	$V_{I(HYS)}$		0.2*VDD		V	
High Level Output Voltage	V_{OH}	VDD-0.4			V	$I_{OH} \le 4mA$
Low Level Output Voltage	V_{OL}			0.4	V	$I_{OL} \le 4mA$
Output Impedance	R_{out}		50		ohm	
Input Pull high or low Current	I_{pull}		5	10	uA	
Start Up Time after POR	trbs		15	30	usec	

Common Mode Transient Immunity	CMTI	±150	±200		kV/us	See Figure 6.8

6.2. Supply Current Characteristics –5V Supply

(VDD1=5V± 10%, VDD2=5V± 10%, Ta=-40℃ to 125℃. Unless otherwise noted, Typical values are at **VDD1 = 5V, VDD2 = 5V,** Ta = 25℃)

Parameters	*Symbol*	*Min*	*Typ*	*Max*	*Unit*	*Comments*
Supply current	**NSI8120Nx**					
	I_{DD1}(Q0)		0.62	0.90	mA	All Input 0V for NSI812xN0 Or All Input at supply for NSI812xN1
	I_{DD2}(Q0)		1.27	1.84	mA	
	I_{DD1}(Q1)		2.3	3.04	mA	All Input at supply for NSI812xN0 Or All Input 0V for NSI812xN1
	I_{DD2}(Q1)		1.31	1.73	mA	
	I_{DD1}(1M)		1.50	1.98	mA	All Input with 1Mbps, C_L=15pF
	I_{DD2}(1M)		1.43	1.89	mA	
	I_{DD1}(10M)		1.57	2.07	mA	All Input with 10Mbps, C_L=15pF
	I_{DD2}(10M)		2.59	3.39	mA	
	I_{DD1}(100M)		2.02	2.72	mA	All Input with 100Mbps, C_L= 15pF
	I_{DD2}(100M)		12.56	16.95	mA	
	NSI8121Nx/ NSI8122Nx					
	I_{DD1}(Q0)		1.07	1.36	mA	All Input 0V for NSI812xN0 Or All Input at supply for NSI812xN1
	I_{DD2}(Q0)		1.07	1.36	mA	
	I_{DD1}(Q1)		1.98	2.59	mA	All Input at supply for NSI812xN0 Or All Input 0V for NSI812xN1
	I_{DD2}(Q1)		1.98	2.59	mA	
	I_{DD1}(1M)		1.59	2.13	mA	All Input with 1Mbps, C_L=15pF
	I_{DD2}(1M)		1.59	2.13	mA	
	I_{DD1}(10M)		2.12	2.77	mA	All Input with 10Mbps, C_L=15pF
	I_{DD2}(10M)		2.12	2.77	mA	
	I_{DD1}(100M)		7.57	10.06	mA	All Input with 100Mbps, C_L= 15pF
	I_{DD2}(100M)		7.57	10.06	mA	

6.3. Supply Current Characteristics –3.3V Supply

(VDD1=3.3V± 10%, VDD2=3.3V± 10%, Ta=-40℃ to 125℃. Unless otherwise noted, Typical values are at **VDD1 = 3.3V, VDD2 = 3.3V,** Ta = 25℃)

Parameters	*Symbol*	*Min*	*Typ*	*Max*	*Unit*	*Comments*
Supply current	**NSI8120Nx**					
	I_{DD1}(Q0)		0.61	0.88	mA	All Input 0V for NSI812xN0 Or All Input at supply for NSI812xN1
	I_{DD2}(Q0)		1.24	1.79	mA	
	I_{DD1}(Q1)		2.28	3.01	mA	All Input at supply for NSI812xN0 Or All Input 0V for NSI812xN1
	I_{DD2}(Q1)		1.27	1.67	mA	
	I_{DD1}(1M)		1.45	1.92	mA	All Input with 1Mbps, C_L=15pF
	I_{DD2}(1M)		1.34	1.77	mA	
	I_{DD1}(10M)		1.52	2.01	mA	All Input with 10Mbps, C_L=15pF
	I_{DD2}(10M)		2.18	2.88	mA	
	I_{DD1}(100M)		1.87	2.52	mA	All Input with 100Mbps, C_L = 15pF
	I_{DD2}(100M)		8.76	11.83	mA	
	NSI8121Nx / NSI8122Nx					
	I_{DD1}(Q0)		1.03	1.34	mA	All Input 0V for NSI812xN0 Or All Input at supply for NSI812xN1
	I_{DD2}(Q0)		1.03	1.34	mA	
	I_{DD1}(Q1)		1.93	2.57	mA	All Input at supply for NSI812xN0 Or All Input 0V for NSI812xN1
	I_{DD2}(Q1)		1.93	2.57	mA	
	I_{DD1}(1M)		1.52	1.99	mA	All Input with 1Mbps, C_L=15pF
	I_{DD2}(1M)		1.52	1.99	mA	
	I_{DD1}(10M)		1.88	2.47	mA	All Input with 10Mbps, C_L=15pF
	I_{DD2}(10M)		1.88	2.47	mA	
	I_{DD1}(100M)		5.46	7.37	mA	All Input with 100Mbps, C_L = 15pF
	I_{DD2}(100M)		5.46	7.37	mA	

6.4. Supply Current Characteristics–2.5V Supply

(VDD1=2.5V± 10%, VDD2=2.5V± 10%, Ta=-40℃ to 125℃. Unless otherwise noted, Typical values are at **VDD1 = 2.5V, VDD2 = 2.5V,** Ta = 25℃)

Parameters	*Symbol*	*Min*	*Typ*	*Max*	*Unit*	*Comments*
Supply current	**NSI8120Nx**					
	I_{DD1}(Q0)		0.59	0.85	mA	All Input 0V for NSI812xN0 Or All Input at supply for NSI812xN1
	I_{DD2}(Q0)		1.21	1.74	mA	
	I_{DD1}(Q1)		2.24	2.94	mA	All Input at supply for NSI812xN0 Or All Input 0V for NSI812xN1
	I_{DD2}(Q1)		1.25	1.68	mA	
	I_{DD1}(1M)		1.42	1.88	mA	All Input with 1Mbps, C_L=15pF
	I_{DD2}(1M)		1.29	1.72	mA	
	I_{DD1}(10M)		1.50	1.97	mA	All Input with 10Mbps, C_L=15pF
	I_{DD2}(10M)		1.99	2.67	mA	
	I_{DD1}(100M)		1.81	2.44	mA	All Input with 100Mbps, C_L = 15pF
	I_{DD2}(100M)		7.23	9.76	mA	
	NSI8121Nx / NSI8122Nx					
	I_{DD1}(Q0)		1.00	1.33	mA	All Input 0V for NSI812xN0 Or All Input at supply for NSI812xN1
	I_{DD2}(Q0)		1.00	1.33	mA	
	I_{DD1}(Q1)		1.90	2.55	mA	All Input at supply for NSI812xN0 Or All Input 0V for NSI812xN1
	I_{DD2}(Q1)		1.90	2.55	mA	
	I_{DD1}(1M)		1.48	1.94	mA	All Input with 1Mbps, C_L=15pF
	I_{DD2}(1M)		1.48	1.94	mA	
	I_{DD1}(10M)		1.76	2.32	mA	All Input with 10Mbps, C_L=15pF
	I_{DD2}(10M)		1.76	2.32	mA	
	I_{DD1}(100M)		4.50	5.99	mA	All Input with 100Mbps, C_L = 15pF
	I_{DD2}(100M)		4.50	5.99	mA	

6.5. Switching Characteristics - 5V Supply

(VDD1=5V± 10%, VDD2=5V± 10%, Ta=-40℃ to 125℃. Unless otherwise noted, Typical values are at **VDD1 = 5V, VDD2 = 5V,** Ta = 25℃)

Parameters	Symbol	Min	Typ	Max	Unit	Comments
	NSI812xNx					
Data Rate	DR	0		150	Mbps	
Minimum Pulse Width	PW			5.0	ns	
Propagation Delay	t_{PLH}		9.9	18	ns	See Figure 6.7 , C_L = 15pF
	t_{PHL}		8.7	18	ns	See Figure 6.7 , C_L = 15pF
Pulse Width Distortion $\lvert t_{PHL} - t_{PLH} \rvert$	PWD			5.0	ns	See Figure 6.7 , C_L = 15pF
Rising Time	t_r			5.0	ns	See Figure 6.7 , C_L = 15pF
Falling Time	t_f			5.0	ns	See Figure 6.7 , C_L = 15pF
Peak Eye Diagram Jitter	t_{JIT}(PK)		2.5		ns	
Channel-to-Channel Delay Skew	t_{SK}(c2c)			2.5	ns	
Part-to-Part Delay Skew	t_{SK}(p2p)			5.0	ns	

6.6. Switching Characteristics - 3.3V Supply

(VDD1=3.3V± 10%, VDD2=3.3V± 10%, Ta=-40℃ to 125℃. Unless otherwise noted, Typical values are at **VDD1 = 3.3V, VDD2 = 3.3V,** Ta = 25℃)

Parameters	Symbol	Min	Typ	Max	Unit	Comments
	NSI812xNx					
Data Rate	DR	0		150	Mbps	
Minimum Pulse Width	PW			5.0	ns	
Propagation Delay	t_{PLH}		10.8	19	ns	See Figure 6.7 , C_L = 15pF
	t_{PHL}		9.6	19	ns	See Figure 6.7 , C_L = 15pF
Pulse Width Distortion $\lvert t_{PHL} - t_{PLH} \rvert$	PWD			5.0	ns	See Figure 6.7 , C_L = 15pF
Rising Time	t_r			5.0	ns	See Figure 6.7 , C_L = 15pF
Falling Time	t_f			5.0	ns	See Figure 6.7 , C_L = 15pF

Peak Eye Diagram Jitter	t_{JIT}(PK)		2.5		ns	
Channel-to-Channel Delay Skew	t_{SK}(c2c)			2.5	ns	
Part-to-Part Delay Skew	t_{SK}(p2p)			5.0	ns	

6.7. Switching Characteristics - 2.5V Supply

(VDD1=2.5V± 10%, VDD2=2.5V± 10%, Ta=-40℃ to 125℃. Unless otherwise noted, Typical values are at **VDD1 = 2.5V, VDD2 = 2.5V,** Ta = 25℃)

Parameters	*Symbol*	*Min*	*Typ*	*Max*	*Unit*	*Comments*
	NSI812xNx					
Data Rate	DR	0		150	Mbps	
Minimum Pulse Width	PW			5.0	ns	
Propagation Delay	t_{PLH}		12.0	20	ns	See Figure 6.7 , C_L = 15pF
	t_{PHL}		11.0	20	ns	See Figure 6.7 , C_L = 15pF
Pulse Width Distortion $\lvert t_{PHL} - t_{PLH} \rvert$	PWD			5.0	ns	See Figure 6.7 , C_L = 15pF
Rising Time	t_r			5.0	ns	See Figure 6.7 , C_L = 15pF
Falling Time	t_f			5.0	ns	See Figure 6.7 , C_L = 15pF
Peak Eye Diagram Jitter	t_{JIT}(PK)		2.5		ns	
Channel-to-Channel Delay Skew	t_{SK}(c2c)			2.5	ns	
Part-to-Part Delay Skew	t_{SK}(p2p)			5.0	ns	

6.8. Typical Performance Characteristics

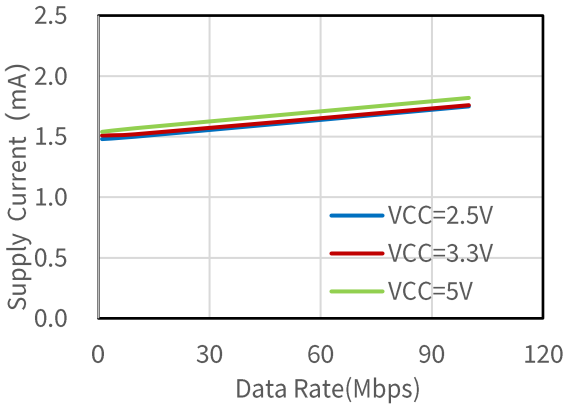


Figure 6.1 NSI8120Nx VDD1 Supply Current vs Data Rate

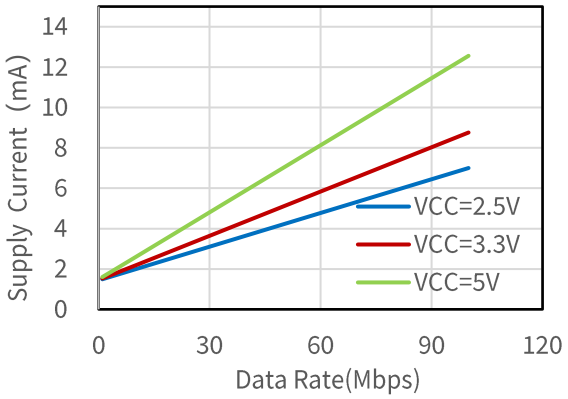


Figure 6.2 NSI8120Nx VDD2 Supply Current vs Data Rate

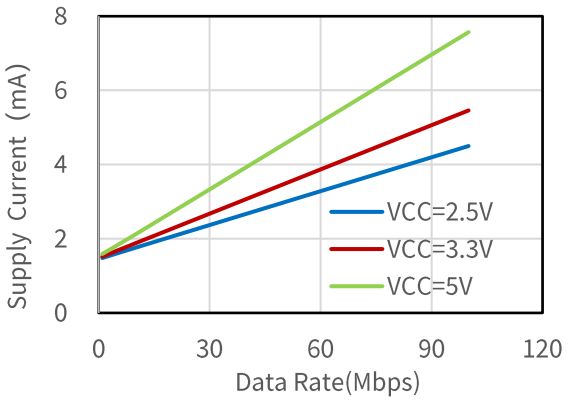


Figure 6.3 NSI8121Nx / NSI8122Nx VDD1 Supply Current vs Data Rate

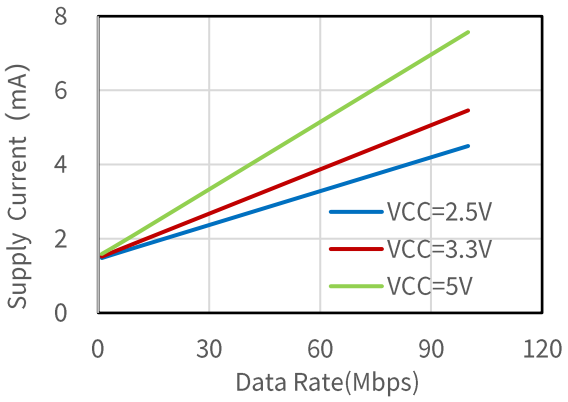


Figure 6.4 NSI8121Nx / NSI8122Nx VDD2 Supply Current vs Data Rate

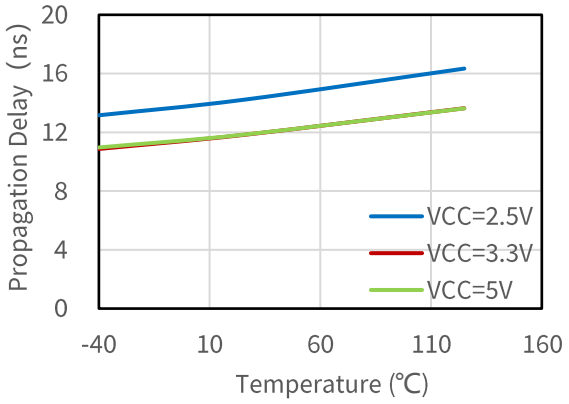


Figure 6.5 NSI812xNx Rising Edge Propagation Delay Vs Temp

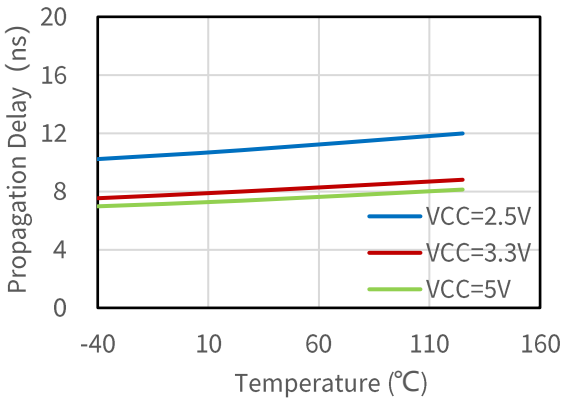
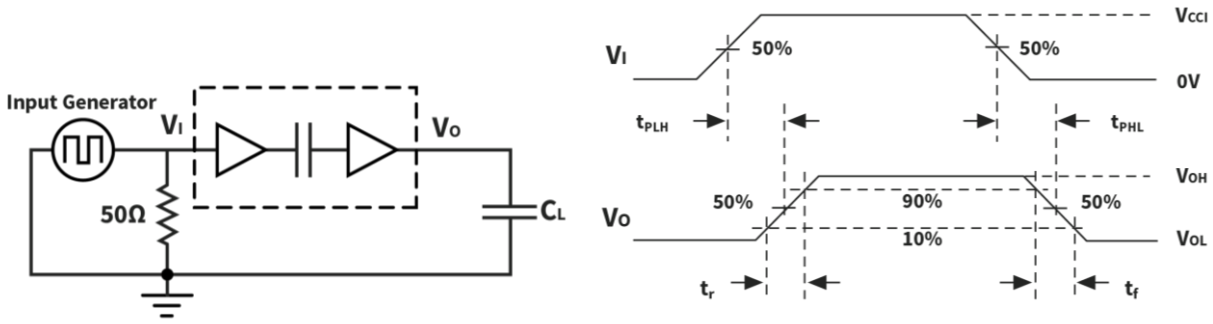


Figure 6.6 NSI812xNx Falling Edge Propagation Delay Vs Temp

6.9. Parameter Measurement Information



(1) Input Generator Characteristics : PRR ≤ 50kHz, tr ≤ 3ns, tf ≤ 3ns, Duty cycle = 50%, Zo = 50Ω.

Figure 6.7 Switching Characteristics Test Circuit and Waveform

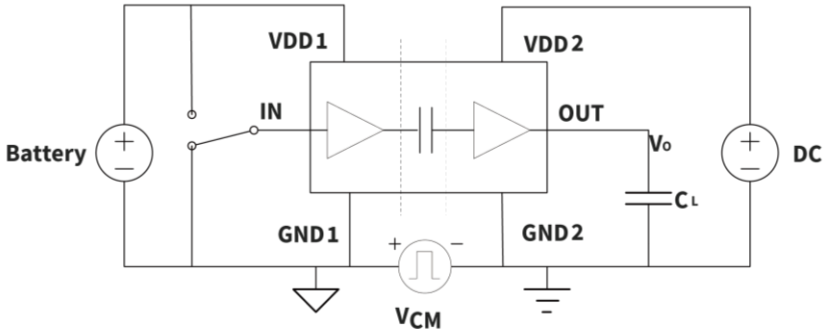


Figure 6.8 Common-Mode Transient Immunity Test Circuit

7. High Voltage Feature Description

7.1. Insulation and Safety Related Specifications

Parameters	*Symbol*	*Value* *SOP8*	*Unit*	*Comments*
Minimum External Clearance	CLR	4.0	mm	IEC 60664-1:2007
Minimum External Creepage	CPG	4.0	mm	IEC 60664-1:2007
Distance Through Insulation	DTI	10	um	
Tracking Resistance (Comparative Tracking Index)	CTI	>600	V	DIN EN 60112 (VDE 0303-11); IEC 60112
Material Group		Ⅰ		IEC 60664-1

Description	Test Condition	Value SOP8
Overvoltage Category per IEC60664-1	For Rated Mains Voltage ≤ 150Vrms	Ⅰ to Ⅳ
	For Rated Mains Voltage ≤ 300Vrms	Ⅰ to Ⅲ
	For Rated Mains Voltage ≤ 600Vrms	Ⅰ to Ⅱ
	For Rated Mains Voltage ≤ 1000Vrms	Ⅰ
Climatic Classification		40/125/21
Pollution Degree per DIN VDE 0110,		2

7.2. Insulation Characteristics

Description	Test Condition	Symbol	Value SOP8	Unit
Maximum repetitive isolation voltage		V_{IORM}	565	V_{PEAK}
Maximum Working Isolation Voltage	AC voltage	V_{IOWM}	400	V_{RMS}
	DC voltage		565	V_{DC}
Apparent Charge	Method a, after Input/output safety test subgroup 2/3, Vini=V_{IOTM}, t_{ini}= 60 s , $V_{pd(m)}$=1.2*V_{IORM}, t_m=10s.	q_{pd}		pC
	Method a, after environmental tests subgroup 1, Vini=V_{IOTM}, t_{ini}=60s ,$V_{pd(m)}$=1.6*V_{IORM}, t_m=10s			pC
	Method b, routine test (100% production) and preconditioning (type test);V_{ini}=1.2*V_{IOTM}, t_{ini}=1s $V_{pd\ (m)}$=1.875*V_{IORM}, t_m=1s （method b1） or $V_{pd(m)}$=Vini, t_m=t_{ini}(method b2)			pC
	Method a, after Input/output safety test subgroup 2/3, Vini=V_{IOTM}, t_{ini}= 60 s , $V_{pd(m)}$=1.2*V_{IORM}, t_m=10s.	q_{pd}	<5	pC
	Method a, after			pC

Description	Test Condition	Symbol	Value SOP8	Unit
	environmental tests subgroup 1, Vini=V_{IOTM}, t_{ini}=60s ,$V_{pd(m)}$=1.3*V_{IORM}, t_m=10s			
	Method b, routine test (100% production) and preconditioning (type test);V_{ini}=1.2*V_{IOTM}, t_{ini}=1s $V_{pd(m)}$=1.5*V_{IORM}, t_m=1s （method b1） or $V_{pd(m)}$=Vini, t_m=t_{ini}(method b2)			pC
Maximum transient isolation voltage	t = 60 sec	V_{IOTM}	5300	V_{PEAK}
Maximum Surge Isolation Voltage	Test method per IEC60065,1.2/50us waveform, $V_{IOSM} \geqslant V_{IMP} \times 1.3$	V_{IOSM}	5384	V_{PEAK}
Isolation resistance	V_{IO} =500V, T_{amb}=25℃	R_{IO}	>10^{12}	Ω
	V_{IO} =500V, 100℃ ≤ T_{amb}≤ 125℃		>10^{11}	Ω
	V_{IO} =500V, T_{amb}=T_s		>10^{9}	Ω
Isolation capacitance	f = 1MHz	C_{IO}	0.6	pF
Withstand Isolation Voltage	V_{TEST} = V_{ISO}, t = 60 s (qualification), V_{TEST} = 1.2 × V_{ISO}, t = 1 s (100% production test)	V_{ISO}	3750	V_{RMS}

7.3. Safety-Limiting Values

Basic isolation safety-limiting values as outlined in VDE-0884-17 of NSI812xNx SOP8(150mil)

Description	Test Condition	Value	Unit
Safety Supply Power	$R_{\theta JA}$ = 137.7 ℃/W, T J = 150 ℃, T A = 25 ℃	907	mW
Safety Supply Current	$R_{\theta JA}$ = 137.7 ℃/W, V I = 5.5 V, T J = 150 ℃, T A = 25 ℃	165	mA
Safety Temperature[2)]		150	℃

1) Calculate with the junction-to-air thermal resistance, $R_{\theta JA}$, of SOP8(150mil) package (***Thermal Information Table***) which is that of a device installed on a low effective thermal conductivity test board (1s) according to JESD51-3.

2) The maximum safety temperature has the same value as the maximum junction temperature (T_J) specified for the device.

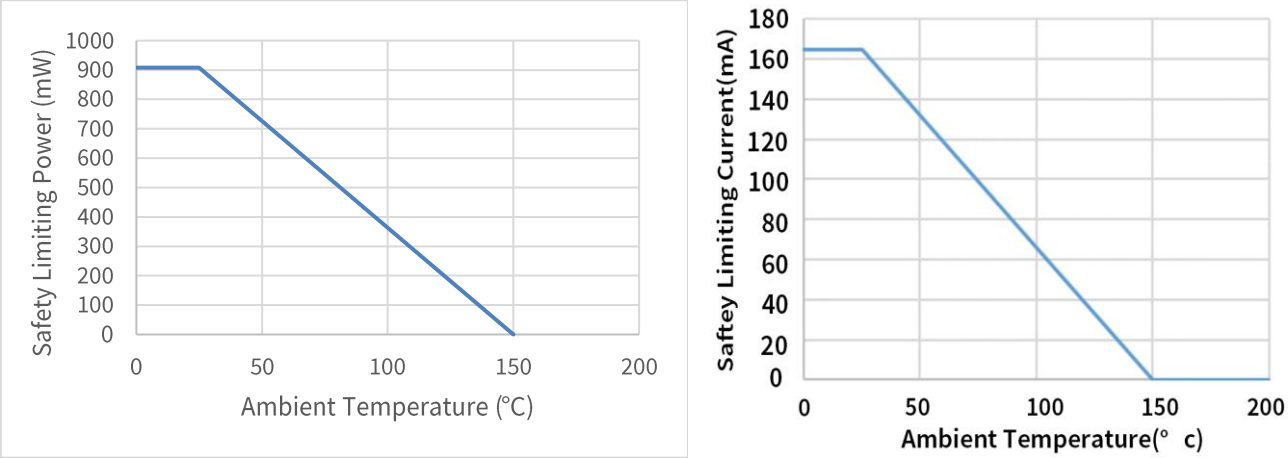


Figure 7.1 NSI812xNx Thermal Derating Curve, Dependence of Safety Limiting Values with Case Temperature per DIN VDE V 0884-17

7.4. Regulatory Information

The NSI812xNx are approved by the organizations listed in table.

UL		*VDE*	*CQC*
UL 1577 Component Recognition Program1	Approved under CSA Component Acceptance Notice 5A	DIN VDE V 0884-11:2017-012	Certified by CQC11-471543-2012 GB4943.1-2011
Single Protection, 3750Vrms Isolation voltage	Single Protection, 3750Vrms Isolation voltage	Basic Insulation 565Vpeak, VIOSM=5384Vpeak	Basic insulation
E500602	E500602	40050121	CQC19001233074

8. Function Description

8.1. Overview

The NSI812x is a Dual-channel digital isolator based on a capacitive isolation barrier technique. The digital signal is modulated with RF carrier generated by the internal oscillator at the Transmitter side. Then it is transferred through the capacitive isolation barrier and demodulated at the Receiver side.

The NSI812x devices are high reliability dual-channel digital isolator. The NSI812x device is safety certified by UL1577 support 5kV$_{rms}$ insulation withstand voltage, while providing high electromagnetic immunity and low emissions at low power consumption. The data rate of the NSI812x is up to 150Mbps, and the common-mode transient immunity (CMTI) is up to 200kV/us. The NSI812x device provides digital channel direction configuration and the default output level configuration when the input power is lost. Wide supply voltage of the NSI812x device support to connect with most digital interface directly, easy to do the level shift. High system level EMC performance enhance reliability and stability of use.

The NSI812x has a default output status when VDDIN is unready and VDDOUT is ready as shown in Table 8.1, which helps for diagnosis when power is missing at the transmitter side. The output B follows the same status with the input A within 60us after powering up.

Table 8.1 Output status vs. power status

Input[1]	***VDDIN status***	***VDDOUT status***	***Output***	***Comment***
H	Ready	Ready	H	Normal operation.
L	Ready	Ready	L	
X	Unready	Ready	L(NSI812xx0) H(NSI812xx1)	The output follows the same status with the input within 60us after input side VDD is powered on.
X	Ready	Unready	Undetermined	The output follows the same status with the input within 60us after output side VDD is powered on.

Note: H=Logic high; L=Logic low; X=Logic low or logic high

VDDIN is input side power; VDDOUT is output side power.

(1) There is a protection diode between the input and the VDDIN. When the VDDIN is floating, the strong drive signal through the input pin will put the VDDIN in an indeterminate state.

8.2. OOK Modulation

NSI812x is based on a capacitive isolation barrier technique and the digital signal is modulated with RF carrier generated by the internal oscillator at the transmitter side, as shown in Figure 8.1, then it is transferred through the capacitive isolation barrier and demodulated at the receiver side. The modulation uses OOK modulation technique with key benefits of high noise immunity and low radiation EMI.

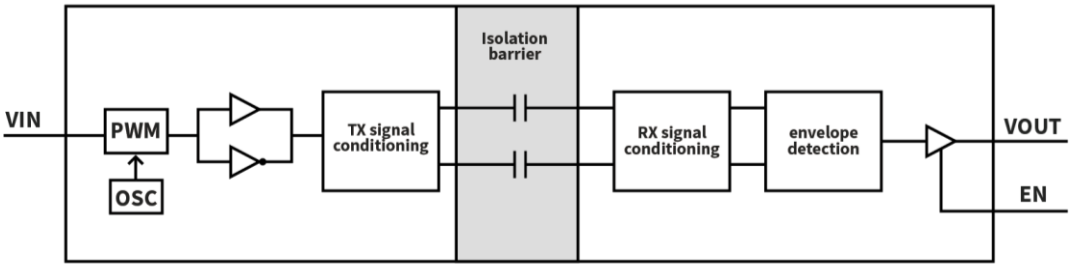


Figure 8.1 Single Channel Function Block Diagram

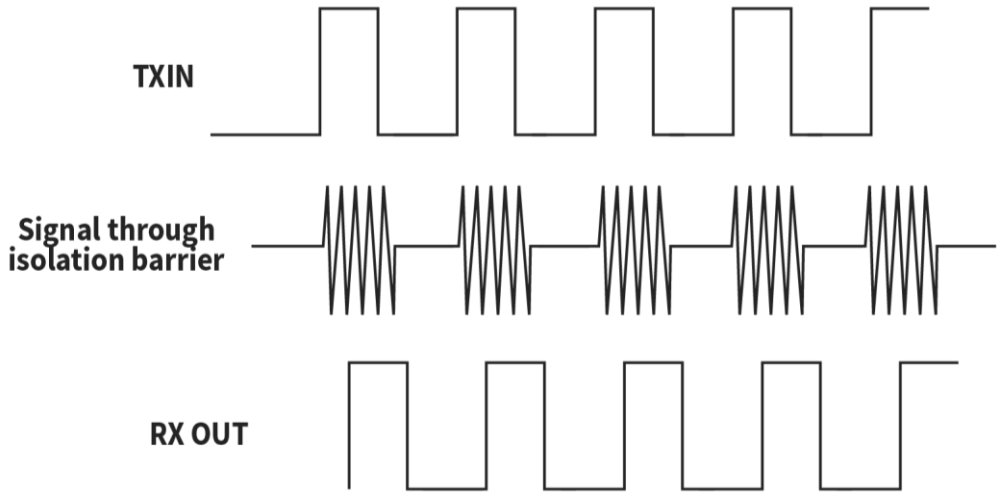


Figure 8.2 OOK Modulation

9. Application Note

9.1. Typical Application Circuit

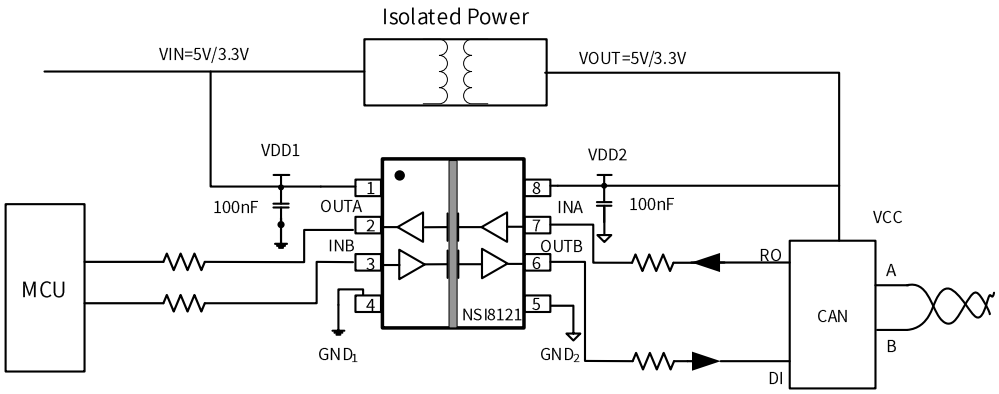


Figure9.1 Typical SCH for ISO CAN Interface

9.2. PCB Layout

The NSI812x requires a 0.1 µF bypass capacitor between VDD1 and GND1, VDD2 and GND2. The capacitor should be

placed as close as possible to the package. Figure 9.2 to Figure 9.3 show the recommended PCB layout, make sure the space under the chip should keep free from planes, traces, pads and via. To enhance the robustness of a design, the user may also include resistors (50–300 Ω) in series with the inputs and outputs if the system is excessively noisy. The series resistors also improve the system reliability such as latch-up immunity.

The typical output impedance of an isolator driver channel is approximately 50 Ω, ±40%. When driving loads where transmission line effects will be a factor, output pins should be appropriately terminated with controlled impedance PCB traces.

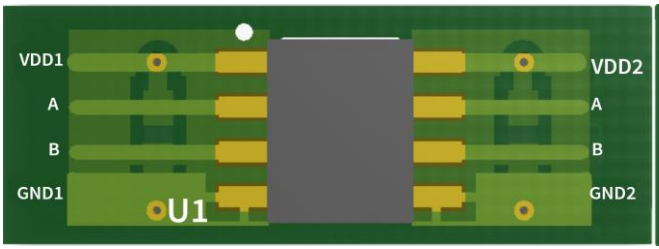


Figure 9.2 Recommended PCB Layout — Top Layer

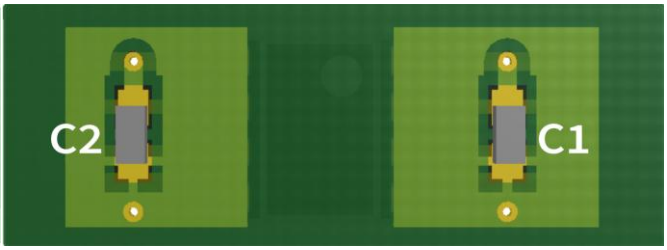


Figure 9.3 Recommended PCB Layout — Bottom Layer

9.3. High Speed Performance

Figure 9.4 shows the eye diagram of NSI812x at 50Mbps data rate output. The result shows a typical measurement on NSI812x with low jitter and wide open eye characteristics.

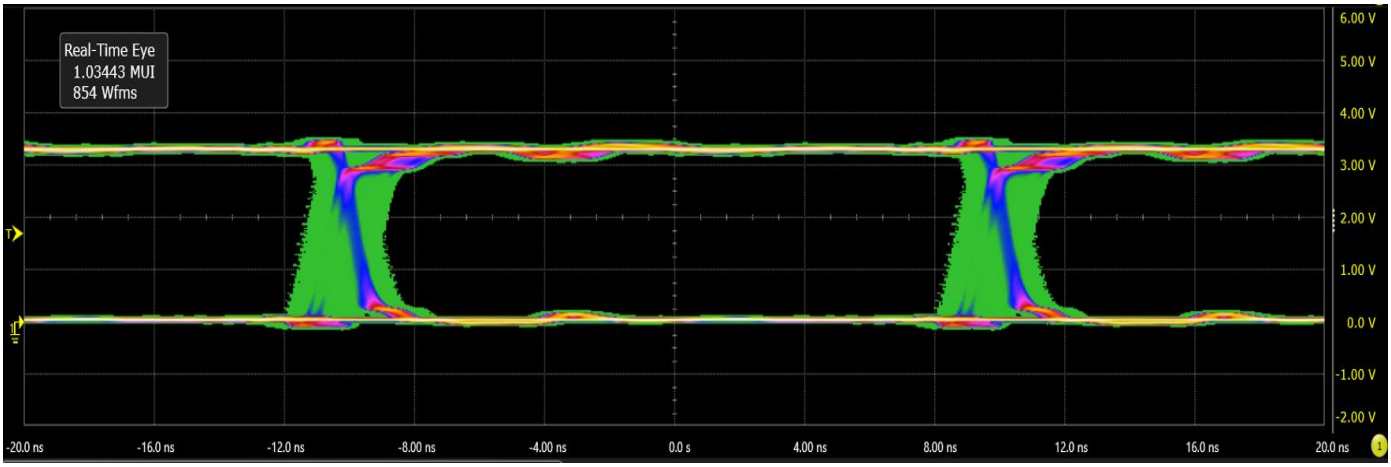
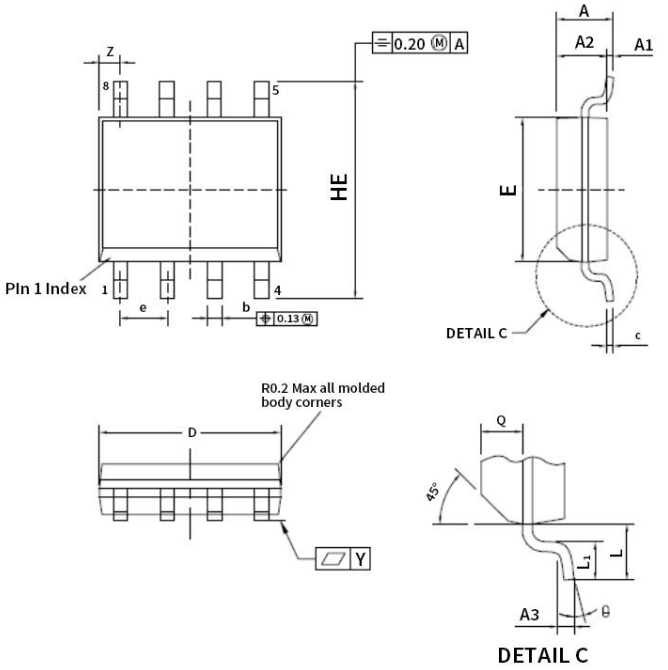


Figure9.4 Eye Diagram at 50Mbps PRBS 2^{16}-1, 2.5V and 25℃

10. Package Information

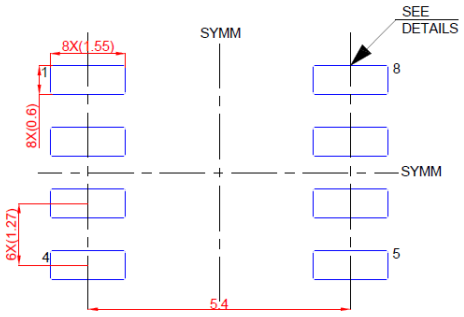


* CONTROLLING DIMENSION:MM

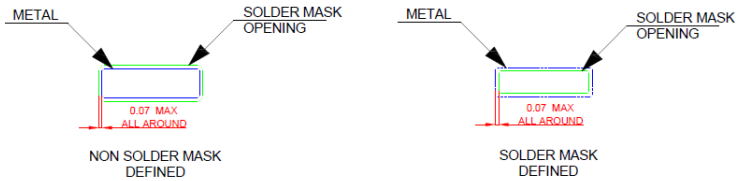
SYMBOL	MILLIMETER		
	MIN.	NOM.	MAX.
A	---	---	1.75
A1	0.10	---	0.25
A2	1.25	1.35	1.45
b	0.33	0.38	0.49
c	0.19	0.20	0.25
D	4.80	4.90	5.00
E	3.80	3.90	4.00
Q	0.60	0.65	0.70
HE	5.80	6.00	6.20
e	1.27 BSC		
L	1.05 BSC		
L1	0.40	0.64	1.00
Y	---	0.10	---
Z	0.3	0.5	0.7
A3	0.25 BSC		
θ	0°	5°	8°

NOTE: This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm, per side.

Figure 10.1 SOP8 Package Shape and Dimension in millimeters



LAND PATTERN EXAMPLE(mm)



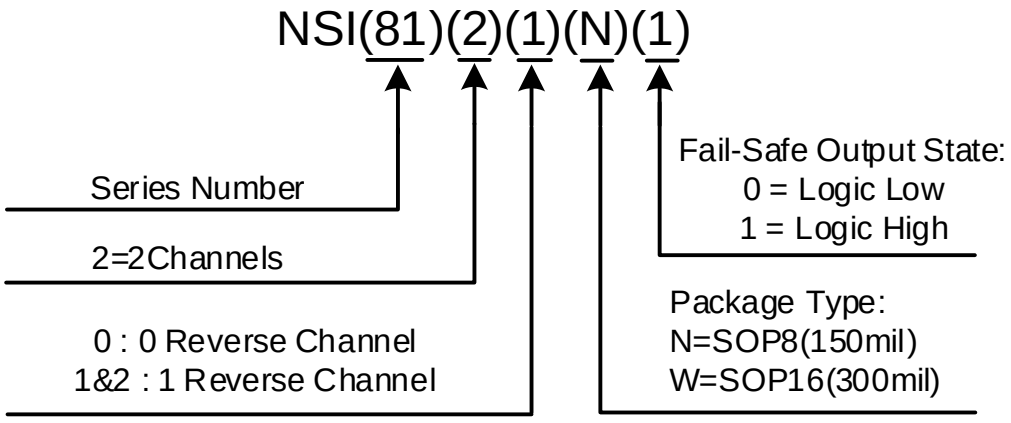
SOLDER MASK DETAILS

Figure 10.2 SOP8 Package Board Layout Example

11. Order Information

Part Number	Isolation Rating (kV)	Number of side 1 inputs	Number of side 2 inputs	Max Data Rate (Mbps)	Default Output State	Temperature	MSL	Package Type	Package Drawing	SPQ
NSI8120N0	3.75	2	0	150	Low	-40 to 125℃	3	SOP8 (150mil)	SOP8	2500
NSI8120N1	3.75	2	0	150	High	-40 to 125℃	3	SOP8 (150mil)	SOP8	2500
NSI8121N0	3.75	1	1	150	Low	-40 to 125℃	3	SOP8 (150mil)	SOP8	2500
NSI8121N1	3.75	1	1	150	High	-40 to 125℃	3	SOP8 (150mil)	SOP8	2500
NSI8122N0	3.75	1	1	150	Low	-40 to 125℃	3	SOP8 (150mil)	SOP8	2500
NSI8122N1	3.75	1	1	150	High	-40 to 125℃	3	SOP8 (150mil)	SOP8	2500
NOTE: All packages are RoHS-compliant with peak reflow temperatures of 260 ℃ according to the JEDEC industry standard classifications and peak solder temperatures.										

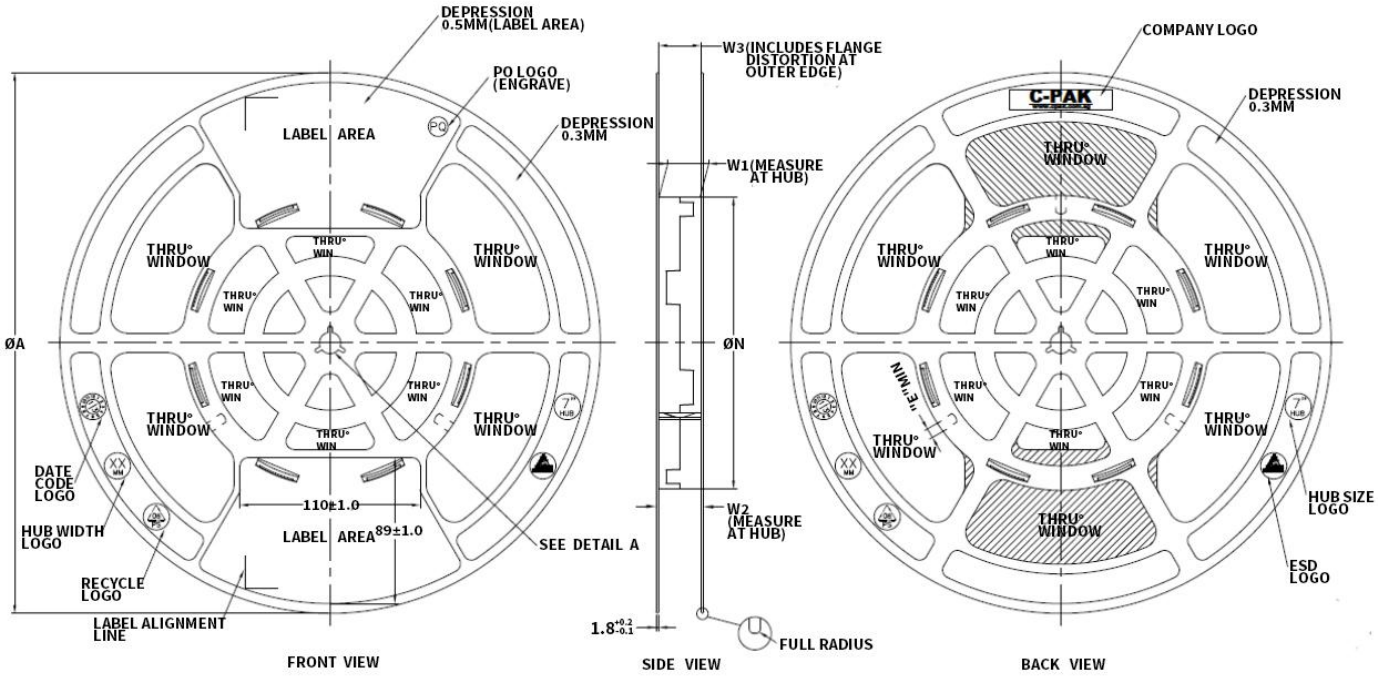
Part Number Rule:

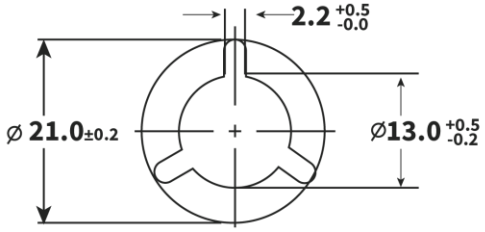


12. Documentation Support

Part Number	Product Folder	Datasheet	Technical Documents	Isolator selection guide
NSI812x	tbd	tbd	tbd	tbd

13. Tape and Reel Information



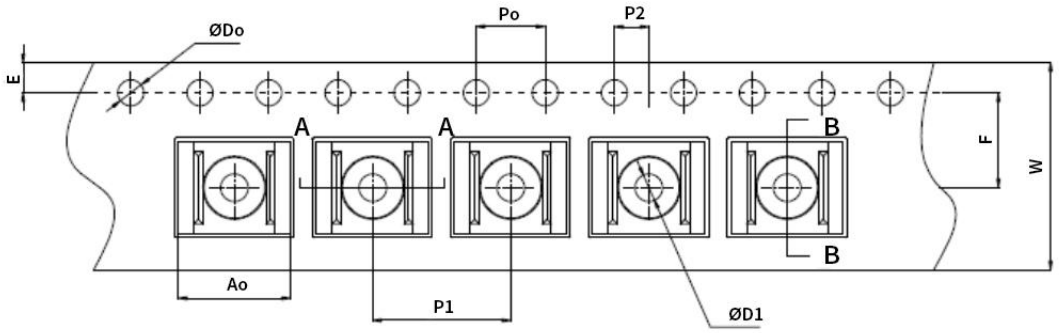


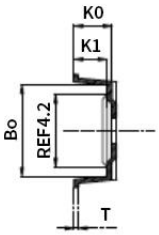
ARBOR HOLE
DETAIL A
SCALE: 3:1

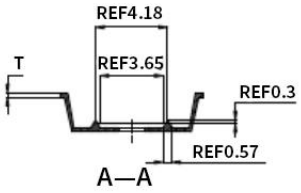
PRODUCT SPECIFICATION						
TAPE WIDTH	Ø A ±2.0	Ø N ±2.0	W1	W2 (Max)	W3	E (MIN)
08MM	330	178	8.4 +1.5 -0.0	14.4	SHALL ACCOMMODATE TAPE WIDTH WITHOUT NTERFERENCE	5.5
12MM	330	178	12.4 +2.0 -0.0	18.4		5.5
16MM	330	178	16.4 +2.0 -0.0	22.4		5.5
24MM	330	178	24.4 +2.0 -0.0	30.4		5.5
32MM	330	178	32.4 +2.0 -0.0	38.4		5.5

SURFACE RESISTIVITY			
LEGEND	SR RANGE	TYPE	COLOUR
A	BELOW 10^{12}	ANTISTATIC	ALL TYPES
B	10^{6} TO 10^{11}	STATIC DISSIPATIVE	BLACK ONLY
C	10^{5} & BELOW 10^{5}	CONDUCTIVE(GENERIC)	BLACK ONLY
E	10^{9} TO 10^{11}	ANTISTATIC(COATED)	ALL TYPES

Figure 13.1 Reel Information of SOP8(150mil)





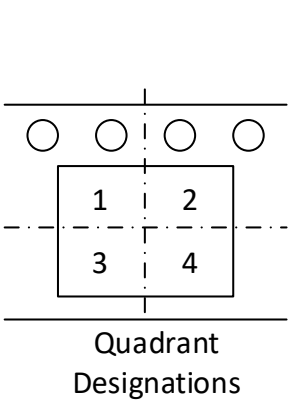


Common size

Appearance	Size(mm)
E	1.75±0.10
F	5.5±0.10
P2	2.00±0.10
D0	1.55±0.05
D1	1.6±0.10
P0	4.00±0.10
10P0	40.00±0.20

Pocket size

Appearance	Size(mm)
W	12.00±0.30
P_1	8.00±0.10
A_o	6.50±0.10
B_o	5.30±0.10
K_o	2.20±0.10
K_1	1.90±0.10
T	0.30±0.05



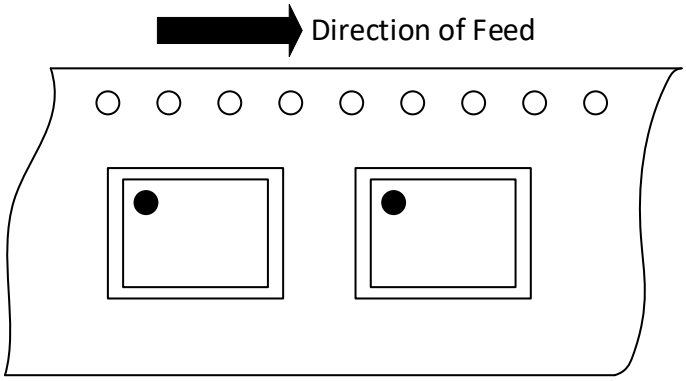


Figure 13.2 Tape Information of SOP8(150mil)

14. Revision History

Revision	Description	Date
1.0	Original	2017/11/15
1.1	Change to Ordering information	2018/3/26
1.2	Add maximum operation current specification.	2018/6/20
1.3	Change block diagram	2018/7/28
1.4	Correct Table 6.2 Pin No.	2018/8/20
1.5	Add specification “Input Pull high or low Current”	2018/9/10
1.6	Add “Maximum Input/Output Pulse Voltage”	2018/10/9
1.7	Change to Ordering information	2018/12/20
1.8	Change Certification Information	2019/06/17
1.9	Add Recommended operating conditions	2020/2/27
2.0	Update format	2021/2/25
2.1	Added MSL information	2021/3/28
2.2	changed tape and reel information of SOW16	2021/5/16
2.3	Correct part number, Change Storage Temperature	2021/11/17
2.4	Update Insulation and Safety Related Specifications, Regulatory Information, delete Isolation barrier life: >60 years, AEC-Q100.	2022/9/15
3.0	Correct formatting and images; Delete SOP16(300mil) package products; Update electrical characteristics; Update supply current characteristics at 2.5V/3.3V/5V. Update switching characteristics at 2.5V/3.3V/5V; Update high voltage feature description; Update function description; Update application note; Update eye diagram; Delete Typical Supply Current Equations; Update package information; Change MSL level;	2025/11/10

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