2.4GHz Zigbee Front-End Module

Features

2.4GHz ZigBee High Power Single-Chip, Single-Die RF Front-End IC

Combined TX / RX Transceiver Port and Single Antenna Port

2.4GHz Transmit High Power Amplifier with Harmonic Filter

Low Noise Amplifier

Transmit / Receive Switch Circuitry

High Transmit Signal Linearity Meeting Standards for OQPSK Modulation

Low Voltage (1.2V) CMOS Control Logic

ESD Protection Circuitry on All Ports

DC Decoupled RF Port

Low Noise Figure for the Receive Channel

Very Low DC Power Consumption

On-chip Matching Network

Minimal External Components Required

CMOS Technology

Applications

ZigBee Extended Range Devices

Wireless Sound and Audio Systems

Home and Industrial Automation

Custom 2.4GHz Radio Systems

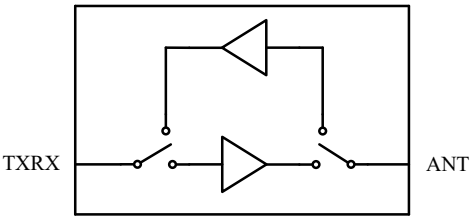


Figure1.1 Block Diagram

Package

QFN, 3 x 3 x 0.75mm, 16-pin

Pin description

Pin diagram

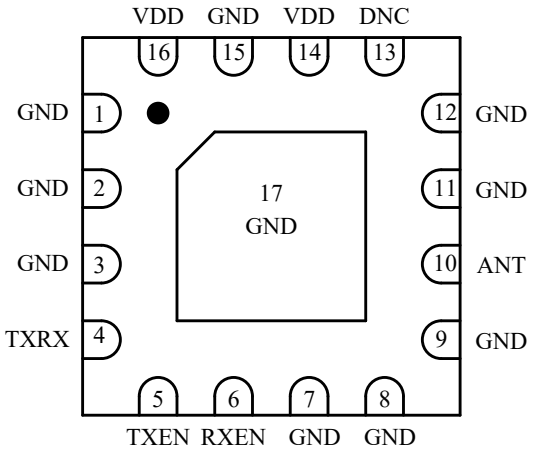


Figure2.1 Pin diagram

Pin description

Pin Number	Pin Name	Description
4	TXRX	RF signal to / from the Transceiver: DC shorted to GND
5	TXEN	Control TX Enable
6	RXEN	Control RX Enable
10	ANT	Antenna terminal; DC Shorted to GND
1,2,3,7,8,9, 11,12,15,17	GND	Ground – Must be connected to Ground in the Application Circuit
13	DNC	Reserved – Do Not Connect in the Application Circuit
14,16	VDD	Voltage Supply

Electrical Characteristics

Absolute Maximum Ratings

Parameters	Units	Min	Max	Conditions
DC VDD Voltage Supply	V	0	4.0	
DC Control Pin Voltage	V	0	3.6	Through 1Kohm resistor

DC VDD Current Consumption	mA		350	Through VDD Pins when TX is “ON”
DC Control Pin Current Consumption	µA		1	
TX RF Input Power	dBm		+5	All Operating Modes
ANT RF Input Power	dBm		+5	When RX is “ON”
Storage Ambient Temperature	℃	-50	+125	No RF and DC Voltages Applied Appropriate care required according to junction temperature

Note: Sustained operation at or above the Absolute Maximum Ratings for any one or combinations of the above parameters may result in permanent damage to the device and is not recommended. All maximum RF input power ratings assume 50-Ohm terminal impedance.

Recommended Operating Conditions

Parameters	Units	Min	Typ	Max	Conditions
DC VDD Voltage Supply	V	2.0	3.3	3.6	All VDD Pins
Control Voltage “High”	V	1.2		VDD	Through 1K resistor
Control Voltage “Low”	V	0		0.3	
Operating Ambient Temperature	℃	-40		+85	

Electrical specifications

Transmit Parameters

Parameters	Units	Typ	Conditions
Operating Frequency Band	GHz	2.4-2.525	All RF Pins Terminated by 50 Ohm
Saturated Output Power	dBm	+22	
Small-Signal Gain	dB	22	
Second Harmonic	dBm	-18	Pout=+20dBm
Third Harmonic	dBm	-25	Pout=+20dBm

Input Return Loss	dB	-17	
Output Return Loss	dB	-8	
RF Port Impedance	Ohm	50	
TX Quiescent Current	mA	17.5	No RF Applied
TX High Power Current	mA	130	Pout=+20dBm

Receive Technical Parameters

Parameters	**Units**	**Typ**	**Conditions**
Operating Frequency Band	GHz	2.4-2.525	All RF Pins Terminated by 50 Ohm
Gain	dB	14	
Noise Figure	dB	2.7	
Input Return Loss	dB	-25	
Output Return Loss	dB	-15	
RF Port Impedance	Ohm	50	
RX Quiescent Current	mA	10.5	No RF Applied
Input P_{1dB}	dBm	-12	At ANT Pin

Standby Mode Technical Paramters

Parameters	**Units**	**Typ**	**Conditions**
DC Shutdown Current	μA	<1	
TXRX-ANT Insertion Loss (S21)	dB	-50	Pin<-20dBm
ANT-TXRX Insertion Loss (S21)	dB	-50	Pin<-20dBm
Return Loss (S11)	dB	-1.5	From TXRX Port
Transmit-Receive Switching Time	nsec	800	
Shut-Down and “ON” State Switching Time	nsec	800	

Control Logic

TXEN	RXEN	Operating Conditions
1	X	TX Active
0	1	RX Active
0	0	Shut-down

Note：

“1” denotes high voltage state (>1.2V) at Control Pins

“0” denotes low voltage state (<0.3V) at Control Pins

“X” denotes do not care：either “1” or “0” can be applied

Application Circuit

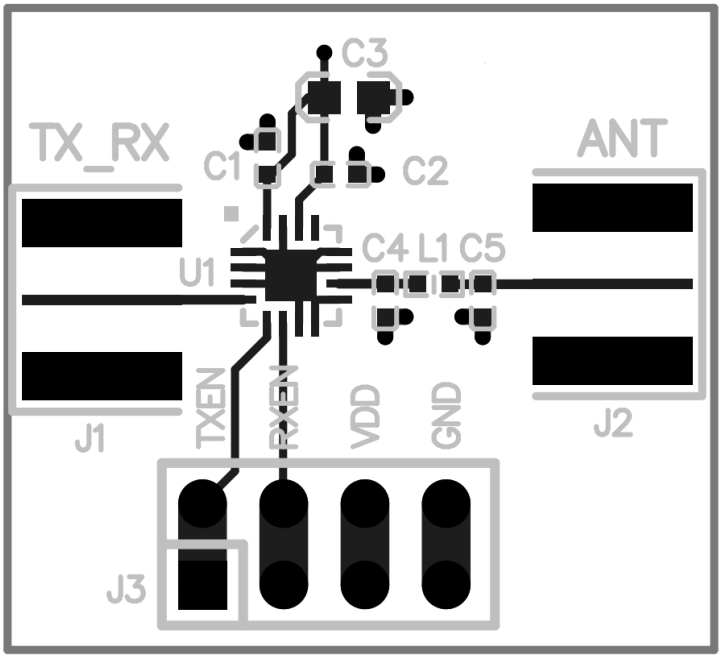


Figure 4.1 Evaluation Board RFX2401C

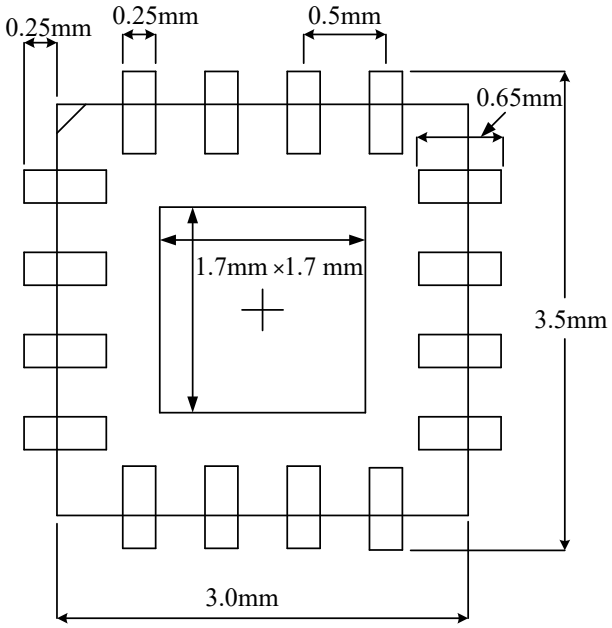


Figure4.2 PCB Land Pattern

Application Circuit 1 (Maximum Output Power)

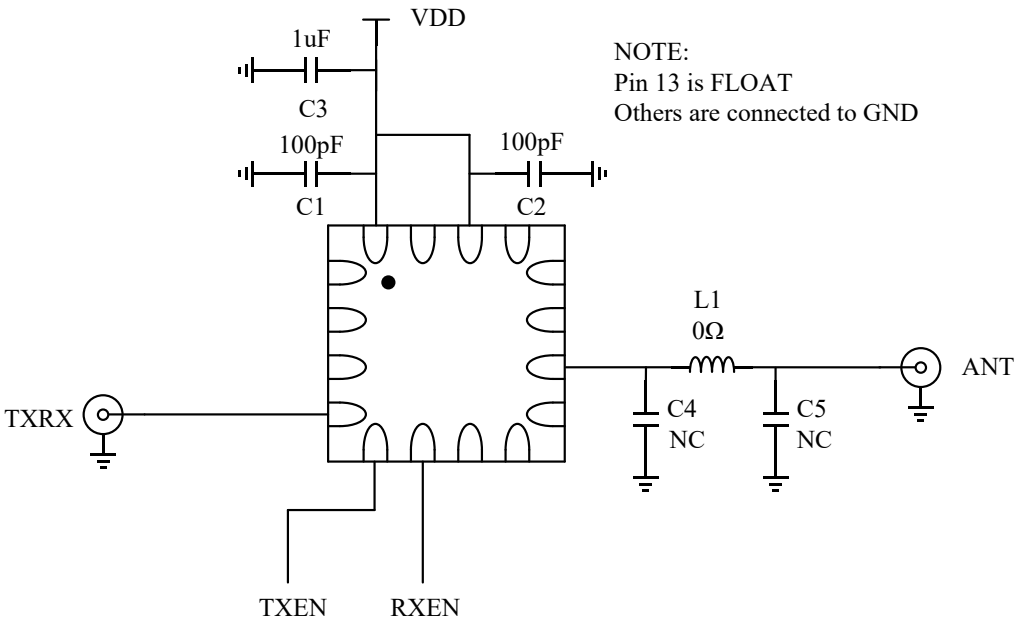


Figure4.3 Application Circuit 1

Application Circuit 2 (Best Harmonic Characteristic)

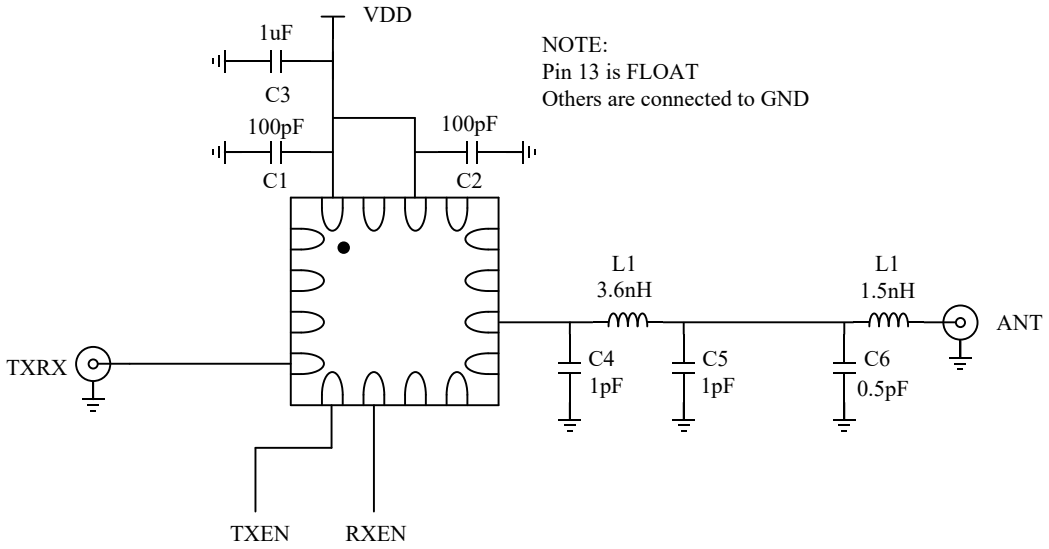


Figure4.4 Application Circuit 2

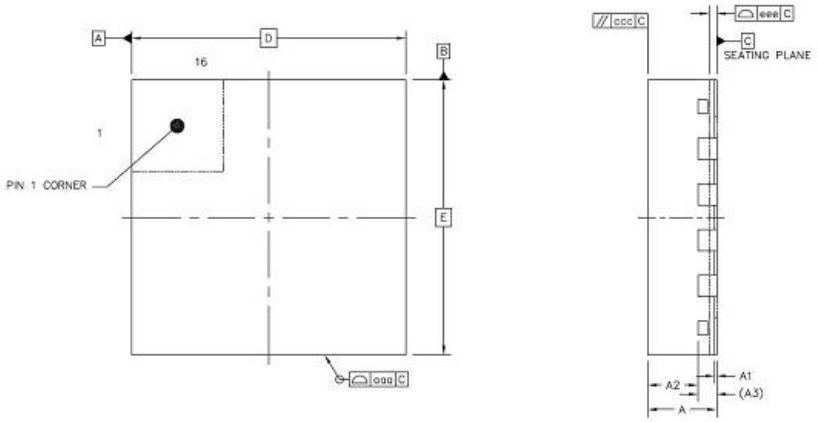
Package

Package Marking

Part Number	Marking
RFX2401C	2401C

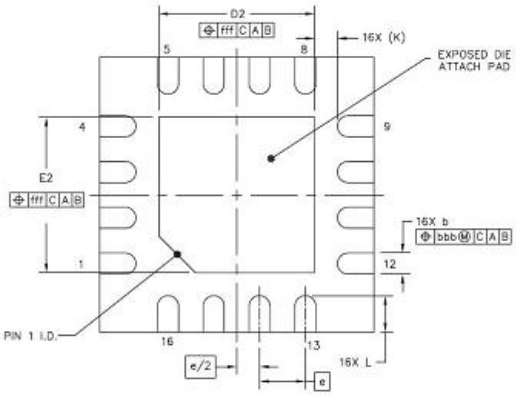
Package Dimensions

3 x 3 x 0.75mm Small Outline QFN-16 Package with Exposed Ground Pad.



TOP VIEW

SIDE VIEW



BOTTOM VIEW

		SYMBOL	MIN	NOM	MAX
TOTAL THICKNESS		A	0.7	0.75	0.8
STAND OFF		A1	0	0.02	0.05
MOLD THICKNESS		A2	---	0.55	---
L/F THICKNESS		A3		0.203 REF	
LEAD WIDTH		b	0.18	0.23	0.28
BODY SIZE	X	D		3 BSC	
	Y	E		3 BSC	
LEAD PITCH		e		0.5 BSC	
EP SIZE	X	D2	1.6	1.7	1.8
	Y	E2	1.6	1.7	1.8
LEAD LENGTH		L	0.3	0.4	0.5
LEAD TIP TO EXPOSED PAD EDGE		K		0.275 REF	
PACKAGE EDGE TOLERANCE		aaa		0.1	
MOLD FLATNESS		ccc		0.1	
COPLANARITY		eee		0.08	
LEAD OFFSET		bbb		0.1	
EXPOSED PAD OFFSET		fff		0.1	

Chip Soldering and Storage

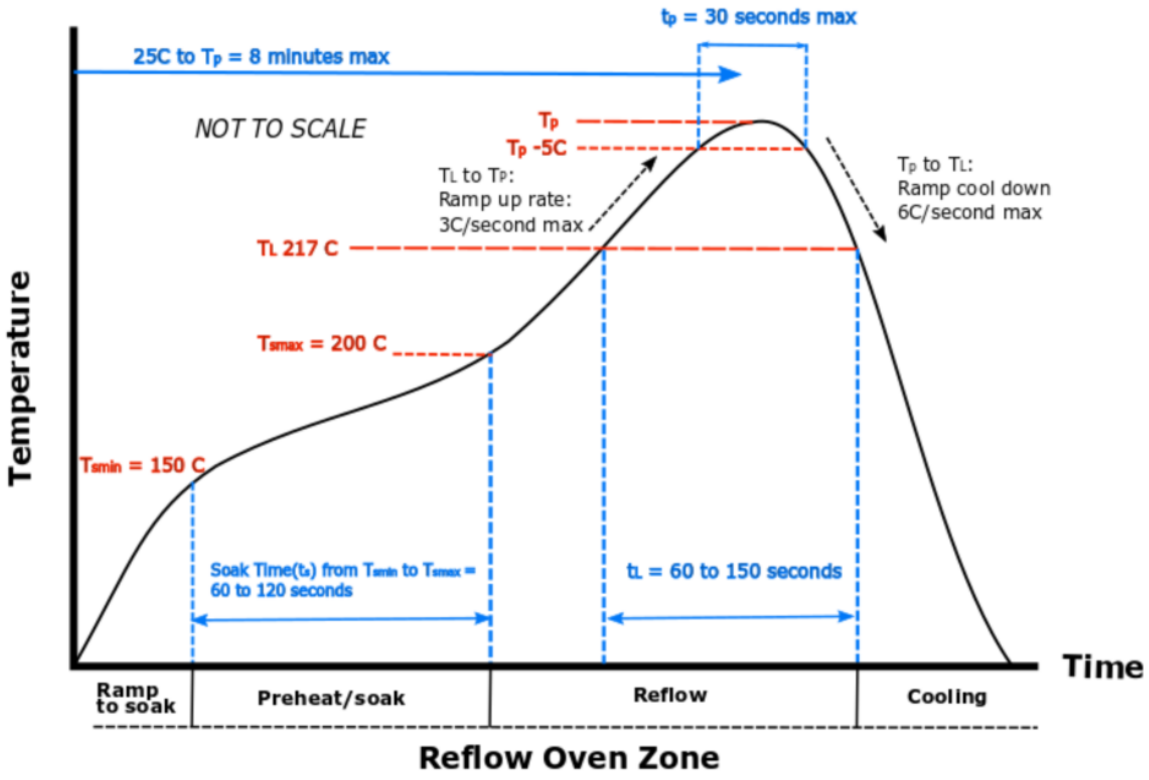
Moisture sensitivity level:

Moisture Sensitivity Level (MSL): Level 3

MSL, please refer to the IPC/JEDEC J-STD-020 standard.

Reflow soldering curve:

Refer to IPC/JEDEC J-STD-020 standard



Lead-free soldering process:

1. Preheat the temperature zone to 150℃-200℃ and maintain it for 60s-120s;

2. Reflow temperature > 217℃, duration 60s-150s;

Temperature rise slope: from the reflux temperature (217℃) to the peak temperature range, the temperature rise slope is ≤3℃/S;

Cooling rate: Within the range from peak temperature to reflow temperature of 217℃, the cooling rate is ≤6℃/S;

3. The peak set temperature should not exceed 260℃, and the actual temperature should also not

exceed 260℃. The total time from the highest temperature to a decrease of 5℃ should not exceed 30 seconds

4. Time from normal temperature (25℃) to peak temperature: ≤8 minutes;

5. The number of reflow soldering cycles for the chip shall be no more than 3;

The reflow soldering time can be set based on various factors such as equipment model, equipment lifespan, number of temperature zones, heating method, PCB board thickness, solder paste model, heat resistance of electronic components, solder paste glossiness after soldering, and stencil condition. Proper adjustments to temperature and chain speed can be made within the conditions specified in Table 5-2 of J-STD-020. The temperature process parameters set for each product and its corresponding equipment should be unique.

- Furnace temperature testing frequency: Furnace temperature testing is required when switching products, and it should be conducted at least every 24 hours during continuous production;
- The reflow oven should undergo a temperature stability verification assessment at least once a year;
- The lifespan of the temperature measurement board is recommended to be 50-100 uses;
- The temperature measuring instrument needs to be calibrated regularly;
- When considering the slope of temperature rise and fall, it is important to ensure that the chain speed and statistical time interval are reasonable.

Key points of temperature measurement:

1. Perform operations at 3-7 locations on the substrate;

2. In areas with high/low component loading density;

3. At or near the location of components with large heat capacity;

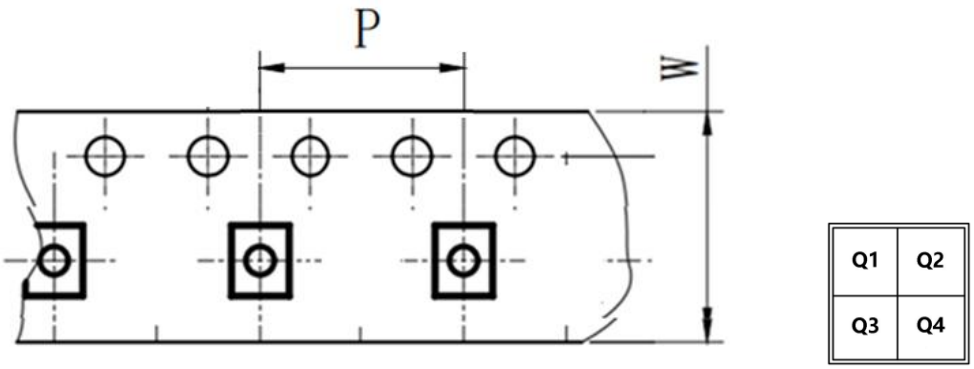
4. For component leads and physical surfaces with weaker heat resistance (IC/electrolytic capacitors);

5. To accurately measure the peak temperature of the package, refer to the thermocouples recommended in JEP140.

Packaging and transportation

Packaging

The chip is packaged in vacuum tape packaging, featuring moisture-proof and anti-static properties. It is compatible with major pick-and-place machines in the industry during use. The minimum packaging is 3000 pieces per tray.



W=12.0mm，P=8.0mm，PIN1 orientation: Q1

ESD protection

Please take precautions against static electricity and moisture during the transportation and production of chips.