

1. General Description

The 74HC373; 74HCT373 is an 8-bit D-type transparent latch with 3-state outputs. The device features latch enable (LE) and output enable ($\overline{OE}$) inputs. When LE is HIGH, data at the inputs enter the latches. In this condition the latches are transparent, a latch output will change each time its corresponding D-input changes. When LE is LOW the latches store the information that was present at the inputs a set-up time preceding the HIGH-to-LOW transition of LE. A HIGH on $\overline{OE}$ causes the outputs to assume a high-impedance OFF-state. Operation of the $\overline{OE}$ input does not affect the state of the latches. Inputs include clamp diodes. This enables the use of current limiting resistors to interface inputs to voltages in excess of V_{CC} .

2. Features and Benefits

- Wide operating voltage 2.0 V to 6.0 V
- High noise immunity
- CMOS low power dissipation
- Latch-up performance exceeds 250 mA
- Input levels:
 - For 74HC373: CMOS level
 - For 74HCT373: TTL level
- 3-state non-inverting outputs for bus-oriented applications
- Common 3-state output enable input
- Complies with JEDEC standards:
 - JESD8C (2.7 V to 3.6 V)
 - JESD7A (2.0 V to 6.0 V)
- ESD protection:
 - HBM: ANSI/ESDA/JEDEC JS-001 class 2 exceeds 2000 V
 - CDM: ANSI/ESDA/JEDEC JS-002 Class C3 exceeds 2000 V
- Multiple package options
- Specified from -40 °C to +85 °C and from -40 °C to +125 °C

74HC373; 74HCT373



Octal D-type transparent latch; 3-state

Draft datasheet, Rev. 1.0

Aug 08, 2024

3. Ordering Information

Table 1. Ordering information

Type number	Package		
	Name	Description	Quantity
74HC373D	SOP-20L	plastic small outline package; 20 leads; body width 7.5 mm	3000
74HCT373D			
74HC373PW	TSSOP20L	plastic thin shrink small outline package; 20 leads; body width 4.4 mm	3000
74HCT373PW			

4. Function Diagram

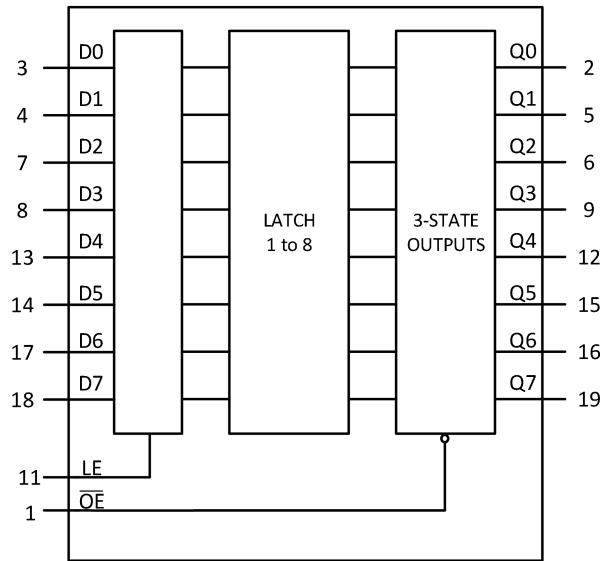


Fig. 1. Functional diagram

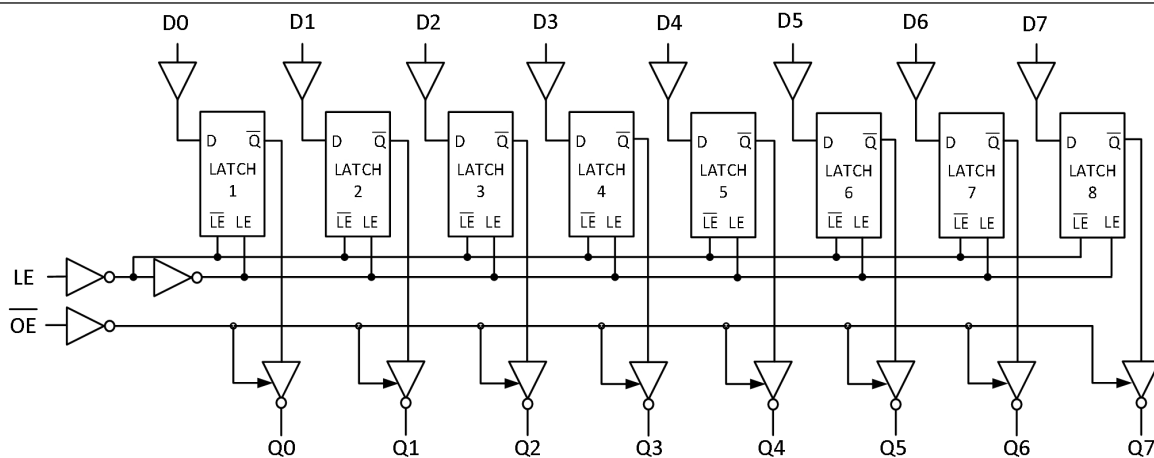
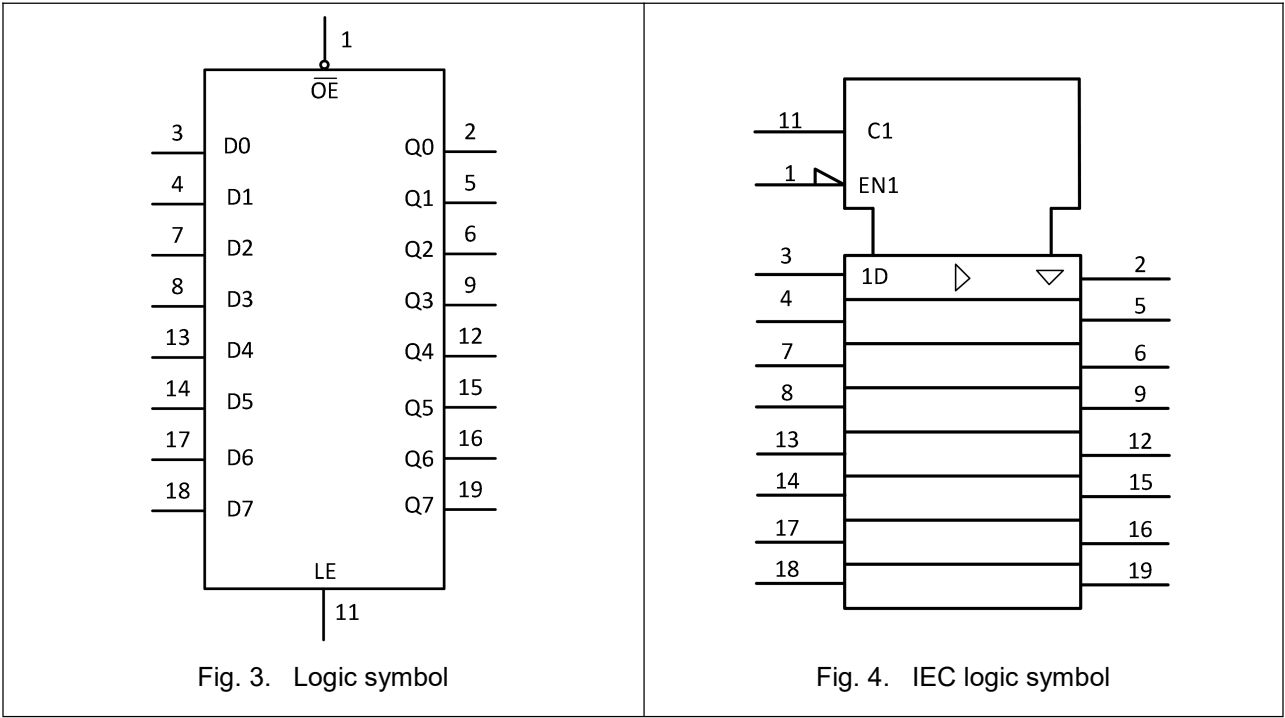
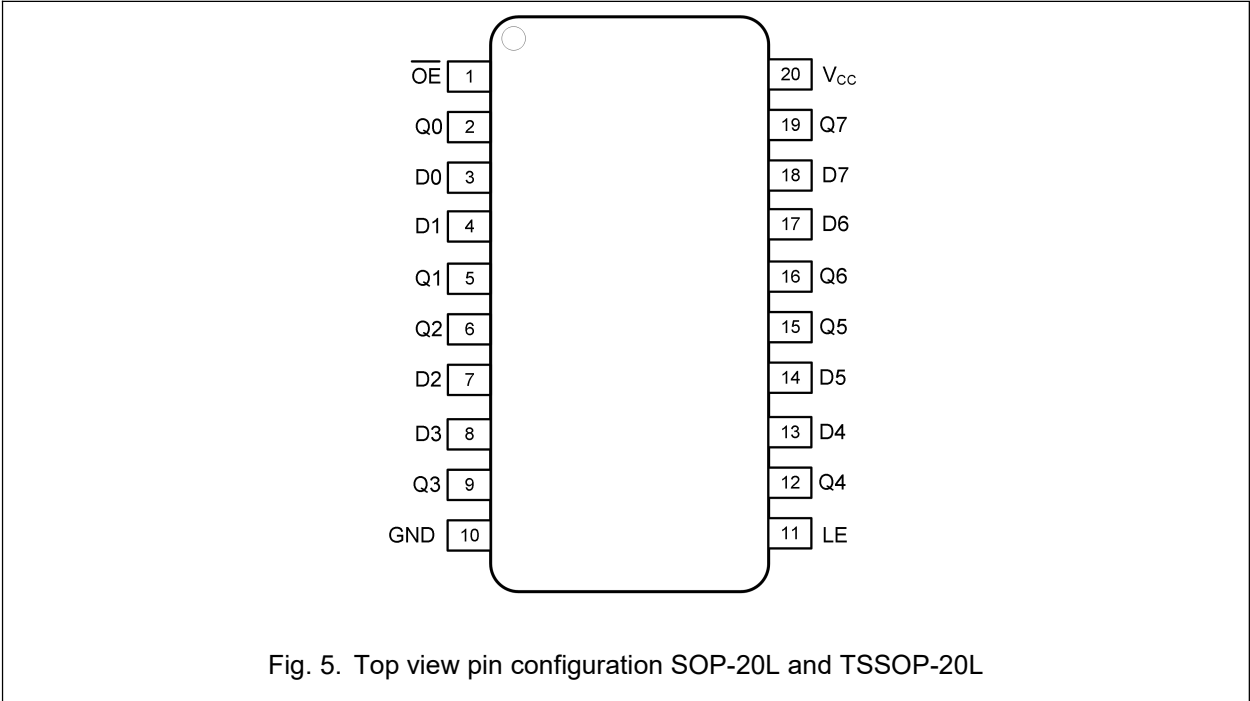


Fig. 2. Logic diagram



5. Pinning Information

5.1. Pinning



5.2. Pin description

Table 2. Pin description

Symbol	Pin	Description
$\overline{OE}$	1	3-state output enable input (active LOW)
Q0, Q1, Q2, Q3, Q4, Q5, Q6, Q7	2, 5, 6, 9, 12, 15, 16, 19	3-state latch output
D0, D1, D2, D3, D4, D5, D6, D7	3, 4, 7, 8, 13, 14, 17, 18	data input
GND	10	ground (0 V)
LE	11	latch enable input (active HIGH)
V _{CC}	20	supply voltage

6. Functional Description

Table 3. Function table

H = HIGH voltage level; h = HIGH voltage level one set-up time prior to the LOW-to-HIGH clock transition;
 L = LOW voltage level; l = LOW voltage level one set-up time prior to the LOW-to-HIGH clock transition; X
 = don't care; Z = high-impedance OFF-state.

Operating modes	Control		Input	Internal latches	Outputs
	$\overline{OE}$	LE	Dn		Qn
Enable and read register (transparent mode)	L	H	L	L	L
			H	H	H
Latch and read register	L	L	l	L	L
			h	H	H
Latch register and disable outputs	H	X	X	X	Z

7. Absolute Maximum Ratings

Stresses exceeding the absolute maximum ratings may damage the device. The device may not function or be operable above the recommended operating conditions and stressing the parts to these levels is not recommended. In addition, extended exposure to stresses above the recommended operating conditions may affect device reliability. The absolute maximum ratings are stress ratings only.

Table 5. Absolute Maximum Ratings

In accordance with the Absolute Maximum Rating System (IEC 60134). Voltages are referenced to GND.

Symbol	Parameter	Conditions	Min	Max	Unit
V_{CC}	supply voltage		-0.5	7	V
I_{IK}	input clamping current	$V_I < -0.5\text{ V}$ or $V_I > V_{CC} + 0.5\text{ V}$		± 20	mA
I_{OK}	output clamping current	$V_O < -0.5\text{ V}$ or $V_O > V_{CC} + 0.5\text{ V}$		± 20	mA
I_O	output current	$-0.5\text{ V} < V_O < V_{CC} + 0.5\text{ V}$		± 35	mA
I_{CC}	supply current			70	mA
I_{GND}	ground current		-70		mA
P_{tot}	total power dissipation	$T_{amb} = -40\text{ }^{\circ}\text{C}$ to $+125\text{ }^{\circ}\text{C}$		500	mW
T_{stg}	storage temperature		-65	+150	$^{\circ}\text{C}$

8. Recommended Operating Conditions

The Recommended Operating Conditions table defines the conditions for actual device operation. Recommended operating conditions are specified to ensure optimal performance to the datasheet specifications. EnergyMath does not recommend exceeding them or designing to Absolute Maximum Ratings.

Table 6. Recommended Operating Conditions

Symbol	Parameter	Conditions	74HC373			74HCT373			Unit
			Min	Min	Typ	Min	Min	Typ	
V_{CC}	supply voltage		2.0	5.0	6.0	4.5	5.0	5.5	V
V_I	input voltage		0		V_{CC}	0		V_{CC}	V
V_O	output voltage		0		V_{CC}	0		V_{CC}	V
T_{amb}	ambient temperature		-40	+25	+125	-40	+25	+125	$^{\circ}\text{C}$
$\Delta t/\Delta V$	input transition rise and fall rate	$V_{CC} = 2.0\text{ V}$			625				ns/V
		$V_{CC} = 4.5\text{ V}$		1.67	139		1.67	139	ns/V
		$V_{CC} = 6.0\text{ V}$			83				ns/V

9.Static Characteristics

Table 6. Static characteristics

At recommended operating conditions. Voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions	-40 °C to +85 °C			-40 °C to +125 °C		Unit
			Min	Typ[1]	Max	Min	Max	
74HC373								
V _{IH}	HIGH-level input voltage	V _{CC} = 2.0 V	1.5			1.5		V
		V _{CC} = 4.5 V	3.15			3.15		V
		V _{CC} = 6.0 V	4.2			4.2		V
V _{IL}	LOW-level input voltage	V _{CC} = 2.0 V			0.5		0.5	V
		V _{CC} = 4.5 V			1.35		1.35	V
		V _{CC} = 6.0 V			1.8		1.8	V
V _{OH}	HIGH-level output voltage	V _I = V _{IH} or V _{IL}						
		I _O = -20μA; V _{CC} = 2.0 V	1.9			1.9		V
		I _O = -20μA; V _{CC} = 4.5 V	4.4			4.4		V
		I _O = -20μA; V _{CC} = 6.0 V	5.9			5.9		V
		I _O = -6.0 mA; V _{CC} = 4.5 V	3.84			3.7		V
		I _O = -7.8 mA; V _{CC} = 6.0 V	5.34			5.2		V
V _{OL}	LOW-level output voltage	V _I = V _{IH} or V _{IL}						
		I _O = 20μA; V _{CC} = 2.0 V			0.1		0.1	V
		I _O = 20μA; V _{CC} = 4.5 V			0.1		0.1	V
		I _O = 20μA; V _{CC} = 6.0 V			0.1		0.1	V
		I _O = 6.0 mA; V _{CC} = 4.5 V			0.33		0.4	V
		I _O = 7.8 mA; V _{CC} = 6.0 V			0.33		0.4	V
I _I	input leakage current	V _I = V _{CC} or GND ; V _{CC} = 6.0 V			±1		±1	μA
I _{OZ}	OFF-state output current	V _I = V _{IH} or V _{IL} ; V _{CC} = 6.0V ; V _O = V _{CC} or GND			±5		±10	μA
I _{CC}	supply current	V _I = V _{CC} or GND ; I _O = 0A ; V _{CC} = 6.0 V			20		40	μA
C _I	input capacitance			6.5				pF

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Octal D-type transparent latch; 3-state

Symbol	Parameter	Conditions	-40 °C to +85 °C			-40 °C to +125 °C		Unit
			Min	Typ[1]	Max	Min	Max	
74HCT373								
V _{IH}	HIGH-level input voltage	V _{CC} = 4.5 V to 5.5 V	2.0			2.0		V
V _{IL}	LOW-level input voltage	V _{CC} = 4.5 V to 5.5 V			0.8		0.8	V
V _{OH}	HIGH-level output voltage	V _I = V _{IH} or V _{IL}						
		I _O = -20µA; V _{CC} = 4.5 V	4.4			4.4		V
		I _O = -6.0 mA; V _{CC} = 4.5 V	3.84			3.7		V
V _{OL}	LOW-level output voltage	V _I = V _{IH} or V _{IL}						
		I _O = 20µA; V _{CC} = 4.5 V			0.1		0.1	V
		I _O = 6.0 mA; V _{CC} = 4.5 V			0.33		0.4	V
I _I	input leakage current	V _I = V _{CC} or GND ; V _{CC} = 5.5 V			±1		±1	µA
I _{OZ}	OFF-state output current	V _I = V _{IH} or V _{IL} ; V _{CC} = 5.5 V ; V _O = V _{CC} or GND			±5		±10	µA
I _{CC}	supply current	V _I = V _{CC} or GND ; I _O = 0 A ; V _{CC} = 5.5 V			20		40	µA
ΔI _{CC}	additional supply current	per pin ; V _I = V _{CC} - 2.1 V; I _O = 0 A; other inputs at V _{CC} or GND; V _{CC} = 4.5 V to 5.5 V			300		350	µA
C _I	input capacitance			6.5				pF

[1]All typical values are measured at $T_{amb} = 25^\circ\text{C}$.

10. Dynamic Characteristics

Table 7. Dynamic characteristics

Voltages are referenced to GND (ground = 0 V); for test circuit see Fig. 10.

Symbol	Parameter	Conditions	-40 °C to +85 °C			-40 °C to +125 °C		Unit
			Min	Typ[1]	Max	Min	Max	
74HC373								
t _{pd}	propagation delay	Dn to Qn; see Fig. 6 [2]						
		V _{CC} = 2.0 V			30		40	ns
		V _{CC} = 4.5 V			20		25	ns
		V _{CC} = 6.0 V			15		18	ns
		LE to Qn; see Fig. 7 [3]						
		V _{CC} = 2.0 V			45		50	ns
		V _{CC} = 4.5 V			25		30	ns
		V _{CC} = 6.0 V			20		25	ns
t _t	transition time	Qn; see Fig. 6						
		V _{CC} = 2.0 V			30		35	ns
		V _{CC} = 4.5 V			19		22	ns
		V _{CC} = 6.0 V			16		19	ns
t _{en}	enable time	$\overline{OE}$ to Qn; see Fig. 8 [3]						
		V _{CC} = 2.0 V			22		25	ns
		V _{CC} = 4.5 V			14		17	ns
		V _{CC} = 6.0 V			13		16	ns
t _{dis}	disable time	$\overline{OE}$ to Qn; see Fig. 8 [4]						
		V _{CC} = 2.0 V			22		25	ns
		V _{CC} = 4.5 V			15		18	ns
		V _{CC} = 6.0 V			13		15	ns
t _w	pulse width	LE HIGH; see Fig. 7						
		V _{CC} = 2.0 V	100			120		ns
		V _{CC} = 4.5 V	20			24		ns
		V _{CC} = 6.0 V	17			20		ns
t _{su}	set up time	Dn to LE; see Fig.9						
		V _{CC} = 2.0 V	65			75		ns
		V _{CC} = 4.5 V	13			15		ns
		V _{CC} = 6.0 V	11			13		ns
t _h	hold time	Dn to LE; see Fig.9						
		V _{CC} = 2.0 V	5			5		ns
		V _{CC} = 4.5 V	5			5		ns
		V _{CC} = 6.0 V	5			5		ns

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Octal D-type transparent latch; 3-state

Symbol	Parameter	Conditions	-40 °C to +85 °C			-40 °C to +125 °C		Unit
			Min	Typ[1]	Max	Min	Max	
C_{PD}	power dissipation capacitance	$f_i = 1 \text{ MHz}$; $V_I = \text{GND to } V_{CC}$; [6]		45				pF
74HCT373								
t_{pd}	propagation delay	Dn to Qn; see Fig. 6 [2]						
		$V_{CC} = 4.5 \text{ V}$			25		30	ns
		LE to Qn; see Fig. 7 [2]						
		$V_{CC} = 4.5 \text{ V}$			25		30	ns
t_t	transition time	Qn; see Fig. 6 [5]						
		$V_{CC} = 4.5 \text{ V}$			25		30	ns
t_{en}	enable time	$\overline{OE}$ to Qn; see Fig. 8 [3]						
		$V_{CC} = 4.5 \text{ V}$			20		25	ns
t_{dis}	disable time	$\overline{OE}$ to Qn; see Fig. 8 [4]						
		$V_{CC} = 4.5 \text{ V}$			20		25	ns
t_w	pulse width	LE HIGH; see Fig. 7						
		$V_{CC} = 4.5 \text{ V}$	20			24		ns
t_{SU}	set up time	Dn to LE; see Fig.9						
		$V_{CC} = 4.5 \text{ V}$	15			18		ns
t_h	hold time	Dn to LE; see Fig.9						
		$V_{CC} = 4.5 \text{ V}$	4			4		ns
C_{PD}	power dissipation capacitance	$f_i = 1 \text{ MHz}$; $V_I = \text{GND to } V_{CC} - 1.5 \text{ V}$; [6]		45				pF

[1] Typical values are measured at $T_{amb} = 25 \text{ °C}$.

[2] t_{pd} is the same as t_{PLH} and t_{PHL} .

[3] t_{en} is the same as t_{PZL} and t_{PZH} .

[4] t_{dis} is the same as t_{PLZ} and t_{PHZ} .

[5] t_t is the same as t_{THL} and t_{TLH} .

[6] C_{PD} is used to determine the dynamic power dissipation (P_D in μW).

$P_D = C_{PD} \times V_{CC}^2 \times f_i \times N + \sum (C_L \times V_{CC}^2 \times f_o)$ where:

f_i = input frequency in MHz;

f_o = output frequency in MHz;

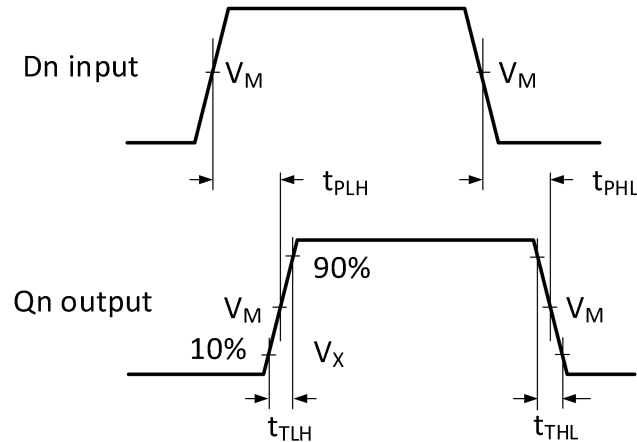
C_L = output load capacitance in pF;

V_{CC} = supply voltage in V;

N = number of inputs switching;

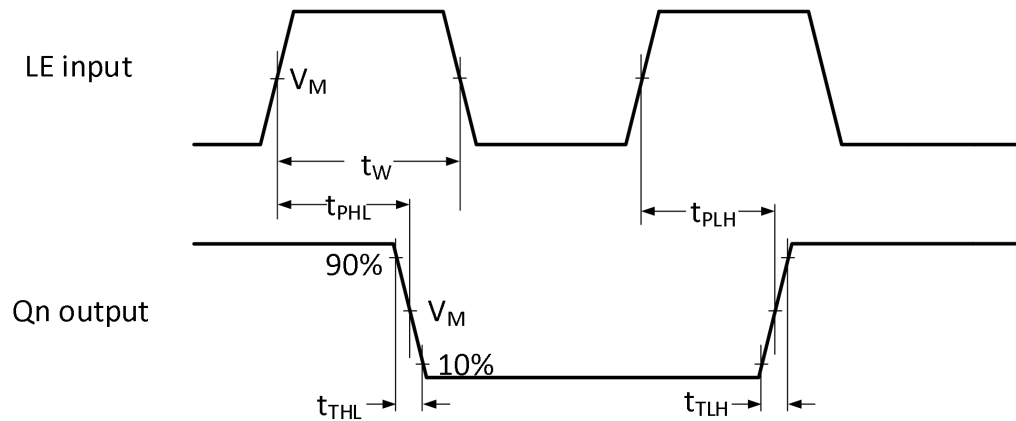
$\sum (C_L \times V_{CC}^2 \times f_o)$ = sum of outputs.

10.1. Waveforms and test circuit



Measurement points are given in Table 8.

Fig. 6. Propagation delay input (Dn) to output (Qn) and transition time output (Qn)

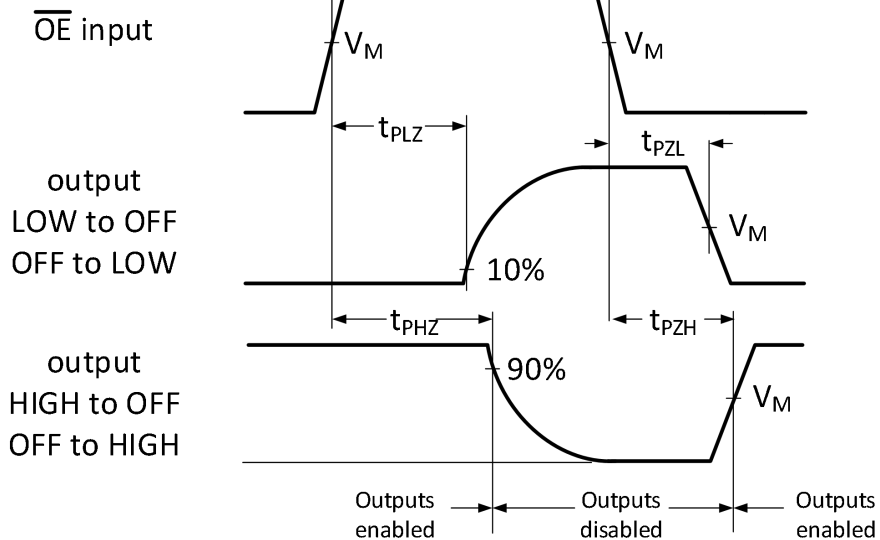


Measurement points are given in Table 8.

Fig. 7. Pulse width latch enable input (LE), propagation delay (LE) to output (Qn) and transition time output (Qn)

74HC373; 74HCT373

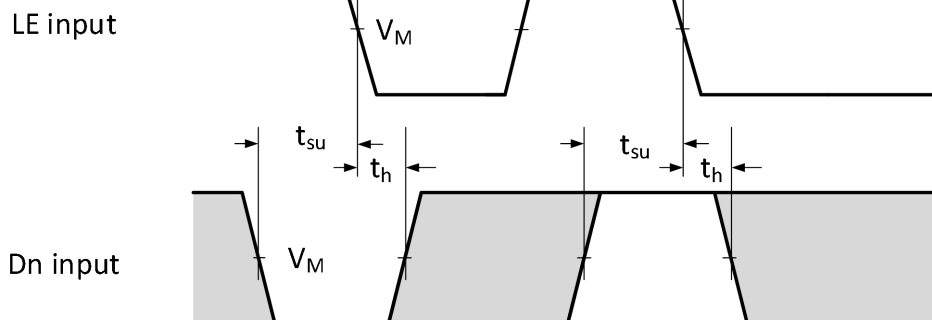
Octal D-type transparent latch; 3-state



Measurement points are given in Table 8.

V_{OL} and V_{OH} are typical output voltage levels that occur with the output load.

Fig. 8. Enable and disable times



Measurement points are given in Table 8.

The shaded areas indicate when the input is permitted to change for predictable output performance.

Fig. 9. Set-up and hold times for data input (Dn) to latch input (LE)

Table 8. Measurement points

Type	Input	Output
	V_M	V_M
74HC373	$0.5V_{CC}$	$0.5V_{CC}$
74HCT373	1.3 V	1.3 V

74HC373; 74HCT373

Octal D-type transparent latch; 3-state

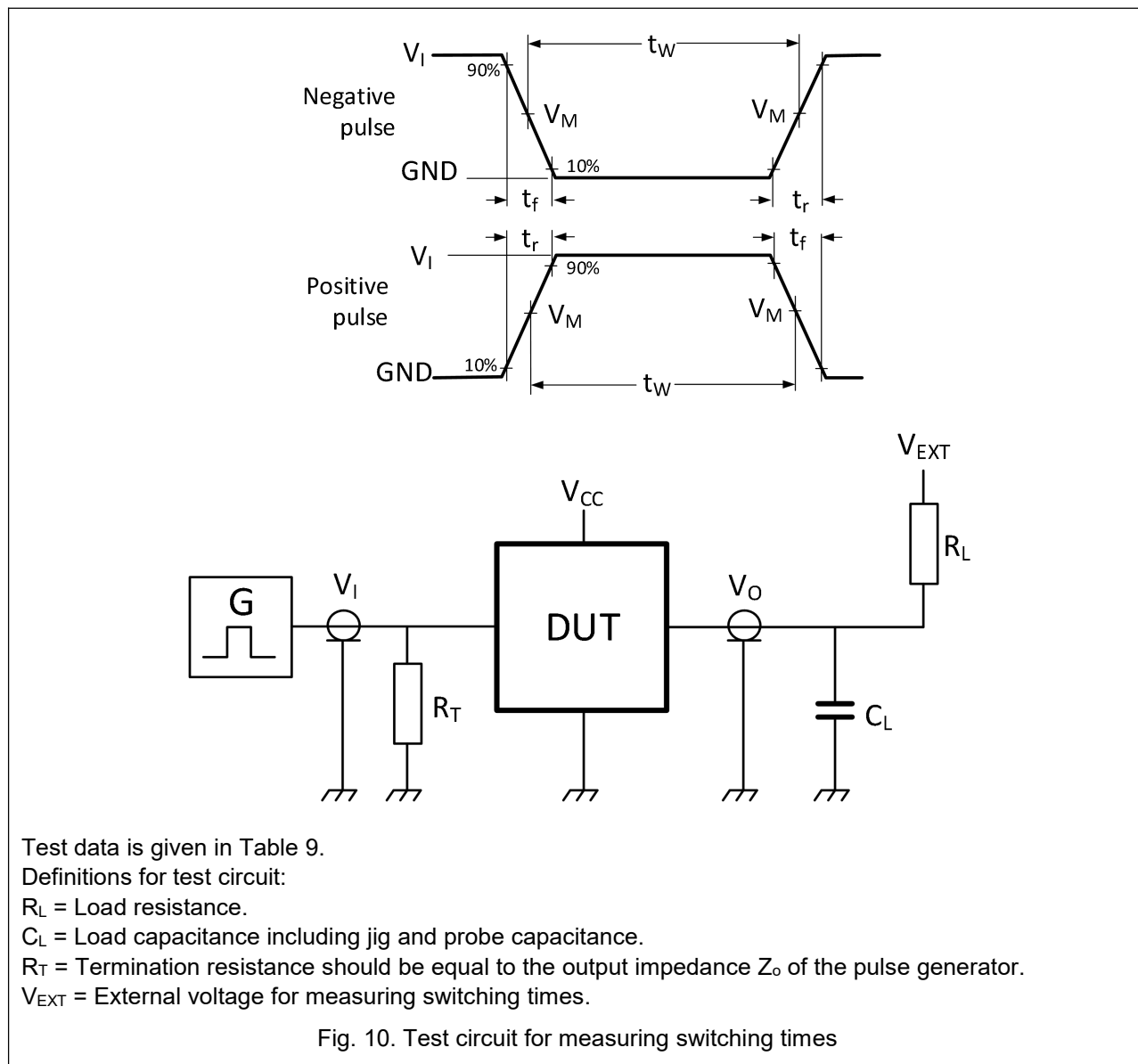
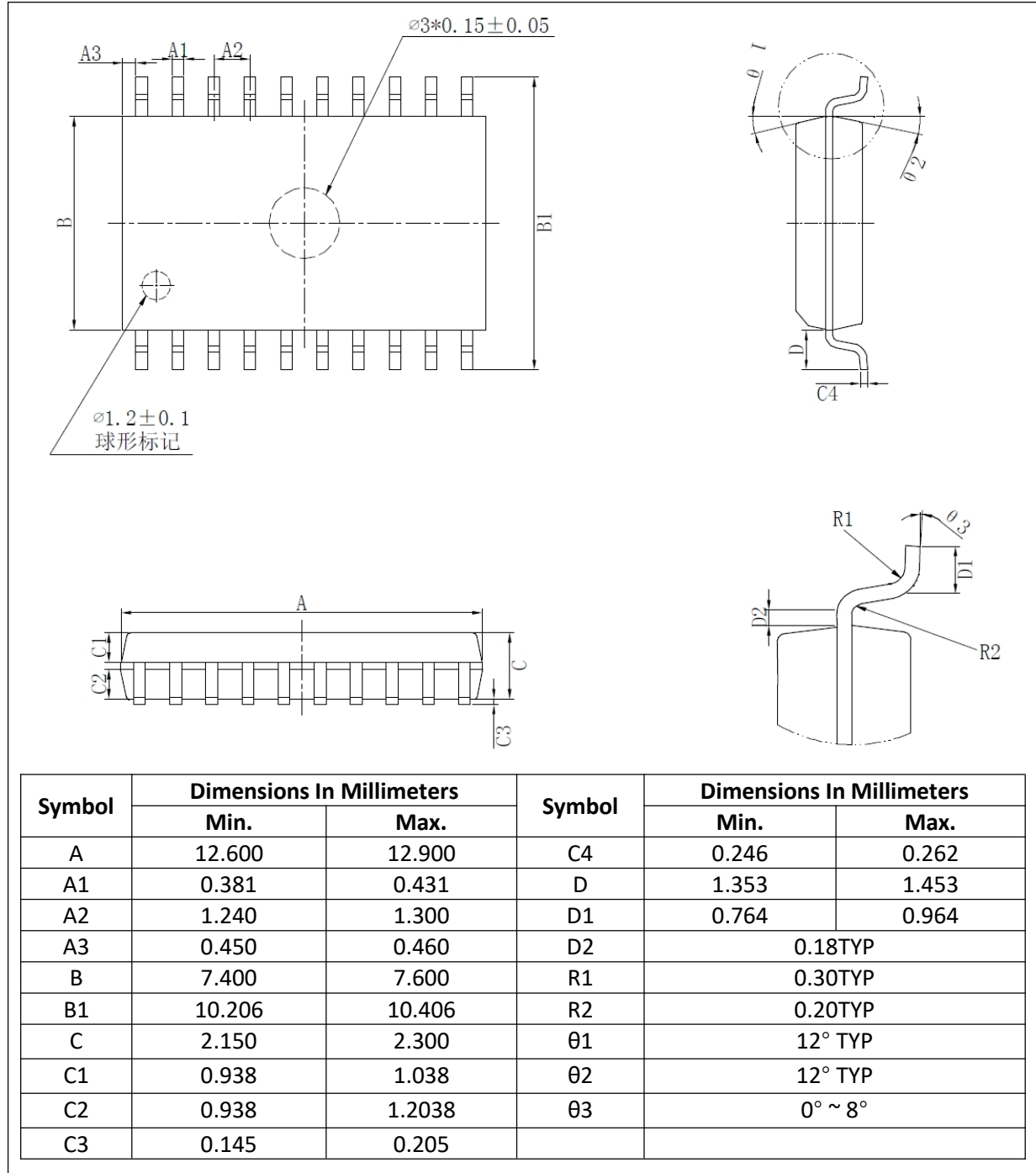


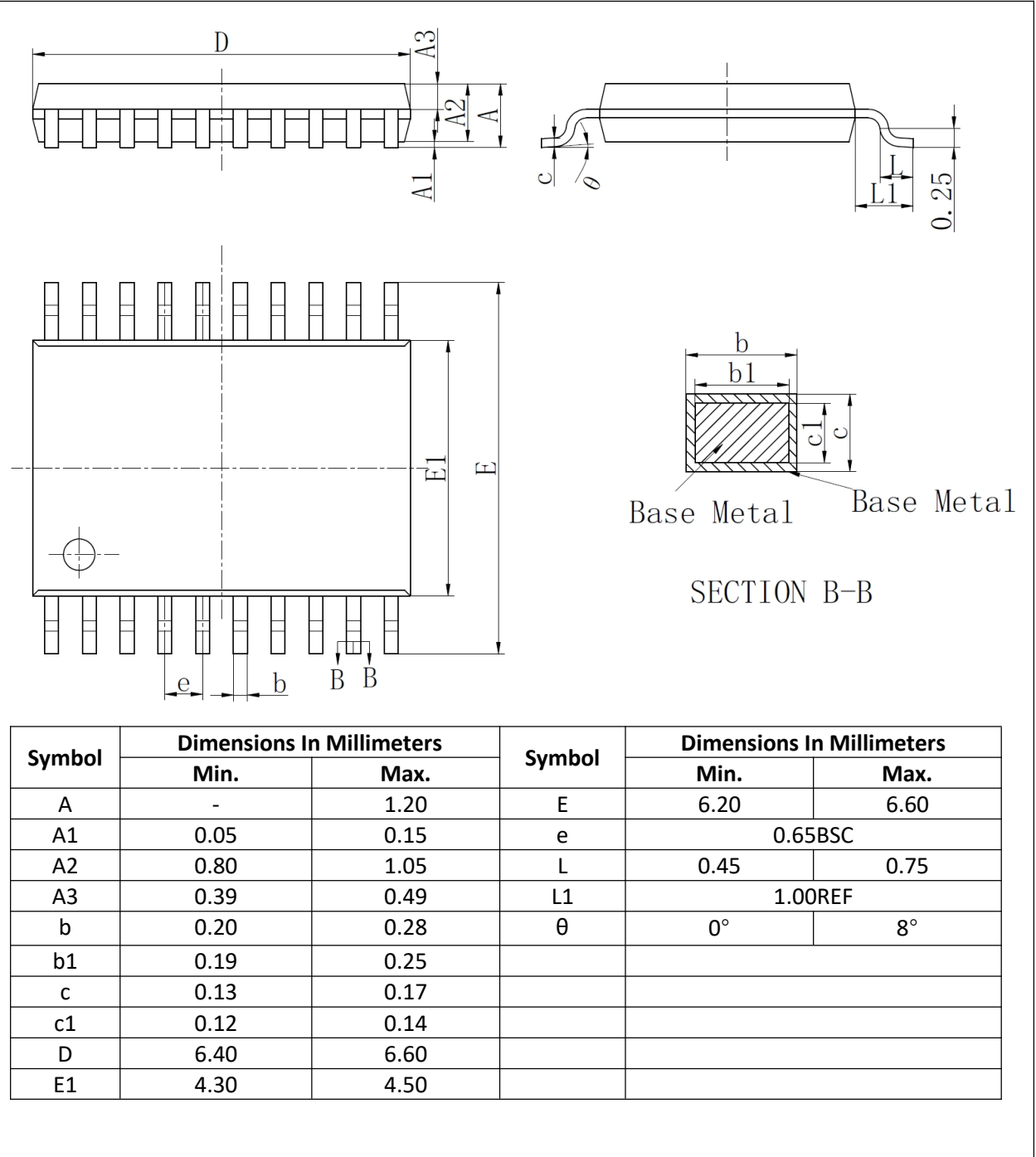
Table 9. Test data

Type	Input		Load		V_{EXT}		
	V_I	$t_r = t_f$	C_L	R_L	t_{PZL}, t_{PLZ}	t_{PHL}, t_{PLH}	t_{PZH}, t_{PHZ}
74HC373	V_{CC}	2.5 ns	50 pF	500 Ω	V_{CC}	Open	GND
74HCT373	3 V	2.5 ns	50 pF	500 Ω	V_{CC}	Open	GND

11. Package Outline

SOP-20L



TSSOP-20L


12. Abbreviations

Table 10. Abbreviations

Acronym	Description
CMOS	Complementary Metal-Oxide Semiconductor
DUT	Device Under Test
ESD	ElectroStatic Discharge
HBM	Human Body Model
CDM	Charged Device Model
TTL	Transistor-Transistor Logic

13. Revision History

Table 11. Revision history

Document ID	Release Date	Data sheet status	Change notice	Supersedes
74HC_HCT373 Rev. 1.0	Aug 08, 2024	Draft datasheet		