74HC273; 74HCT273

Octal D-type flip-flop with reset; positive-edge trigger

Draft datasheet, Rev. 1.0 Aug 08, 2024

1.General Description

The 74HC273; 74HCT273 is an octal positive-edge triggered D-type flip-flop. The device features clock (CP) and master reset ($\overline{MR}$) inputs. The outputs Qn will assume the state of their corresponding Dn inputs that meet the set-up and hold time requirements on the LOW-to-HIGH clock (CP) transition. A LOW on $\overline{MR}$ forces the outputs LOW independently of clock and data inputs. Inputs include clamp diodes. This enables the use of current limiting resistors to interface inputs to voltages in excess of V_{CC}.

2.Features and Benefits

- Wide operating voltage 2.0 V to 6.0 V
- High noise immunity
- CMOS low power dissipation
- Latch-up performance exceeds 250 mA
- Input levels:
  - For 74HC273: CMOS level
  - For 74HCT273: TTL level
- Common clock and master reset
- Eight positive edge-triggered D-type flip-flops
- ESD protection:
  - HBM ANSI/ESDA/JEDEC JS-001 Class 2 exceeds 3500 V
  - CDM ANSI/ESDA/JEDEC JS-002 Class C3 exceeds 2000 V
- Multiple package options
- Specified from -40 °C to +85 °C and from -40 °C to +125 °C

3.Applications

- Buffer/Storage Registers;
- Shift Registers;
- Pattern Generators

4.Ordering Information

Table 1. Ordering information

Type number	Package		
	Name	Description	Quantity
74HC273D	SOP-20L	plastic small outline package; 20 leads; body width 7.5mm	3000
74HCT273D			
74HC273PW	TSSOP-20L	plastic thin shrink small outline package; 20 leads; body width 4.4 mm	3000
74HCT273PW			

5.Function Diagram

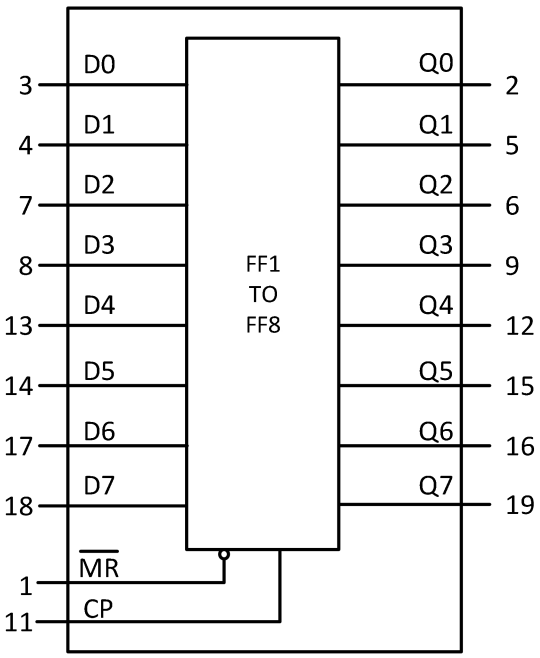


Fig 1.Functional diagram

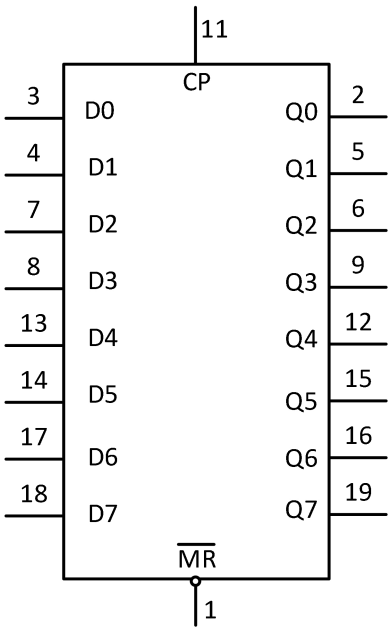


Fig 2. Logic symbol

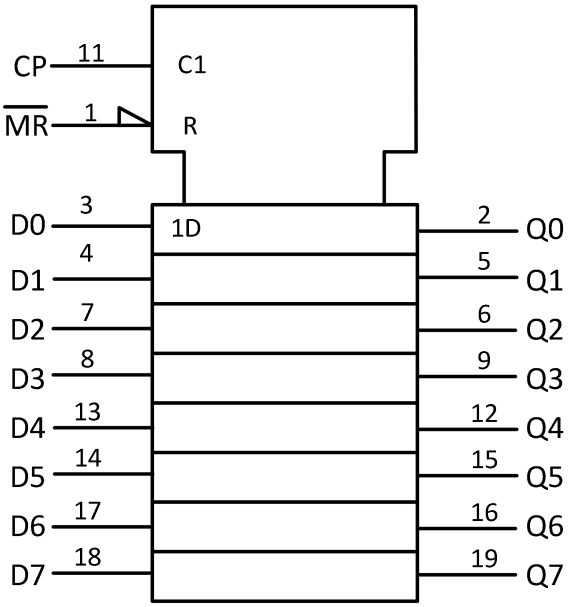


Fig 3. IEC logic symbol

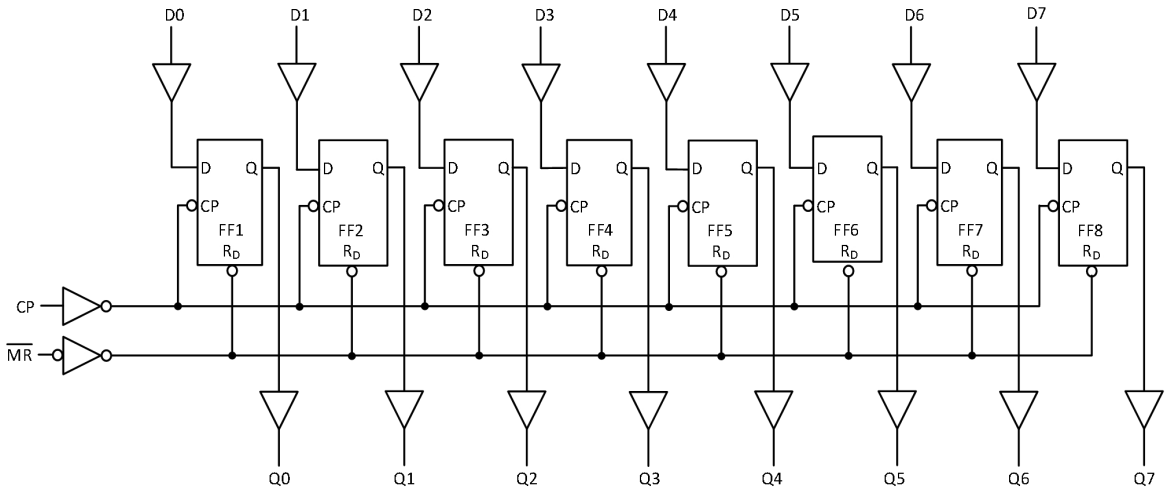


Fig 4. Logic diagram

6.Pinning Information

5.1. Pin map

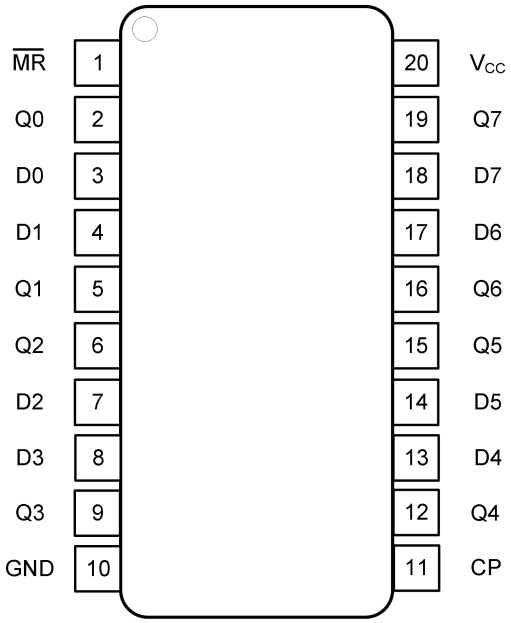


Fig 5. Top view pin configuration SOP and TSSOP

5.2. Pin description

Table 2. Pin description

Symbol	Pin	Description
$\overline{MR}$	1	master reset (active LOW)
Q0, Q1, Q2, Q3, Q4, Q5, Q6, Q7	2, 5, 6, 9, 12, 15, 16, 19	flip-flop output
D0, D1, D2, D3, D4, D5, D6, D7	3, 4, 7, 8, 13, 14, 17, 18	data input
GND	10	ground (0V)
CP	11	clock input (LOW-to-HIGH, edge-triggered)
V_{CC}	20	supply voltage

7.Functional Description

Table 3. Function table

H = HIGH voltage level;

h = HIGH voltage level one set-up time prior to the LOW-to-HIGH clock transition;

L = LOW voltage level;

l = LOW voltage level one set-up time prior to the LOW-to-HIGH clock transition;

X = don't care;

↑ = LOW-to-HIGH transition.

Operating modes	Inputs			Output
	$\overline{MR}$	CP	Dn	Qn
reset (clear)	L	X	X	L
load "1"	H	↑	h	H
load "0"	H	↑	l	L

8.Absolute Maximum Ratings

Stresses exceeding the absolute maximum ratings may damage the device. The device may not function or be operable above the recommended operating conditions and stressing the parts to these levels is not recommended. In addition, extended exposure to stresses above the recommended operating conditions may affect device reliability. The absolute maximum ratings are stress ratings only.

Table 4. Absolute Maximum Ratings

In accordance with the Absolute Maximum Rating System (IEC 60134). Voltages are referenced to GND.

Symbol	Parameter	Conditions	Min	Max	Unit
V_{CC}	supply voltage		-0.5	7	V
I_{IK}	input clamping current	$V_I < -0.5$ V or $V_I > V_{CC} + 0.5$ V [1]		±20	mA
I_{OK}	output clamping current	$V_O < -0.5$ V or $V_O > V_{CC} + 0.5$ V [1]		±20	mA
I_O	output current	-0.5 V $< V_O < V_{CC} + 0.5$ V		±25	mA
I_{CC}	supply current			50	mA
I_{GND}	ground current		-50		mA
P_{tot}	total power dissipation	T_{amb} = -40 °C to + 125 °C		500	mW
T_{stg}	storage temperature		-65	150	°C

[1] The input and output voltage ratings may be exceeded if the input and output current ratings are observed.

9.Recommended Operating Conditions

The Recommended Operating Conditions table defines the conditions for actual device operation. Recommended operating conditions are specified to ensure optimal performance to the datasheet specifications. EnergyMath does not recommend exceeding them or designing to Absolute Maximum Ratings.

Table 5. Recommended Operating Conditions

Symbol	Parameter	Conditions	74HC273			74HCT273			Unit
			Min	Typ	Max	Min	Typ	Max	
V_{CC}	supply voltage		2.0	5.0	6.0	4.5	5.0	5.5	V
V_I	input voltage		0		V_{CC}	0		V_{CC}	V
V_O	output voltage		0		V_{CC}	0		V_{CC}	V
T_{amb}	ambient temperature		-40	+25	+125	-40	+25	+125	°C
Δt/ΔV	Input transition rise and fall rate	V_{CC} = 2.0 V			625				ns/V
		V_{CC} = 4.5 V		1.67	139		1.67	139	ns/V
		V_{CC} = 6.0 V			83				ns/V

10. Static Characteristics

Table 6. Static characteristics

At recommended operating conditions. Voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions	-40 °C to +85 °C			-40 °C to +125 °C		Unit
			Min	Typ[1]	Max	Min	Max	
74HC273								
V_{IH}	HIGH-level input voltage	V_{CC} = 2.0 V	1.5			1.5		V
		V_{CC} = 4.5 V	3.15			3.15		V
		V_{CC} = 6.0 V	4.2			4.2		V
V_{IL}	LOW-level input voltage	V_{CC} = 2.0 V			0.5		0.5	V
		V_{CC} = 4.5 V			1.35		1.35	V
		V_{CC} = 6.0 V			1.8		1.8	V
V_{OH}	HIGH-level output voltage	V_I = V_{IH} or V_{IL}						
		I_O = -20µA; V_{CC} = 2.0 V	1.9			1.9		V
		I_O = -20µA; V_{CC} = 4.5 V	4.4			4.4		V
		I_O = -20µA; V_{CC} = 6.0 V	5.9			5.9		V
		I_O = -4.0 mA; V_{CC} = 4.5 V	3.84			3.7		V
		I_O = -5.2 mA; V_{CC} = 6.0 V	5.34			5.2		V
V_{OL}	LOW-level output voltage	V_I = V_{IH} or V_{IL}						
		I_O = 20µA; V_{CC} = 2.0 V			0.1		0.1	V
		I_O = 20µA; V_{CC} = 4.5 V			0.1		0.1	V
		I_O = 20µA; V_{CC} = 6.0 V			0.1		0.1	V
		I_O = 4.0 mA; V_{CC} = 4.5 V			0.33		0.4	V
		I_O = 5.2 mA; V_{CC} = 6.0 V			0.33		0.4	V
I_I	Input leakage current	V_I = V_{CC} or GND ; V_{CC} = 6.0 V			±1		±1	µA
I_{CC}	supply current	V_I = V_{CC} or GND ; I_O = 0A ; V_{CC} = 6.0 V			80		160	µA
C_I	input capacitance			3.5				pF

Symbol	Parameter	Conditions	-40 °C to +85 °C			-40 °C to +125 °C		Unit
			Min	Typ[1]	Max	Min	Max	
74HCT273								
V_{IH}	HIGH-level input voltage	V_{CC} = 4.5 V to 5.5 V	2.0			2.0		V
V_{IL}	LOW-level input voltage	V_{CC} = 4.5 V to 5.5 V			0.8		0.8	V
V_{OH}	HIGH-level output voltage	V_I = V_{IH} or V_{IL}; V_{CC} = 4.5 V						
		All outputs						
		I_O = -20µA	4.4			4.4		V
		Q7S output						
		I_O = -4.0 mA	3.84			3.7		V
		Qn bus driver outputs						
		I_O = -6.0 mA	3.7			3.7		V
V_{OL}	LOW-level output voltage	V_I = V_{IH} or V_{IL}; V_{CC} = 4.5 V						
		all outputs						
		I_O = 20µA			0.1		0.1	V
		Q7S output						
		I_O = 4.0 mA			0.33		0.4	V
		Qn bus driver outputs						
		I_O = 6.0 mA			0.33		0.4	V
I_I	Input leakage current	V_I = V_{CC} or GND ; V_{CC} = 5.5 V			±1		±1	µA
I_{CC}	supply current	V_I = V_{CC} or GND ; I_O = 0A ; V_{CC} = 5.5 V			80		160	µA
ΔI_{CC}	additional supply current	per pin ; V_I = V_{CC} - 2.1 V; I_O = 0 A; other inputs at V_{CC} or GND;V_{CC} = 4.5 V to 5.5 V			270		294	µA
C_I	input capacitance			3.5				pF

[1]All typical values are measured at T_{amb} = 25℃.

11. Dynamic Characteristics

Table 7. Dynamic characteristics

Voltages are referenced to GND (ground = 0 V); for test circuit see Fig. 9.

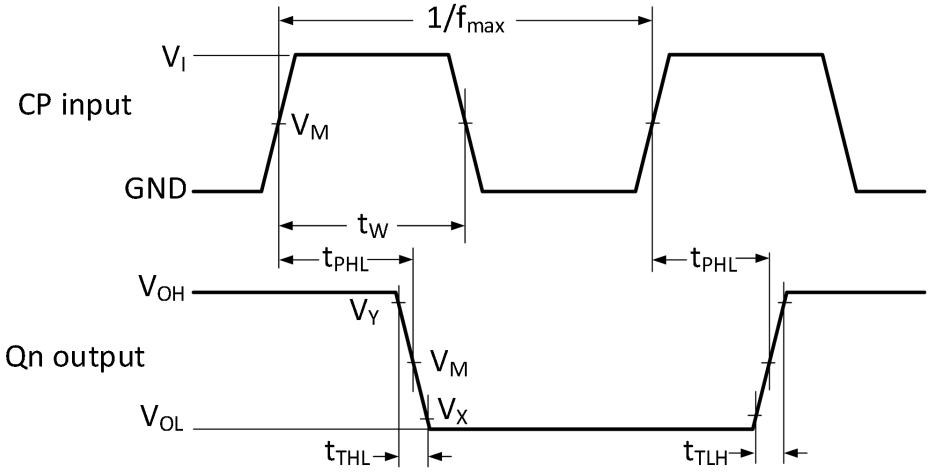
Symbol	Parameter	Conditions	-40 °C to +85 °C			-40 °C to +125 °C		Unit
			Min	Typ[1]	Max	Min	Max	
74HC273								
t_{pd}	propagation delay	CP to Qn; see Fig. 6 [2]						
		V_{CC} = 2.0 V			185		225	ns
		V_{CC} = 4.5 V			37		45	ns
		V_{CC} = 6.0 V			31		38	ns
t_{PHL}	HIGH to LOW propagation delay	$\overline{MR}$ to Qn; see Fig. 7						
		V_{CC} = 2.0 V			185		225	ns
		V_{CC} = 4.5 V			37		45	ns
		V_{CC} = 6.0 V			31		38	ns
t_t	transition time	Qn; see Fig. 6						
		V_{CC} = 2.0 V			95		110	ns
		V_{CC} = 4.5 V			19		22	ns
		V_{CC} = 6.0 V			15		19	ns
t_W	pulse width	CP HIGH or LOW; see Fig. 6						
		V_{CC} = 2.0 V	100			120		ns
		V_{CC} = 4.5 V	20			24		ns
		V_{CC} = 6.0 V	17			20		ns
		$\overline{MR}$ LOW; see Fig.7						
		V_{CC} = 2.0 V	75			90		ns
		V_{CC} = 4.5 V	15			18		ns
		V_{CC} = 6.0 V	13			15		ns
t_{rec}	recovery time	$\overline{MR}$ to CP; see Fig.7						
		V_{CC} = 2.0 V	65			75		ns
		V_{CC} = 4.5 V	13			15		ns

Symbol	Parameter	Conditions	-40 °C to +85 °C			-40 °C to +125 °C		Unit
			Min	Typ[1]	Max	Min	Max	
		V_{CC} = 6.0 V	11			13		ns
t_{SU}	set up time	Dn to CP; see Fig.8						
		V_{CC} = 2.0 V	75			90		ns
		V_{CC} = 4.5 V	15			18		ns
		V_{CC} = 6.0 V	13			15		ns
t_h	hold time	Dn to CP; see Fig.8						
		V_{CC} = 2.0 V	3			3		ns
		V_{CC} = 4.5 V	3			3		ns
		V_{CC} = 6.0 V	3			3		ns
f_{max}	maximum frequency	CP input; see Fig.6						
		V_{CC} = 2.0 V	4.8			4		MHz
		V_{CC} = 4.5 V	24			20		MHz
		V_{CC} = 6.0 V	28			24		MHz
C_{PD}	power dissipation capacitance	Per package ; V_I = GND to V_{CC} [3]		20				pF
74HCT273								
t_{pd}	propagation delay	CP to Qn; see Fig. 6 [2]			38		45	ns
t_{PHL}	HIGH to LOW propagation delay	$\overline{MR}$ to Qn; see Fig. 7						ns
t_t	transition time	Qn; see Fig. 6			43		51	ns
t_W	pulse width	CP input; see Fig. 6	20			24		ns
		$\overline{MR}$ LOW; see Fig.7	20			24		ns
t_{rec}	recovery time	$\overline{MR}$ to CP; see Fig. 7	13			15		ns
t_{su}	set up time	Dn to CP; see Fig. 8	15			18		ns
t_h	hold time	Dn to CP; see Fig. 8	3			3		ns
f_{max}	maximum frequency	CP input; see Fig.6	24			20		MHz
C_{PD}	power dissipation capacitance	Per package ; V_I = GND to V_{CC} - 1.5 V ; [3]		23				pF

[1] Typical values are measured at nominal supply voltage and 25℃.

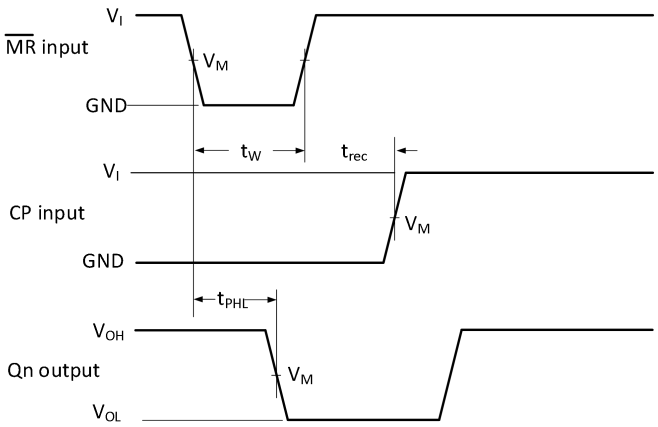
[2] t_{pd} is the same as t_{PHL} and t_{PLH}.
[3] C_{PD} is used to determine the dynamic power dissipation (P_D in µW).
$P_D = C_{PD} \times V_{CC}^2 \times f_i \times N + \Sigma(C_L \times V_{CC}^2 \times f_o)$ where:
f_i = input frequency in MHz;
f_o = output frequency in MHz;
C_L = output load capacitance in pF;
V_{CC} = supply voltage in V;
N = number of inputs switching;
$\Sigma(C_L \times V_{CC}^2 \times f_o)$ = sum of outputs.

10.1. Waveforms and test circuit



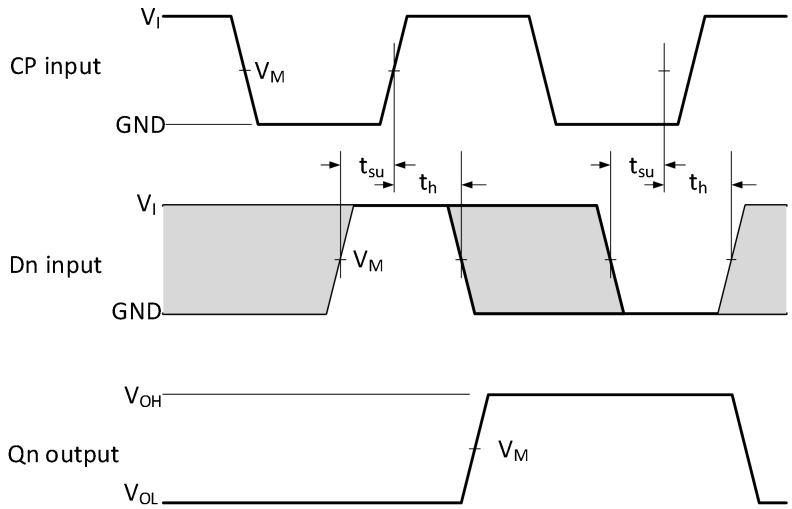
Measurement points are given in Table 8.
V_{OL} and V_{OH} are typical output voltage levels that occur with the output load.

Fig 6. Propagation delaysPropagation delay clock input (CP) to output (Qn), clock (CP) pulse width, output transition time and the maximum clock pulse frequency



Measurement points are given in Table 8.
V_{OL} and V_{OH} are typical output voltage levels that occur with the output load.

Fig 7. Propagation delay master reset ($\overline{MR}$) to output (Qn), pulse width master reset ($\overline{MR}$) and recovery time master reset ($\overline{MR}$) to clock (CP)



Measurement points are given in Table 8.

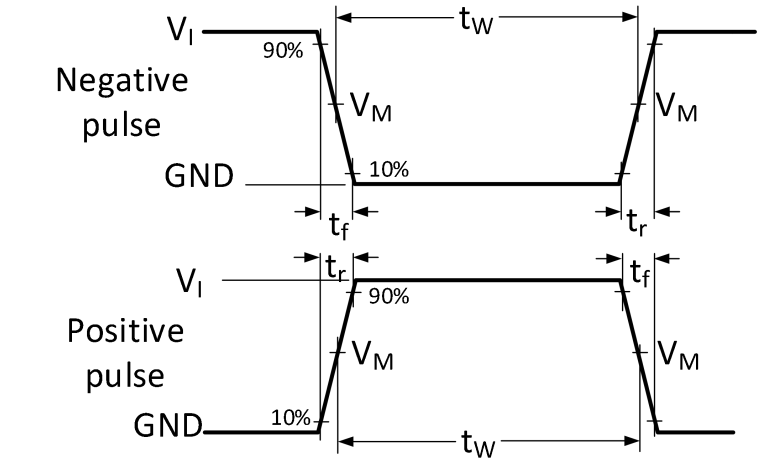
The shaded areas indicate when the input is permitted to change for predictable output performance.

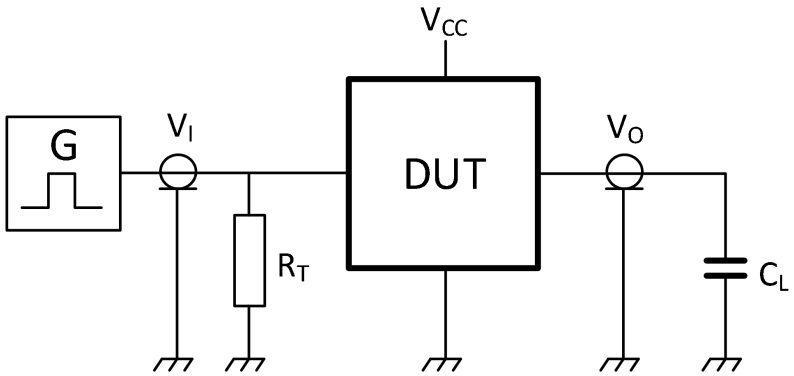
V_{OL} and V_{OH} are typical output voltage levels that occur with the output load.

Fig 8. Data set up and hold times data input(Dn)

Table 8. Measurement points

Type	Input	Output
	V_M	V_M
74HC273	$0.5V_{CC}$	$0.5V_{CC}$
74HCT273	1.3V	1.3V





Test data is given in Table 9.
Definitions for test circuit:
R_L = Load resistance.
C_L = Load capacitance including jig and probe capacitance.
R_T = Termination resistance should be equal to the output impedance Z_o of the pulse generator.

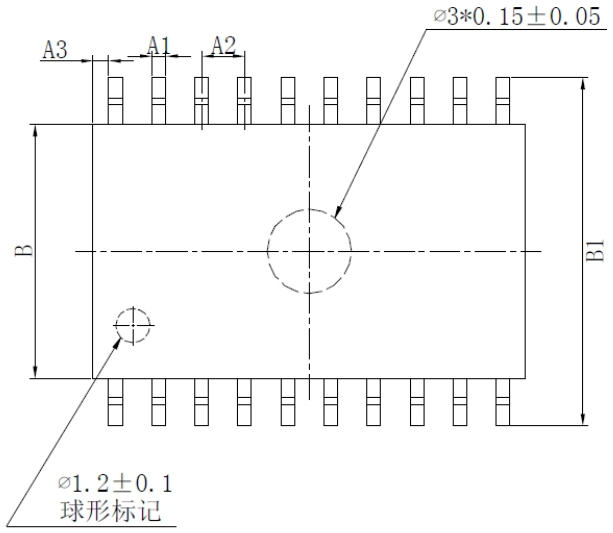
Fig 9. Test circuit for measuring switching times

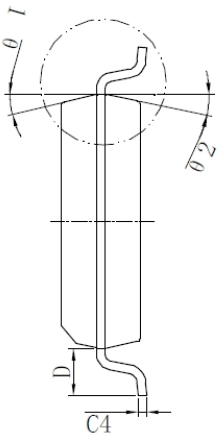
Table 9. Test data

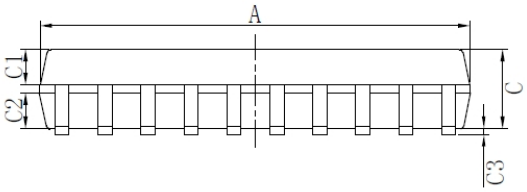
Type	Input		Load
	V_I	$t_r = t_f$	C_L
74HC273	V_{CC}	2.5ns	50pF
74HCT273	3.0V	2.5ns	50pF

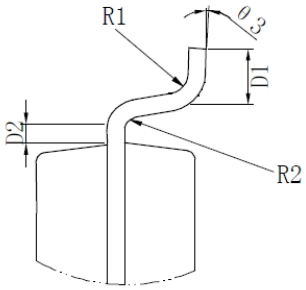
12. Package Outline

SOP-20L



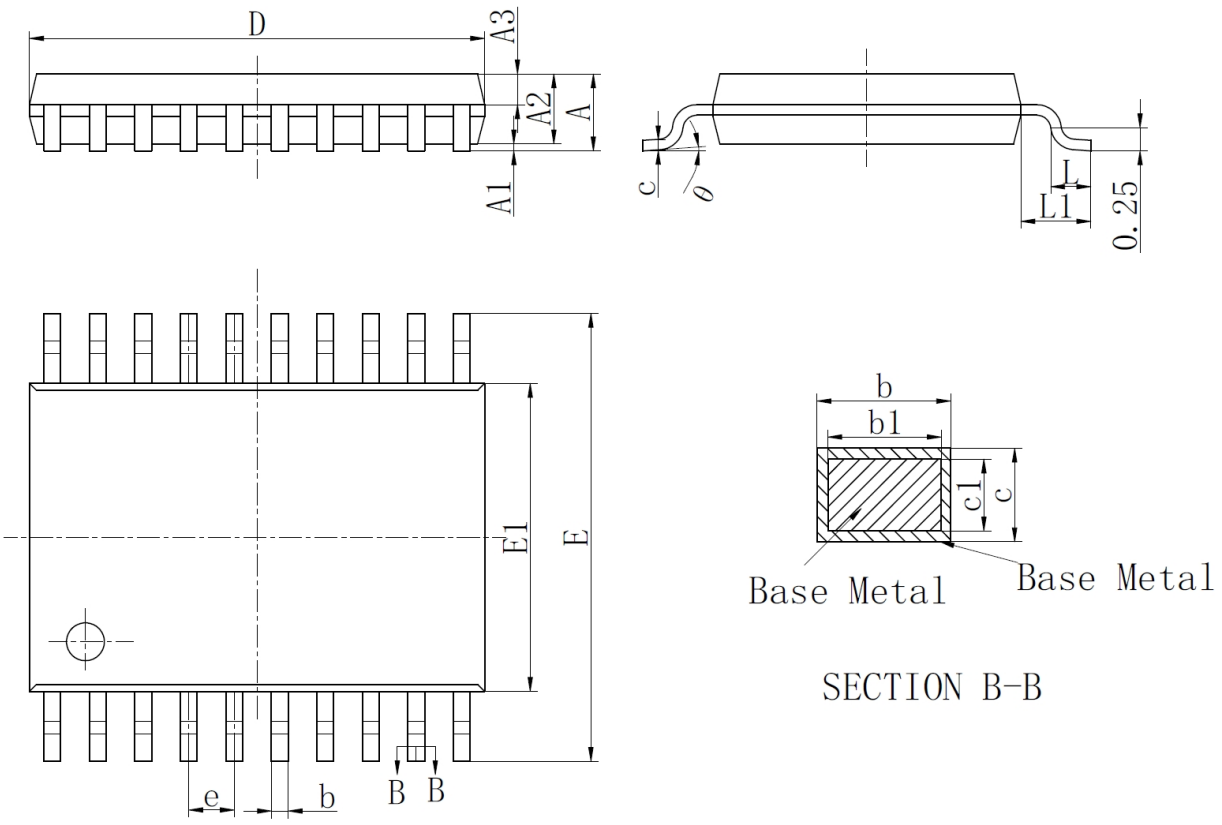






Symbol	Dimensions In Millimeters		Symbol	Dimensions In Millimeters	
	Min.	Max.		Min.	Max.
A	12.600	12.900	C4	0.246	0.262
A1	0.381	0.431	D	1.353	1.453
A2	1.240	1.300	D1	0.764	0.964
A3	0.450	0.460	D2	0.18TYP	
B	7.400	7.600	R1	0.30TYP	
B1	10.206	10.406	R2	0.20TYP	
C	2.150	2.300	θ1	12° TYP	
C1	0.938	1.038	θ2	12° TYP	
C2	0.938	1.2038	θ3	0° ~ 8°	
C3	0.145	0.205			

TSSOP-20L



Symbol	Dimensions In Millimeters		Symbol	Dimensions In Millimeters	
	Min.	Max.		Min.	Max.
A	-	1.20	E	6.20	6.60
A1	0.05	0.15	e	0.65BSC	
A2	0.80	1.05	L	0.45	0.75
A3	0.39	0.49	L1	1.00REF	
b	0.20	0.28	θ	0°	8°
b1	0.19	0.25			
c	0.13	0.17			
c1	0.12	0.14			
D	6.40	6.60			
E1	4.30	4.50			

13. Abbreviations

Table 10. Abbreviations

Acronym	Description
CMOS	Complementary Metal-Oxide Semiconductor
DUT	Device Under Test
ESD	ElectroStatic Discharge
HBM	Human Body Model
CDM	Charge Device Model
TTL	Transistor-Transistor Logic

14. Revision History

Table 11. Revision history

Document ID	Release Date	Data sheet status	Change notice	Supersedes
74HC_HCT273 Rev. 1.0	Aug 08, 2024	Draft datasheet		