DESCRIPTION

The JRC4558 consists of two high performance operational amplifiers. The IC features high gain, low equivalent input noise voltage, high input resistance, excellent channel separation, wide range of operating voltage and internal frequency compensation. It can work with ±16V maximum power supply voltage or single power supply up to 32V. The JRC4558 is available in DIP-8 and SOP-8 packages.

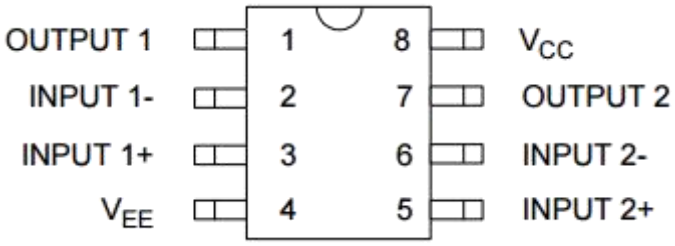
FEATURES

- No frequency compensation required.
- No latch-up
- Large common mode and differential voltage range
- Parameter tracking over temperature range
- Gain and phase match between amplifiers
- Internally frequency compensated
- Low noise input transistors

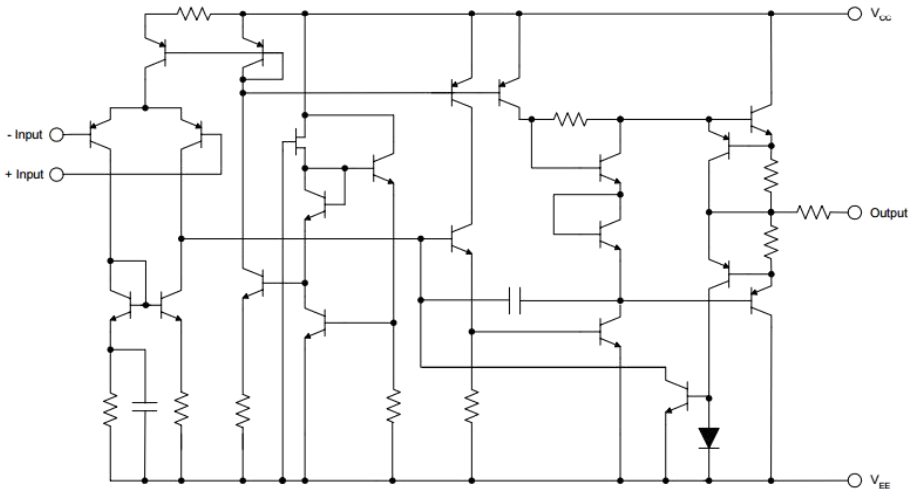
APPLICATIONS

- Audio AC-3 Decoder System
- Audio Amplifier

PIN CONFIGURATION



BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS

Characteristic	Symbol	Value	Unit
Supply Voltage	Vcc	±16	V
Differential input voltage	VI(DIFF)	±16	V
Power Dissipation	PD	400	mW
Input Voltage	VI	±15	V
Operating Temperature	TOPR	0-+70	℃
Storage Temperature	TOPR	-65-+150	℃

ELECTRICAL CHARACTERISTICS(Ta=25℃ ,Vcc=15V,Vee=-15V)

Characteristic	Symbol	Test Condition	Min	Typ	Max	Unit
Supply Current	Icc			3.5	5.6	mA
Input offset voltage	V_{IO}	Rs<10kW		2	6	mV
Input offset current	I_{IO}			5	200	nA
Input bias current	I_{BIAS}			30	500	nA
Large signal voltage gain	Gv	Vo(p-p)=10V,RL<2kW	20	200		V/mV
Common Mode Input Voltage Range	$VI_{(R)}$		±12	±13		V
Common Mode Rejection Ratio	CMRR	Rs<10kW	70	90		dB
Supply Voltage Rejection Ratio	PSRR	Rs<10kW	76	90		dB
Output Voltage swing	$Vo_{(p-p)}$	Rs<10kW		±12	±14	V
Power Dissipation	P_D			70	170	mV
Slew Rate	SR	Vi=10V,RL>2kW,CL<100pF	1.2			V/ms
Rise Time	TRIS	Vi=20mV,RL>2kW CL<100pF		0.3		ms
Overshoot	OS	Vi=20mV,RL>2kW,CL<100pF		15		%
Output Current	I_{SINK}	V-=1V, V+= 0V, VO=2V		35		
	I_{SOURCE}	V+=1V, V-= 0V, VO=2V		15		

TYPICAL PERFORMANCE CHARACTERISTICS

Fig.1 Positive output voltage swing vs Load resistance

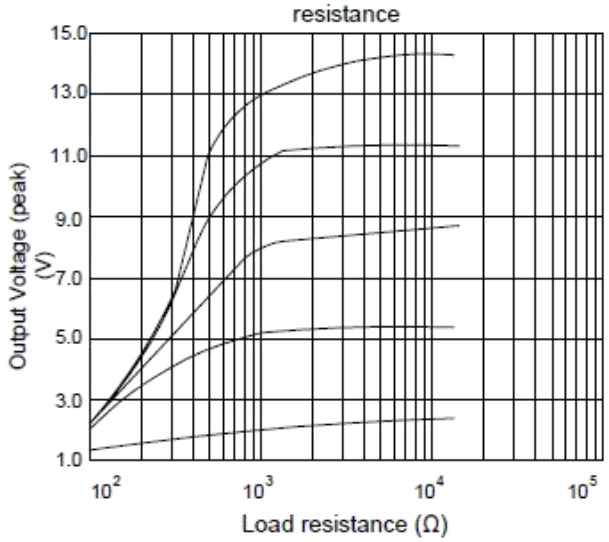


Fig.2 Positive output voltage swing vs Load resistance

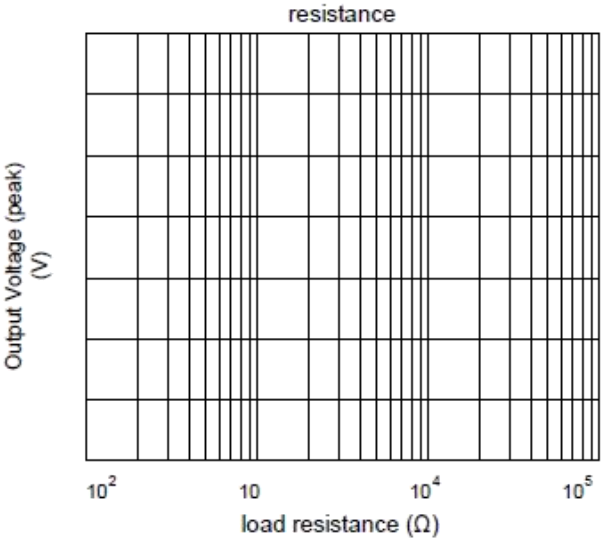


Fig.3 Power bandwith(large signal swing vs frequency)

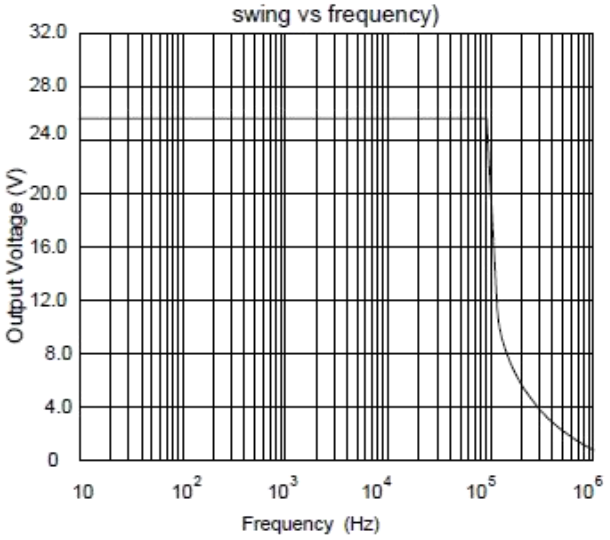


Fig. 4 Burst Noise vs Rs

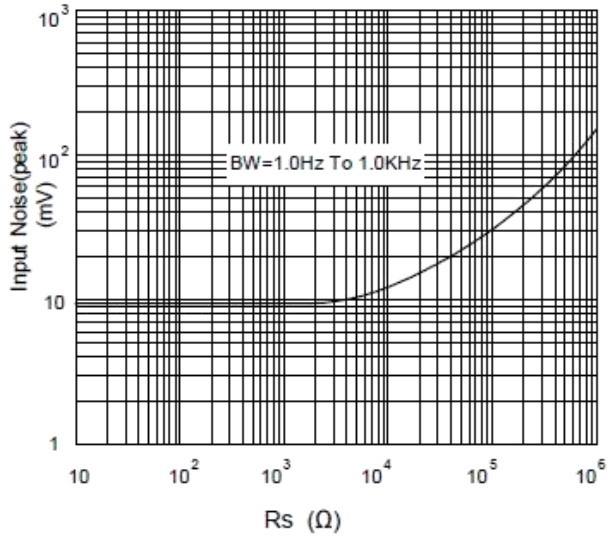
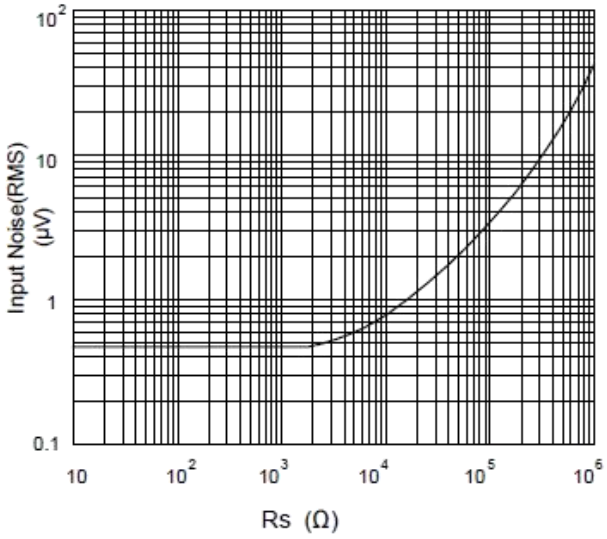


Fig. 5 RMS Noise vs Rs



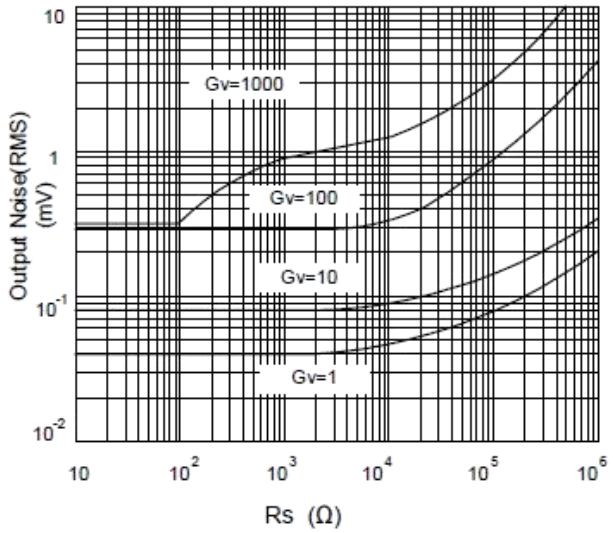


Fig. 8 Open loop frequency response

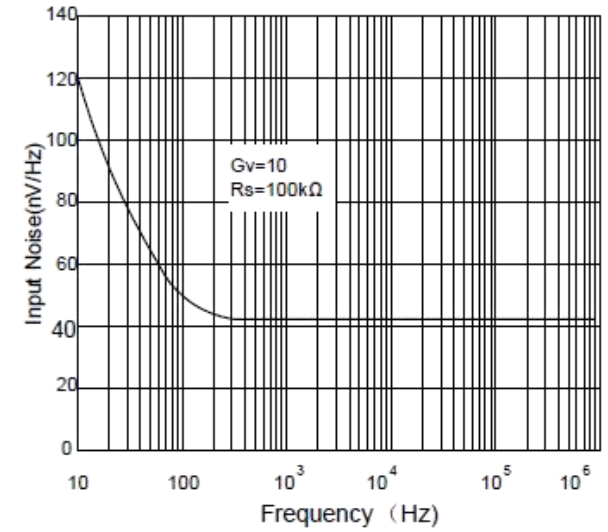
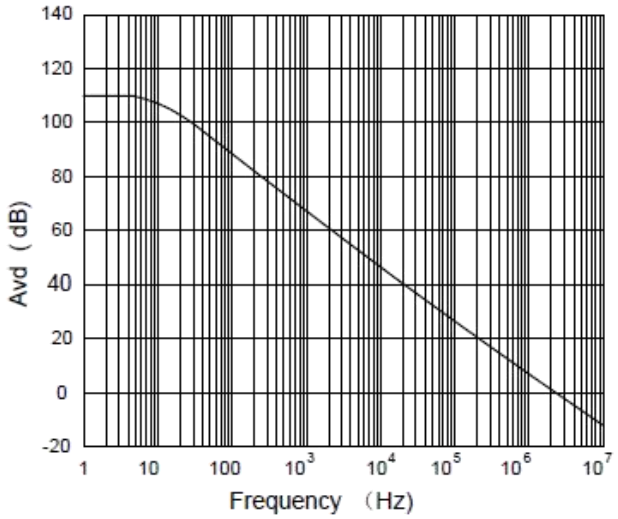
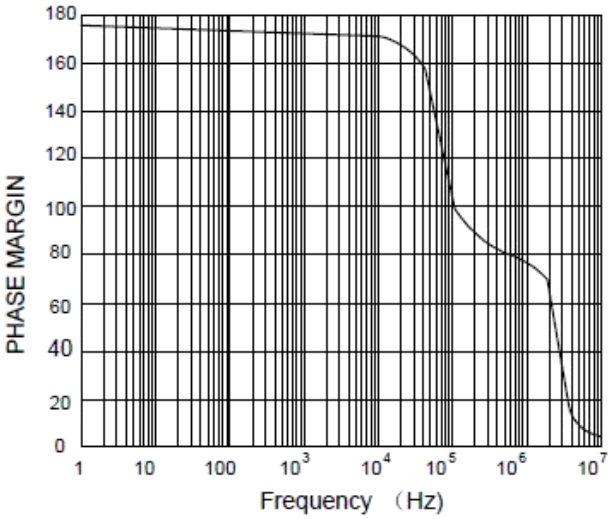


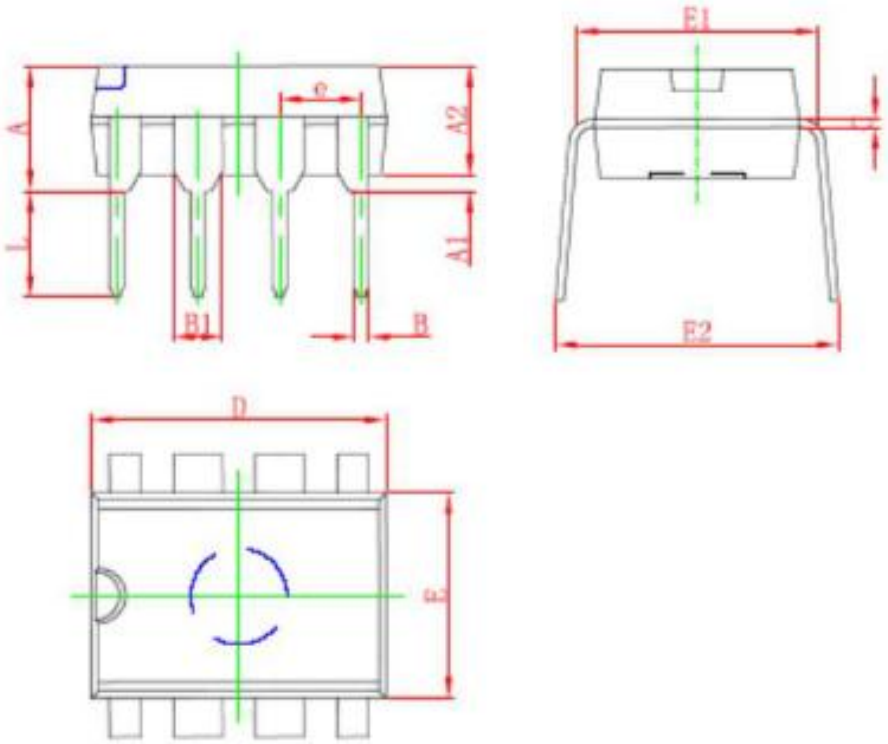
Fig. 9 PHASE MARGIN vs FREQUENCY





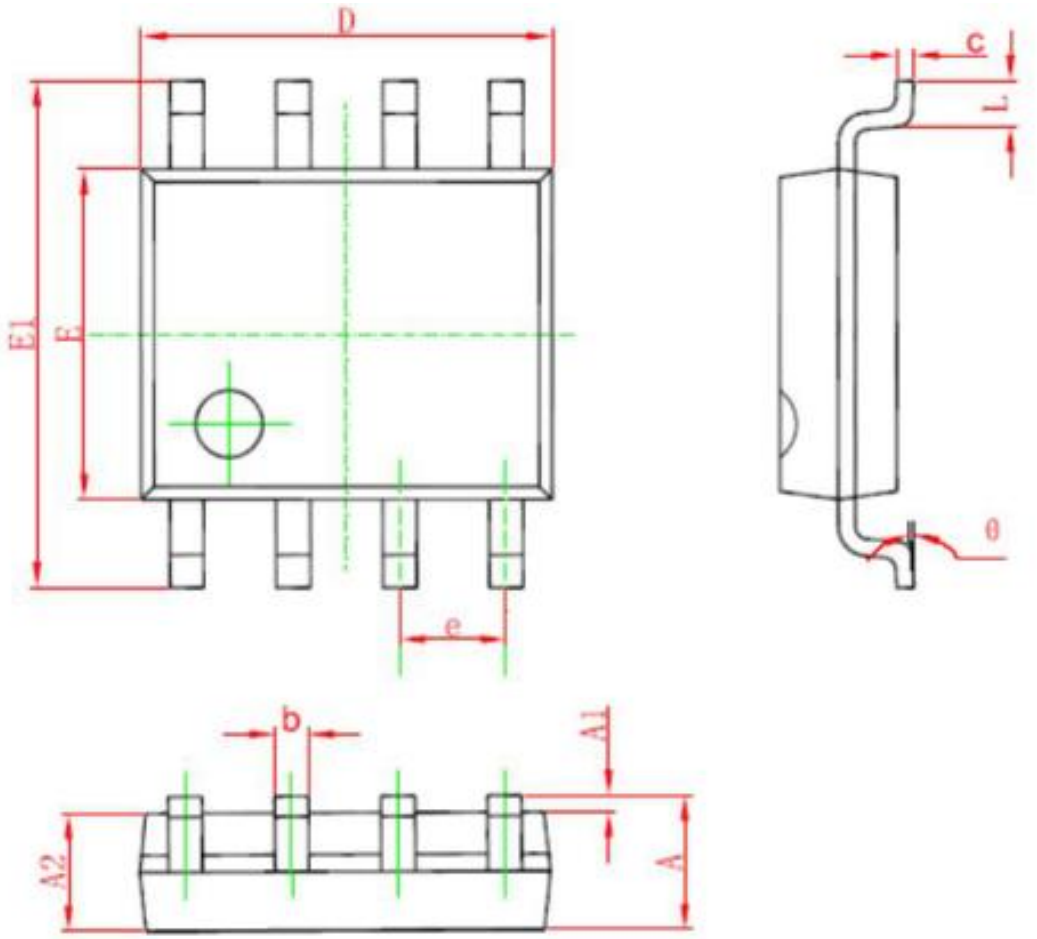
PACKAGE OUTLINE DIMENSIONS

DIP-8



Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min	Max	Min	Max
A	3.710	4.310	0.146	0.170
A1	0.510		0.020	
A2	3.200	3.600	0.126	0.142
B	0.380	0.570	0.015	0.022
B1	1.524 (BSC)		0.060 (BSC)	
C	0.204	0.360	0.008	0.014
D	9.000	9.400	0.354	0.370
E	6.200	6.600	0.244	0.260
E1	7.320	7.920	0.288	0.312
e	2.540 (BSC)		0.100 (BSC)	
L	3.000	3.600	0.118	0.142
E2	8.400	9.000	0.331	0.354

SOP-8



Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min	Max	Min	Max
A	1.350	1.750	0.053	0.069
A1	0.100	0.250	0.004	0.010
A2	1.350	1.550	0.053	0.061
b	0.330	0.510	0.013	0.020
c	0.170	0.250	0.006	0.010
D	4.700	5.100	0.185	0.200
E	3.800	4.000	0.150	0.157
E1	5.800	6.200	0.228	0.244
e	1.270 (BSC)		0.050 (BSC)	
L	0.400	1.270	0.016	0.050
θ	0°	8°	0°	8°