

N-Channel Super Junction Power MOSFET

General Description

The series of devices use advanced super junction technology and design to provide excellent RDS(ON) with low gate charge.

This super junction MOSFET fits the industry's AC-DC SMPS requirements for PFC, AC/DC power conversion, and industrial power applications.

Features

- Multi-layer Epitaxial Chip Technology
- Low On-Resistance
- 100% avalanche tested
- RoHS Compliant

Absolute Maximum Ratings

Symbol	Parameter	Rating	Units
V_{DS}	Drain-Source Voltage	650	V
V_{GS}	Gate-Source Voltage	± 30	V
$I_D@T_C=25^\circ\text{C}$	Continuous Drain Current	11	A
$I_D@T_C=100^\circ\text{C}$	Continuous Drain Current	9	A
I_{DM}	Pulsed Drain Current	44	A
EAS	Single Pulse Avalanche Energy ¹	202	mJ
$P_D@T_C=25^\circ\text{C}$	Total Power Dissipation	83	W
T_{STG}	Storage Temperature Range	-55 to 150	$^\circ\text{C}$
T_J	Operating Junction Temperature Range	-55 to 150	$^\circ\text{C}$

Thermal Data

Symbol	Parameter	Typ.	Max.	Unit
$R_{\theta JA}$	Thermal Resistance Junction-ambient	---	62	$^\circ\text{C/W}$
$R_{\theta JC}$	Thermal Resistance Junction -Case	---	1.5	$^\circ\text{C/W}$

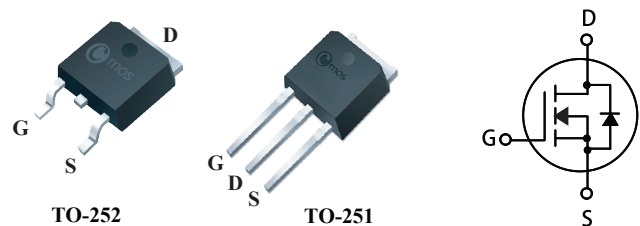
Product Summary

BVDSS	$R_{DS(on)}$ max.	ID
650V	0.38Ω	11A

Applications

- Power factor correction (PFC)
- Switched mode power supplies(SMPS)
- Uninterruptible Power Supply (UPS)

TO-252/TO-251 Pin Configuration



Type	Package	Marking
CMD65R380Q	TO-252	CMD65R380Q
CMU65R380Q	TO-251	CMU65R380Q

Electrical Characteristics ($T_J=25^\circ\text{C}$, unless otherwise noted)

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
BV_{DSS}	Drain-Source Breakdown Voltage	$V_{GS}=0V$, $I_D=250\mu A$	650	---	---	V
$R_{DS(ON)}$	Static Drain-Source On-Resistance	$V_{GS}=10V$, $I_D=5.5A$	---	---	0.38	Ω
$V_{GS(th)}$	Gate Threshold Voltage	$V_{DS}=V_{GS}$, $I_D=250\mu A$	2	---	4	V
I_{DSS}	Drain-Source Leakage Current	$V_{DS}=650V$, $V_{GS}=0V$, $T_J=25^\circ\text{C}$	---	---	1	μA
I_{GSS}	Gate-Source Leakage Current	$V_{GS}=\pm 30V$, $V_{DS}=0V$	---	---	± 100	nA
g_{fs}	Forward Transconductance	$V_{DS}=30V$, $I_D=4A$	---	8	---	S
R_g	Gate Resistance	$V_{DS}=0V$, $V_{GS}=0V$, $f=1\text{MHz}$	---	23	---	Ω
Q_g	Total Gate Charge	$V_{DS}=520V$, $V_{GS}=10V$, $I_D=10.6A$	---	21	---	nC
Q_{gs}	Gate-Source Charge		---	5.3	---	
Q_{gd}	Gate-Drain Charge		---	7.5	---	
$T_{d(on)}$	Turn-On Delay Time	$V_{DS}=325V$, $R_G=25\Omega$ $I_D=10.6A$ $V_{GS}=10V$	---	20	---	ns
T_r	Rise Time		---	39	---	
$T_{d(off)}$	Turn-Off Delay Time		---	109	---	
T_f	Fall Time		---	37	---	
C_{iss}	Input Capacitance	$V_{DS}=100V$, $V_{GS}=0V$, $f=1\text{MHz}$	---	750	---	pF
C_{oss}	Output Capacitance		---	42	---	
C_{rss}	Reverse Transfer Capacitance		---	3.1	---	

Diode Characteristics

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
I_S	Continuous Source Current	$V_G=V_D=0V$, Force Current	---	---	11	A
I_{SM}	Pulsed Source Current		---	---	44	A
V_{SD}	Diode Forward Voltage	$V_{GS}=0V$, $I_S=11A$, $T_J=25^\circ\text{C}$	---	---	1.4	V
t_{rr}	Reverse Recovery Time	$di/dt=100A/\mu s$	---	324	---	ns
Q_{rr}	Reverse Recovery Charge	$V_{DD}=100V$, $I_F=10.6A$	---	3.8	---	μC

Notes:

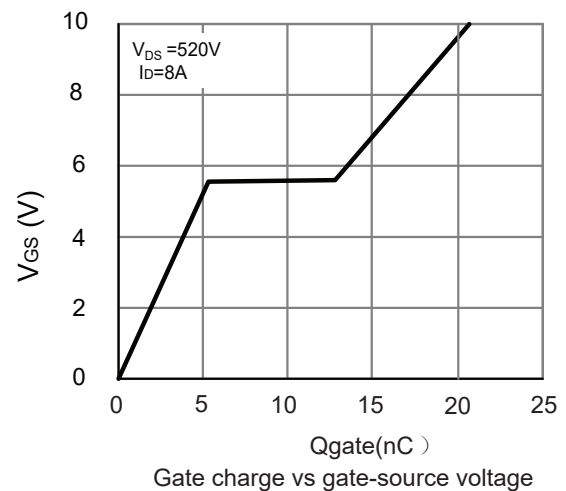
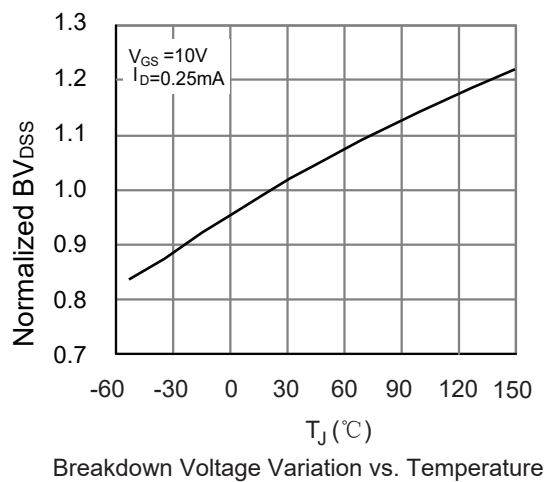
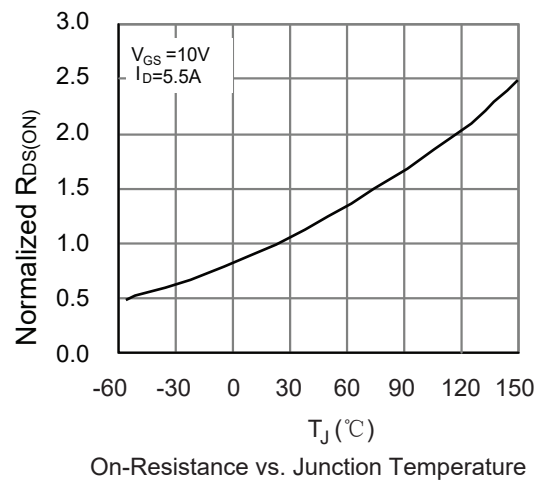
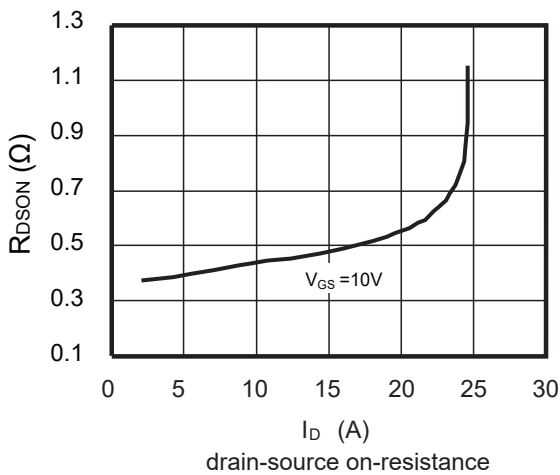
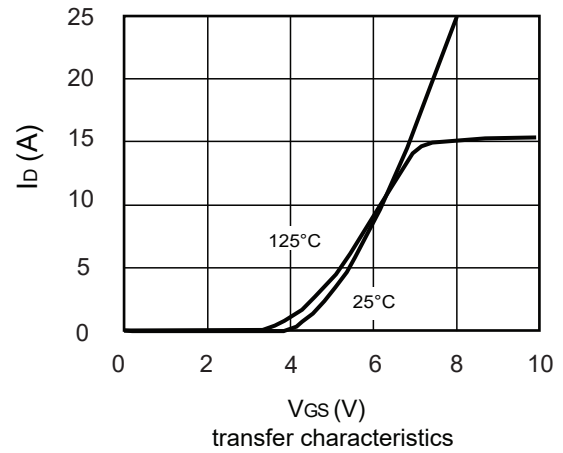
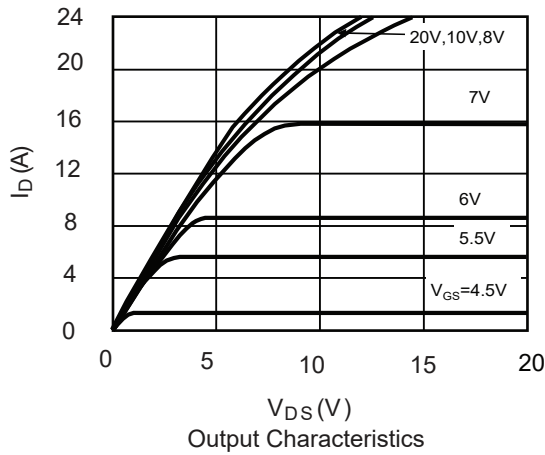
1. The EAS data shows Max. rating. The test condition is $V_{DS}=80V$, $V_{GS}=10V$, $L=20mH$, $I_{AS}=4.5A$.

This product has been designed and qualified for the consumer market.

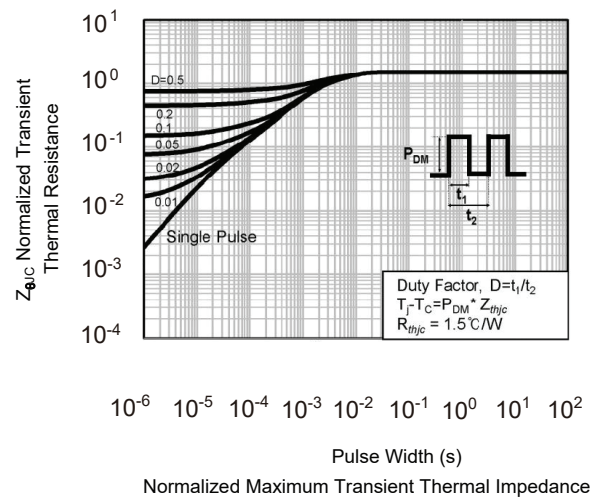
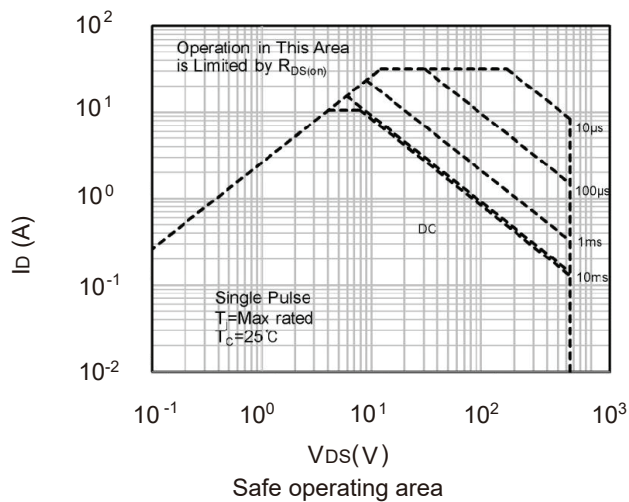
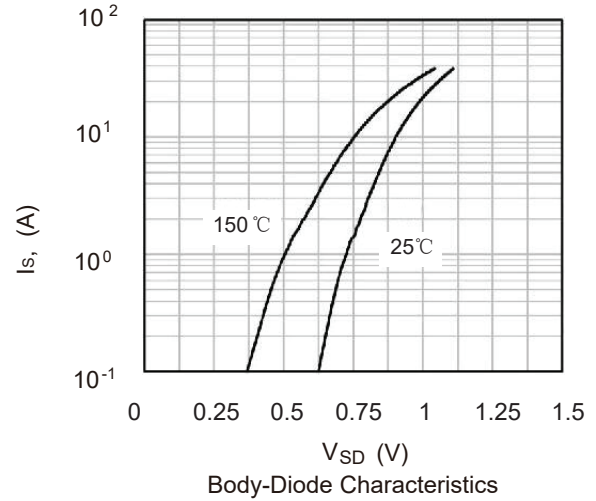
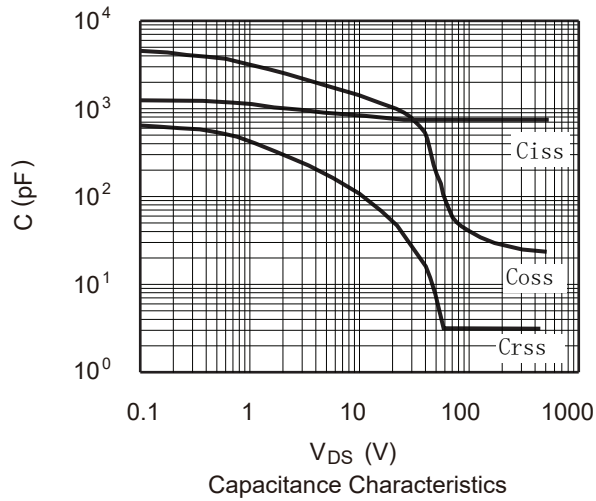
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CMOS reserves the right to improve product design, functions and reliability without notice. Please refer to the latest version of specification.

Typical Characteristics

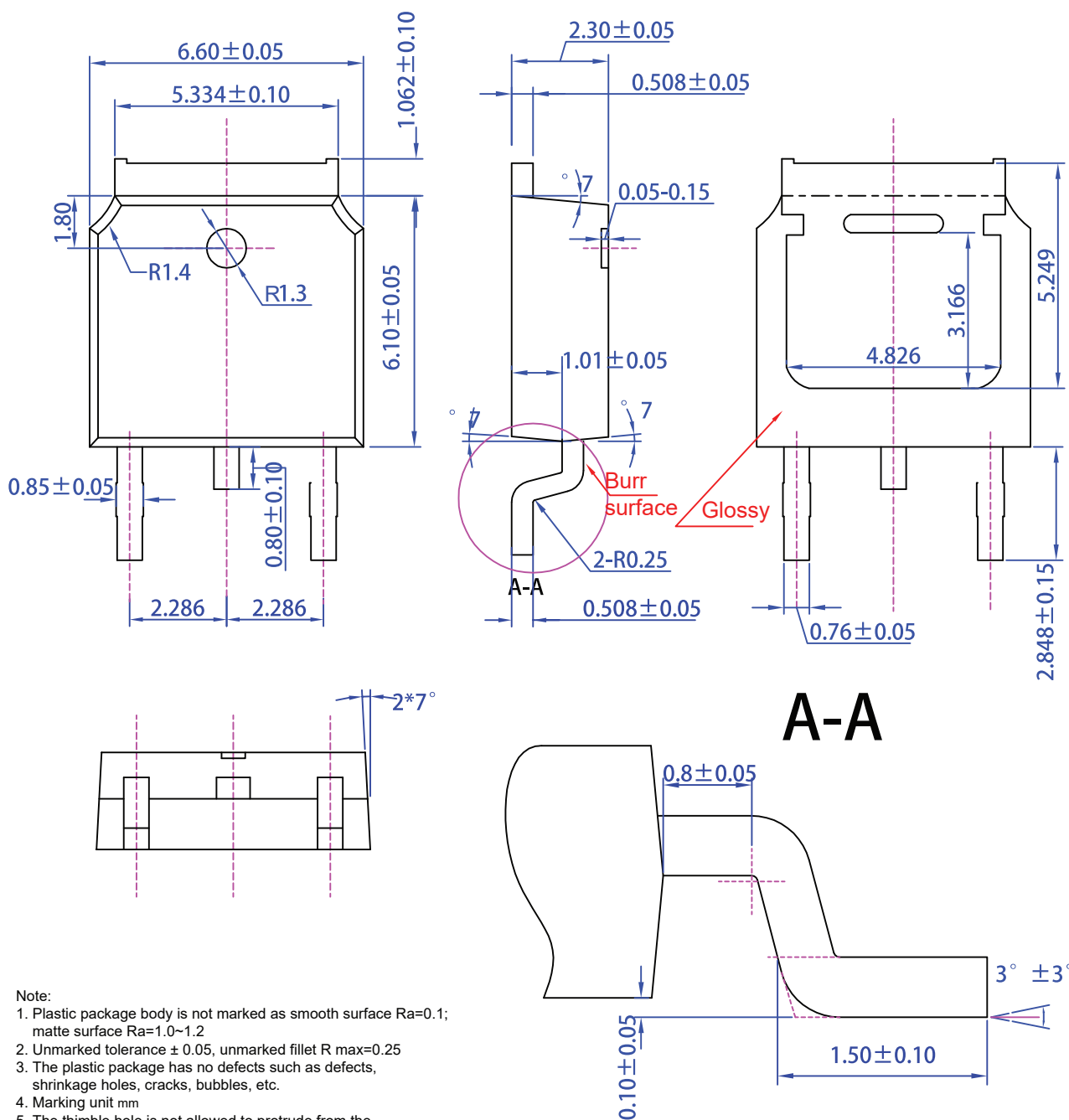


Typical Characteristics



Package Dimension

TO-252



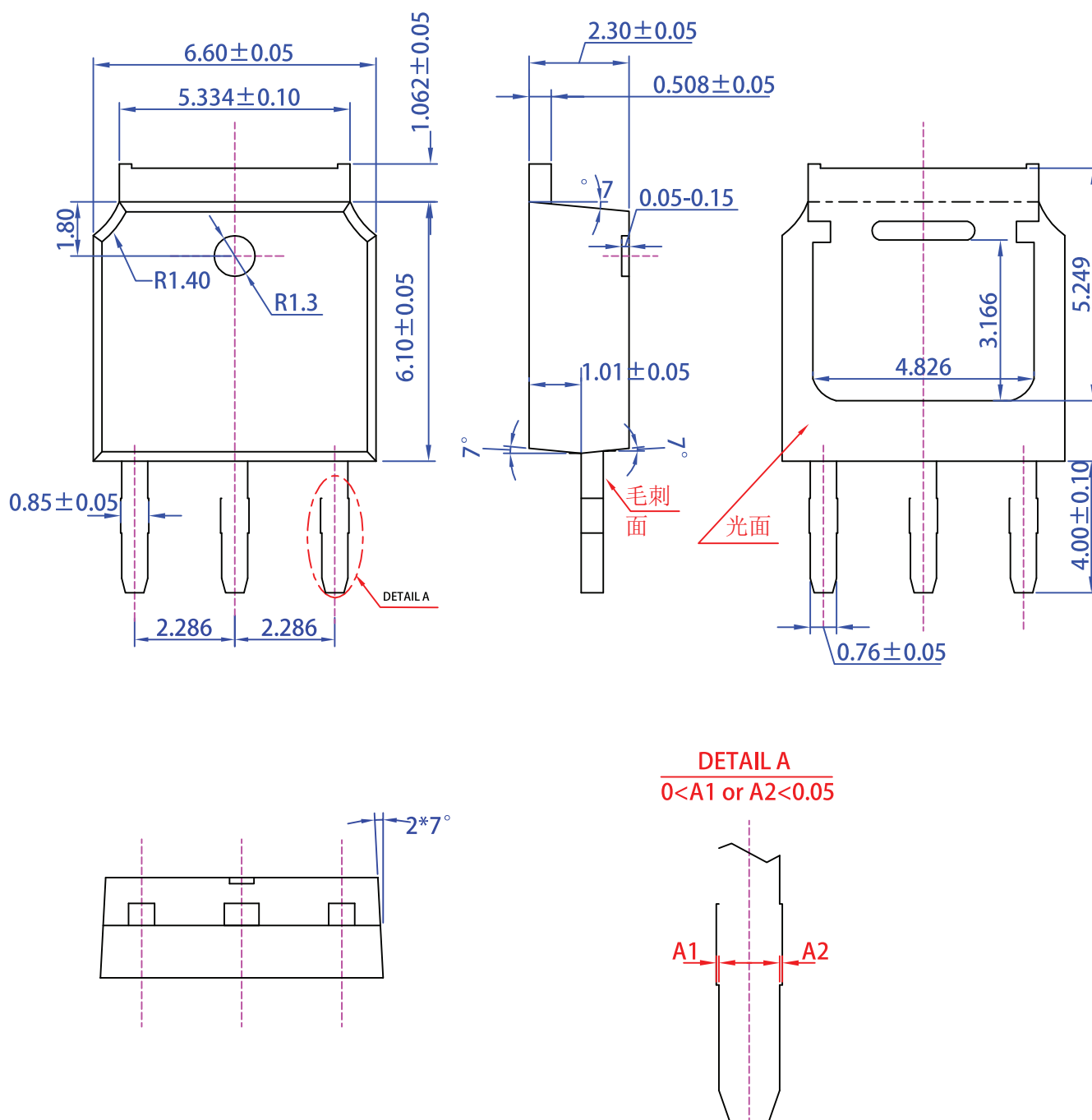
Note:

1. Plastic package body is not marked as smooth surface $Ra=0.1$; matte surface $Ra=1.0\sim 1.2$
2. Unmarked tolerance ± 0.05 , unmarked fillet $R \max=0.25$
3. The plastic package has no defects such as defects, shrinkage holes, cracks, bubbles, etc.
4. Marking unit mm
5. The thimble hole is not allowed to protrude from the surface of the plastic package
6. Dislocation of upper and lower plastic package ≤ 0.05 ; plastic package center and lead Center misalignment of wire frames ≤ 0.05

Package Dimension

TO-251A

Unit :mm



Part Marking Information

