

256-Tap, Single Digital Potentiometer

Features

- ZJC2740-10: 10 k Ω Normal Resistance
- ZJC2740-100: 100 k Ω Normal Resistance
- 256 Tap Position Variable Resistance Device
- SPI™ Serial Interface (mode 0,0 and 1,1)
- INL: ± 0.25 LSB
- DNL: ± 0.15 LSB
- Single Supply: 2.7 V ~ 5.5 V
- 3-Wire SPI™-Interface Compatible
- Package: SOIC-8
- Extended Temperature Range: -40 °C to +125 °C

Applications

- Precision Data Acquisition
- Automated Testing
- Precision Instrument
- Medical Instrument

General Description

The ZJC2740 device is a 256-position digital potentiometers available in 10 k Ω or 100 k Ω resistance version. The ZJC2740 is in an 8-pin SOIC package. The wiper position of the ZJC2740 varies linearly and is controlled via an industry-standard SPI interface. A software shutdown feature is provided that disconnects the “A” terminal from the resistor stack and simultaneously connects the wiper to the “B” terminal. During shutdown mode, the contents of the wiper register can be changed and the potentiometer returns from shutdown to the new value. The wiper is reset to the mid-scale position (0x80) upon power-up. These devices operate from a single 2.7 V ~ 5.5 V supply and are specified over the extended and industrial temperature ranges.

Block Diagram

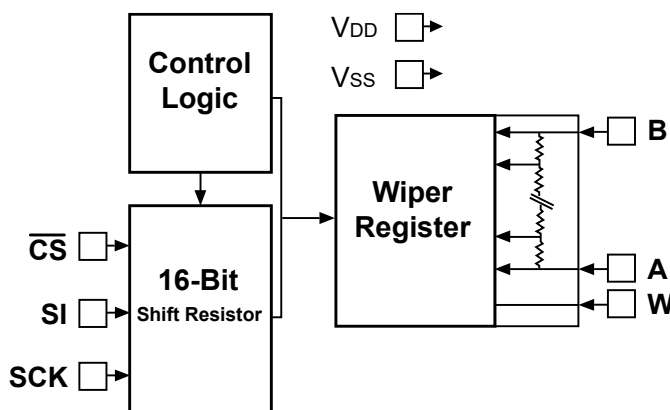


Figure 1. Block Diagram

Typical Characteristics

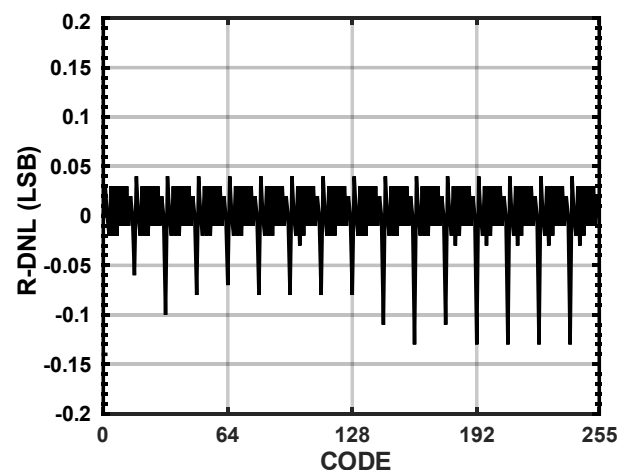


Figure 2. R-DNL vs. Code (10 k Ω)

Table of Contents

Features	1	DC Characteristics: $R_{AB} = 100\text{ k}\Omega$	8
Applications	1	Timing Specifications	10
General Description	1	Typical Performance Characteristics	11
Block Diagram	1	Serial Interface	13
Typical Characteristics	1	Command Byte	13
Table of Contents	2	Writing Data to Data Registers	13
Version (Release A)	3	Programming the Variable Resistor	14
Pin Configurations and Function Descriptions	4	Programming The Potentiometer Divider	15
Absolute Maximum Ratings	5	Outline Dimensions	16
Thermal Resistance	5	Ordering Guide	17
Specifications	6	Product Order Model	17
DC Characteristics: $R_{AB} = 10\text{ k}\Omega$	6	Related Parts	18

Version (Release A)¹

Apr. 2026 — Release A

Update Specifications and Typical Performance Characteristics

Jun. 2025 — Initial

¹ Information furnished by ZJW Microelectronics is believed to be accurate and reliable. However, no responsibility is assumed by ZJW Microelectronics for its use, nor for any infringements of patents or other rights of third parties that may result from its use. Specifications subject to change without notice. No license is granted by implication or otherwise under any patent or patent rights of ZJW Microelectronics. Trademarks and registered trademarks are the property of their respective owners.

Pin Configurations and Function Descriptions

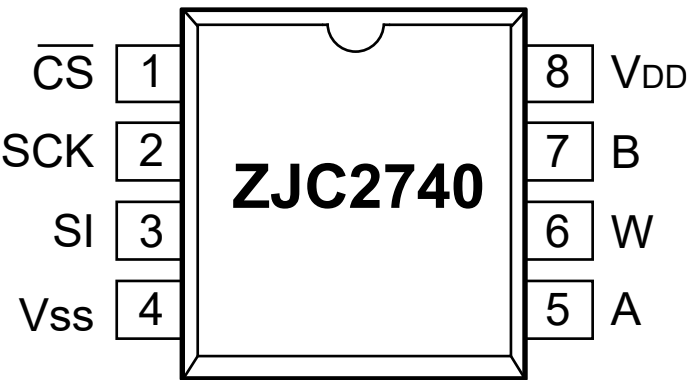


Figure 3. ZJC2740 Pin Configuration (8-lead SOIC)

Mnemonic	Pin No.	I/O ¹	Description
$\overline{\text{CS}}$	1	DI	Chip Select. This is the SPI port chip select pin and is used to execute a new command after it has been loaded into the shift register.
SCK	2	DI	Serial Clock. This is the SPI port clock pin and is used to clock-in new register data. This pin is gated to the $\overline{\text{CS}}$ pin.
SI	3	DI	Serial Data Input. This is the SPI port serial data input pin. The command and data bytes are clocked into the shift register using this pin. This pin is gated to the $\overline{\text{CS}}$ pin.
Vss	4	G	Ground
A	5	AI	Terminal A. Potentiometer Terminal A Connection.
W	6	AI	Wiper. Potentiometer Wiper Connection.
B	7	AI	Terminal B. Potentiometer Terminal B Connection.
VDD	8	P	Power Supply.

¹AI: Analog Input; DI: Digital Input; P: Power; G: Ground;

Absolute Maximum Ratings¹

Parameter	Rating
V _{DD}	6.0 V
All inputs and outputs to V _{SS}	-0.6 V to V _{DD} +0.3 V
Maximum Continuous Current into Pins A, B, and W	5 mA (10 kΩ) 1.5 mA (100 kΩ)
Storage Temperature Range	-60 °C to +150 °C
Junction Temperature Range	150 °C
Reflow Soldering	
Peak Temperature	260 °C
Electrostatic Discharge (ESD) ²	
Human Body Model (HBM) ³	3 kV
Charged Device Model (CDM)	2 kV

Thermal Resistance ⁴

Package Type	θ _{JA}	θ _{JC}	Unit
8-lead SOIC	120	39	°C/W

¹ These ratings apply at 25 °C, unless otherwise noted. Stresses above these ratings may cause permanent damage. Exposure to absolute maximum conditions for extended periods may degrade device reliability. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those specified is not implied.

² Charged devices and circuit boards can discharge without detection.

Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

³ ANSI/ESDA/JEDEC JS-001 Compliant.

⁴ θ_{JA} addresses the conditions for soldering devices onto circuit boards to achieve surface mount packaging.

Specifications

DC Characteristics: $R_{AB} = 10\text{ k}\Omega$

The ● denotes the full temperature range ($-40\text{ }^{\circ}\text{C}$ to $+125\text{ }^{\circ}\text{C}$) for specified performance. Unless otherwise noted, $V_{DD} = 2.7\text{ V}$ to 5.5 V . Typical specifications represent values for $V_{DD} = 5\text{ V}$, $V_{SS} = 0\text{ V}$, $V_B = 0\text{ V}$, $T_A = +25\text{ }^{\circ}\text{C}$.

Parameter	Symbol	Conditions	Min	Typ. ¹	Max	Unit
-----------	--------	------------	-----	-------------------	-----	------

Rheostat Mode

Nominal Resistance ²	R	$T_A = +25\text{ }^{\circ}\text{C}$		10		k Ω
Rheostat Integral Nonlinearity ³	R-INL	$V_{DD} \geq 3.3\text{ V}$	● -0.6	± 0.25	+0.6	
		$V_{DD} < 3.3\text{ V}$	● -0.8	± 0.4	+0.8	LSB
Rheostat Differential Nonlinearity ³	R-DNL		● -0.5	± 0.15	+0.5	LSB
Nominal Resistor Tolerance	$\Delta R_{AB}/R_{AB}$		● -15		+15	%
Resistance Temperature Coefficient	$\Delta R_{AB}/R_{AB}/\Delta T$		●	± 35		ppm/ $^{\circ}\text{C}$
Wiper Resistance	R_W	$V_{DD} = 5.5\text{ V}$, $I_W = 1\text{ mA}$, Code 00h	●	50	100	Ω
Wiper Current	I_W				5	mA

Potentiometer Divider

Resolution	N			8		Bits
Monotonicity	N			8		Bits
Integral Nonlinearity ⁴	INL		● -0.5	± 0.25	+0.5	LSB
Differential Nonlinearity ⁴	DNL		● -0.3	± 0.1	+0.3	LSB
Voltage Divider Temperature Coefficient	$\Delta V_W/V_{AB}/\Delta T$			± 5		ppm/ $^{\circ}\text{C}$
Full Scale Error	V_{WFSE}	Code FFh	● -2.0	-1.2		LSB
Zero Scale Error	V_{WZSE}	Code 00h	●	1.2	2.0	LSB

Resistor Terminals

Terminal Voltage Range ⁵	$V_{A,B,W}$			0	V_{DD}	V
Capacitance (C_A or C_B)	C_A, C_B	$f = 1\text{ MHz}$, Code = 80h			15	pF
Capacitance W	C_W	$f = 1\text{ MHz}$, Code = 80h			15	pF

Dynamic Characteristics (All dynamic characteristics use $V_{DD} = 5\text{ V}$)

-3 dB Bandwidth	BW	$V_B = 0\text{ V}$, Measured at Code 80h, Output Load = 30 pF			3	MHz
Settling Time	T_S	$V_A = V_{DD}$, $V_B = 0\text{ V}$, $\pm 1\%$ Error Band, Transition from Code 00h to Code 80h, Output Load = 30 pF			2	μs
Resistor Noise Voltage	e_{NWB}	$V_A = \text{Open}$, Code 80h, $f = 1\text{ kHz}$			9	nV/ $\sqrt{\text{Hz}}$

¹ Typical values represent average readings at $25\text{ }^{\circ}\text{C}$, $V_{DD} = 5\text{ V}$.

² $V_{AB} = V_{DD}$, no connection on wiper.

³ Rheostat position non-linearity R-INL is the deviation from an ideal value measured between the maximum resistance and the minimum resistance wiper positions. R-DNL measures the relative step change from the ideal between successive tap positions. $I_W = 50\text{ }\mu\text{A}$ for $V_{DD} = 3\text{ V}$ and $I_W = 400\text{ }\mu\text{A}$ for $V_{DD} = 5\text{ V}$ for 10 k Ω version.

⁴ INL and DNL are measured at V_W with the device configured in the voltage divider or potentiometer mode. $V_A = V_{DD}$ and $V_B = 0\text{ V}$. DNL specification limits of $\pm 1\text{ LSB}$ max are specified monotonic operating conditions.

⁵ Resistor terminals A, B and W have no restrictions on polarity with respect to each other.

Parameter	Symbol	Conditions	Min	Typ. ¹	Max	Unit
Digital Inputs ($\overline{\text{CS}}$, SCK, SI)						
Schmitt Trigger High-Level Input Voltage	V_{IH}	$V_{DD} = 5\text{ V}$	• $0.7 \times V_{DD}$			V
Schmitt Trigger Low-Level Input Voltage	V_{IL}	$V_{DD} = 5\text{ V}$	•		$0.3 \times V_{DD}$	V
Hysteresis of Schmitt Trigger Inputs	V_{HYS}		• $0.1 \times V_{DD}$			V
Input Leakage Current	I_{LI}	$\overline{\text{CS}} = V_{DD}$, $V_{IN} = V_{SS}$ or V_{DD} , Includes V_A	•		1	μA
Pin Capacitance (All Inputs)	C_{IN}	$V_{DD} = 5.0\text{ V}$, $T_A = +25\text{ }^\circ\text{C}$, $f_C = 1\text{ MHz}$		3		pF
Power Requirements						
Operating Voltage Range	V_{DD}		2.7		5.5	V
Supply Current, Static	I_{DDs}	$\overline{\text{CS}} = V_{DD} = 5.5\text{ V}$		0.2		μA
Power Supply Sensitivity	PSS	Code 80h		-60		dB
Temperature Range						
Specified Performance			-40		+125	$^\circ\text{C}$

DC Characteristics: $R_{AB} = 100\text{ k}\Omega$

The ● denotes the full temperature range ($-40\text{ }^{\circ}\text{C}$ to $+125\text{ }^{\circ}\text{C}$) for specified performance. Unless otherwise noted, $V_{DD} = 2.7\text{ V}$ to 5.5 V . Typical specifications represent values for $V_{DD} = 5\text{ V}$, $V_{SS} = 0\text{ V}$, $V_B = 0\text{ V}$, $T_A = +25\text{ }^{\circ}\text{C}$.

Parameter	Symbol	Conditions	Min	Typ. ¹	Max	Unit
-----------	--------	------------	-----	-------------------	-----	------

Rheostat Mode

Nominal Resistance ²	R	$T_A = +25\text{ }^{\circ}\text{C}$		100		k Ω
Rheostat Integral Nonlinearity ³	R-INL	$V_{DD} \geq 3.3\text{ V}$	● -0.5	± 0.2	+0.5	LSB
		$V_{DD} < 3.3\text{ V}$	● -0.6	± 0.3	+0.6	LSB
Rheostat Differential Nonlinearity ³	R-DNL		● -0.5	± 0.15	+0.5	LSB
Nominal Resistor Tolerance	$\Delta R_{AB}/R_{AB}$		● -15		+15	%
Resistance Temperature Coefficient	$\Delta R_{AB}/R_{AB}/\Delta T$		●	± 10		ppm/ $^{\circ}\text{C}$
Wiper Resistance	R_W	$V_{DD} = 5.5\text{ V}$, $I_W = 1\text{ mA}$, Code 00h	●	50	100	Ω
Wiper Current	I_W				1.5	mA

Potentiometer Divider

Resolution	N			8		Bits
Monotonicity	N			8		Bits
Integral Nonlinearity ⁴	INL		● -0.5	± 0.2	+0.5	LSB
Differential Nonlinearity ⁴	DNL		● -0.3	± 0.1	+0.3	LSB
Voltage Divider Temperature Coefficient	$\Delta V_W/V_{AB}/\Delta T$			± 5		ppm/ $^{\circ}\text{C}$
Full Scale Error	V_{WFSE}	Code FFh	● -0.5	-0.2		LSB
Zero Scale Error	V_{WZSE}	Code 00h	●	0.15	+0.5	LSB

Resistor Terminals

Terminal Voltage Range ⁵	$V_{A,B,W}$			0	V_{DD}	V
Capacitance (C_A or C_B)	C_A, C_B	$f = 1\text{ MHz}$, Code = 80h			15	pF
Capacitance W	C_W	$f = 1\text{ MHz}$, Code = 80h			15	pF

Dynamic Characteristics (All dynamic characteristics use $V_{DD} = 5\text{ V}$)

-3 dB Bandwidth	BW	$V_B = 0\text{ V}$, Measured at Code 80h, Output Load = 30 pF			0.4	MHz
Settling Time	T_S	$V_A = V_{DD}$, $V_B = 0\text{ V}$, $\pm 1\%$ Error Band, Transition from Code 00h to Code 80h, Output Load = 30 pF			12	μs
Resistor Noise Voltage	e_{NWB}	$V_A = \text{Open}$, Code 80h, $f = 1\text{ kHz}$			28.5	nV/ $\sqrt{\text{Hz}}$

¹ Typical values represent average readings at $25\text{ }^{\circ}\text{C}$, $V_{DD} = 5\text{ V}$.

² $V_{AB} = V_{DD}$, no connection on wiper.

³ Rheostat position non-linearity R-INL is the deviation from an ideal value measured between the maximum resistance and the minimum resistance wiper positions. R-DNL measures the relative step change from the ideal between successive tap positions. $I_W = 5\text{ }\mu\text{A}$ for $V_{DD} = 3\text{ V}$ and $I_W = 40\text{ }\mu\text{A}$ for $V_{DD} = 5\text{ V}$ for 100 k Ω version.

⁴ INL and DNL are measured at VW with the device configured in the voltage divider or potentiometer mode. $V_A = V_{DD}$ and $V_B = 0\text{ V}$. DNL specification limits of $\pm 1\text{ LSB}$ max are specified monotonic operating conditions.

⁵ Resistor terminals A, B and W have no restrictions on polarity with respect to each other.

Parameter	Symbol	Conditions	Min	Typ. ¹	Max	Unit
Digital Inputs ($\overline{\text{CS}}$, SCK, SI)						
Schmitt Trigger High-level Input Voltage	V_{IH}	$V_{DD} = 5\text{ V}$	• $0.7 \times V_{DD}$			V
Schmitt Trigger Low-level Input Voltage	V_{IL}	$V_{DD} = 5\text{ V}$	•		$0.3 \times V_{DD}$	V
Hysteresis of Schmitt Trigger Inputs	V_{HYS}		• $0.1 \times V_{DD}$			V
Input Leakage Current	I_{LI}	$\overline{\text{CS}} = V_{DD}$, $V_{IN} = V_{SS}$ or V_{DD} , Includes V_A			1	μA
Pin Capacitance (All Inputs)	C_{IN}	$V_{DD} = 5.0\text{ V}$, $T_A = +25\text{ }^\circ\text{C}$, $f_c = 1\text{ MHz}$		3		pF
Power Requirements						
Operating Voltage Range	V_{DD}		2.7		5.5	V
Supply Current, Static	I_{DDs}	$\overline{\text{CS}} = V_{DD} = 5.5\text{ V}$		0.2		μA
Power Supply Sensitivity	PSS	Code 80h		-60		dB
Temperature Range						
Specified Performance			-40		+125	$^\circ\text{C}$

Timing Specifications

Unless otherwise specified, $V_{DD} = 2.7\text{ V to }5.5\text{ V}$, $T_A = -40\text{ }^{\circ}\text{C to }+125\text{ }^{\circ}\text{C}$

Parameter	Symbol		Min	Typ.	Max	Unit
Clock Frequency ($V_{DD} = 5\text{ V}$)	F_{CLK}	•			25	MHz
Clock High Time	t_{HI}	•	18			ns
Clock Low Time	t_{LO}	•	18			ns
$\overline{CS}$ Fall to First Rising SCK Edge	t_{CSSR}	•	15			ns
Data Input Setup Time	t_{SU}	•	5			ns
Data Input Hold Time	t_{HD}	•	5			ns
SCK Rise to $\overline{CS}$ Rise Hold Time	t_{CHS}	•	30			ns
SCK Rise to $\overline{CS}$ Fall Delay	t_{CS0}	•	10			ns
$\overline{CS}$ Rise to SCK Rise Hold	t_{CS1}	•	100			ns
$\overline{CS}$ High Time	t_{CSH}	•	10			ns

Data is clocked in on the rising edge of clock. The device will track the number of clocks (rising edges) while $\overline{CS}$ is low and will abort all commands if the number of clocks is not a multiple of 16.

For one frame ($\overline{CS}$ is low) of serial data write operation, if the number of SCK cycles during the chip select low level is multiples of 16, the last 16-bit data is valid, and the redundant high bits are ignored.

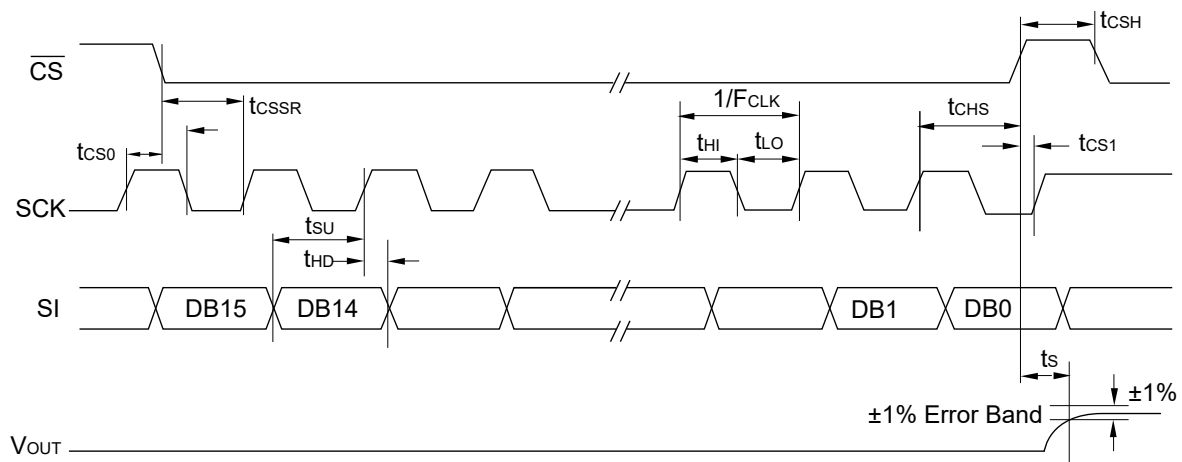


Figure 4. Detailed Serial Interface Timing

Typical Performance Characteristics

Unless otherwise stated, $T_A = 25\text{ }^{\circ}\text{C}$, $V_{DD} = 5.0\text{ V}$.

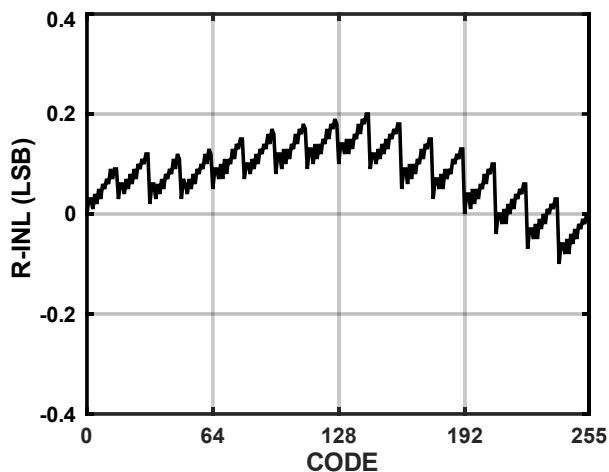


Figure 5. Rheostat-INL vs. Code (10 kΩ)

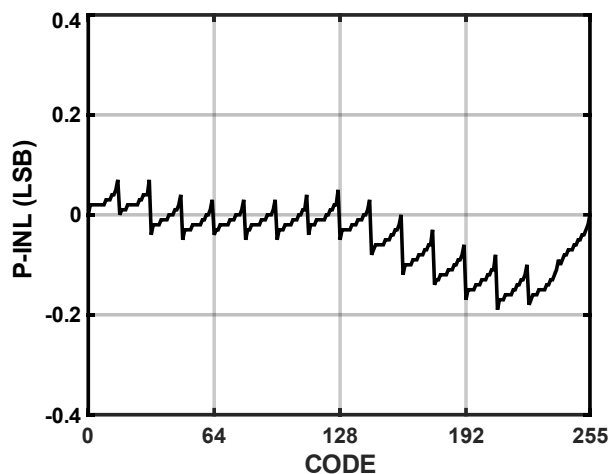


Figure 6. Potentio-INL vs. Code (10 kΩ)

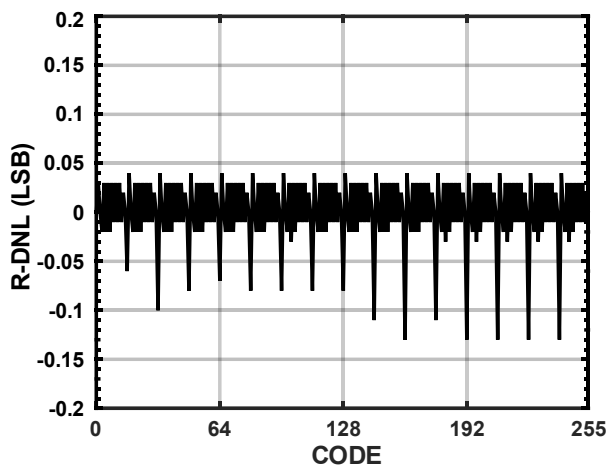


Figure 7. Rheostat-DNL vs. Code (10 kΩ)

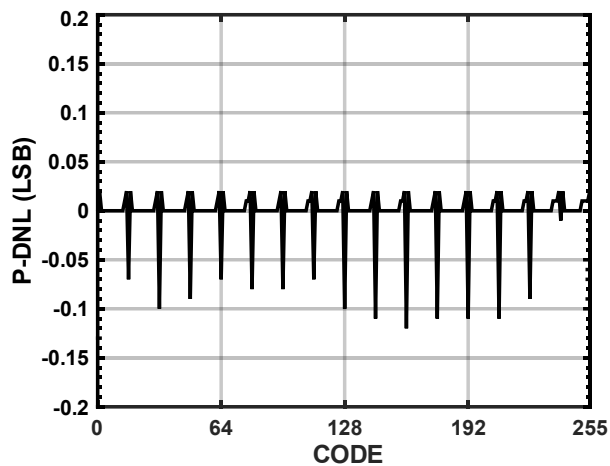


Figure 8. Potentio-DNL vs. Code (10 kΩ)

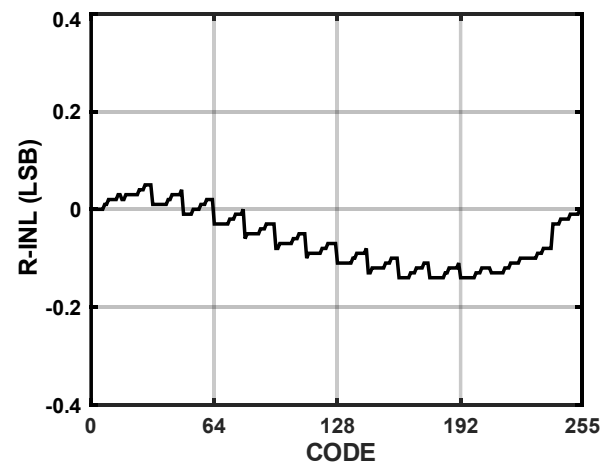


Figure 9. Rheostat-INL vs. Code (100 kΩ)

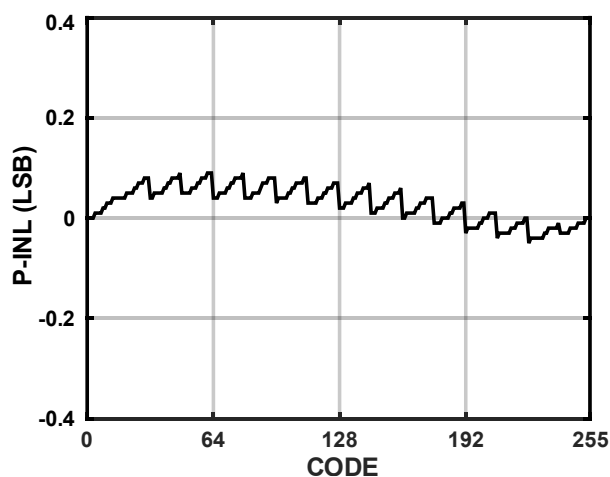
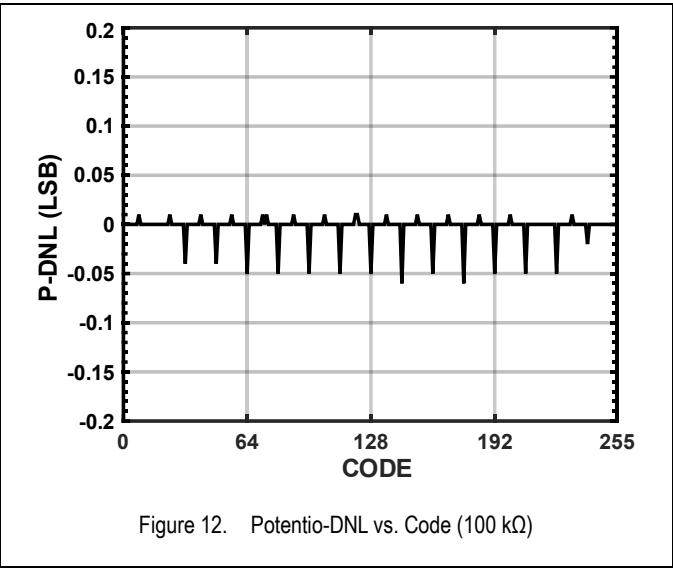
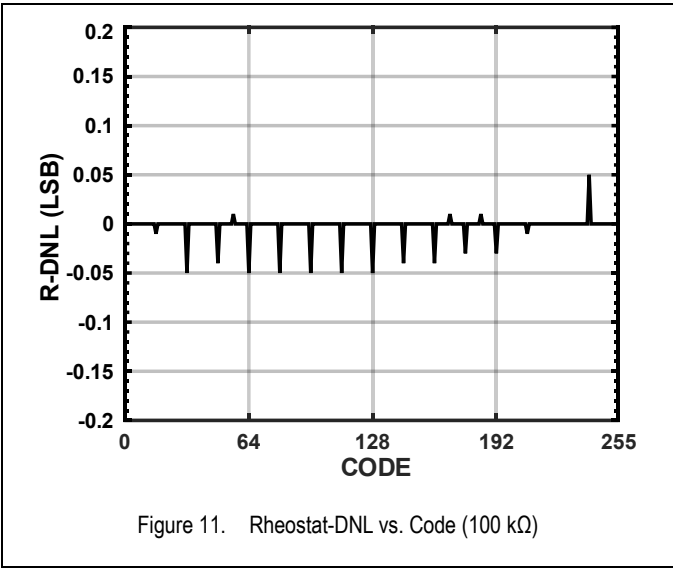


Figure 10. Potentio-INL vs. Code (100 kΩ)



Serial Interface

Communications from the controller to the ZJC2740 digital potentiometers is by using the SPI serial interface.

Executing any command is accomplished by setting $\overline{CS}$ low and then clocking-in a code byte into the shift register. The code is executed when $\overline{CS}$ is raised. Data is clocked in on the rising edge of clock. The device will track the number of clocks (rising edges) while $\overline{CS}$ is low and will abort all commands if the number of clocks is not a multiple of 16.

For one frame ($\overline{CS}$ is low) of serial data write operation, if the number of SCK cycles during the chip select low level is multiple of 16, the last 16-bit data is valid, and the redundant high bits are ignored.

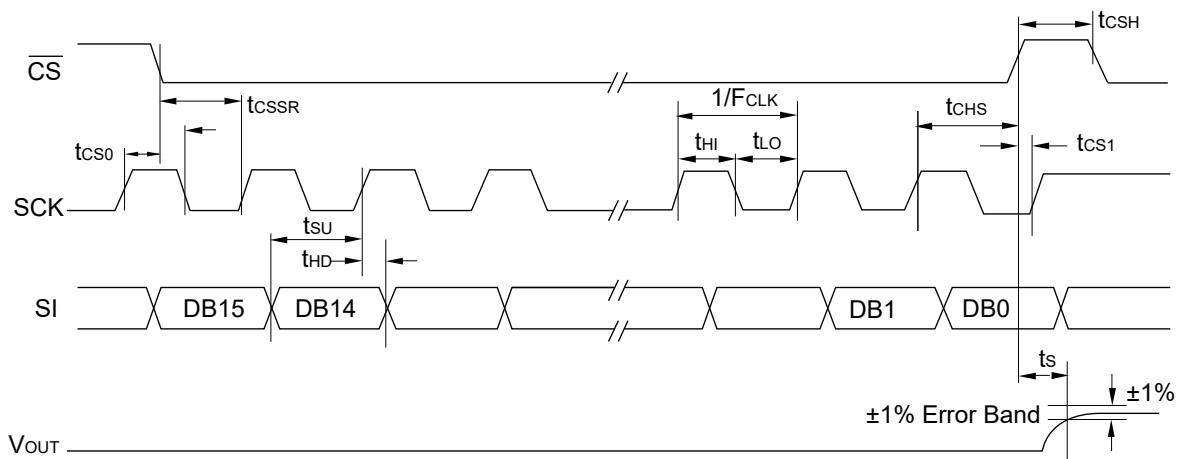


Figure 13. Detailed Serial Interface Timing

Communications from the controller to the ZJC2740 digital potentiometers is by using the SPI serial interface. The SPI allows three commands:

- Write a new value to the potentiometer data register.
- Cause to enter low power shutdown mode.
- NOP (No Operation) command.

Command Byte

The first byte sent is always the command byte, followed by the data byte. The command byte contains two command select bits and two potentiometer select bits. Unused bits are 'don't care' bits. The command select bits C1 and C0 (bits 4:5) of the command byte determine which command will be executed. If the command bits are both 0's or 1's, then a NOP command will be executed once all 16 bits have been loaded.

When the command bits are 0,1, a write command will be executed with the 8 bits sent in the data byte. The data will be written to the potentiometer (s) determined by the potentiometer select bits. If the command bits are C1='1' and C0='0', then a shutdown command will be executed on the potentiometers determined by the potentiometer select bits.

For the ZJC2740 devices, the potentiometer select bits P0 must be '1' to determine the potentiometer to be acted upon by the command.

Writing Data to Data Registers

When new data is written into one or more of the potentiometer data registers, the write command is followed by the data byte for the new value. The command select bits C1, C0 are set to C1='0' and C0='1'.

Command Byte:

X	X	C1	C0	X	X	P1	P0
---	---	----	----	---	---	----	----

C1	C0	Command	Command Summary
0	0	None	No Command will be executed.
0	1	Write Data	Write the data contained in Data Byte to the potentiometer(s) determined by the potentiometer selection bits.
1	0	Shutdown	Potentiometer(s) determined by potentiometer selection bits will enter Shutdown Mode. Data bits for this command are 'don't cares'.
1	1	None	No Command will be executed.

P1	P0	Command Summary
0	0	Invalid.
0	1	Command executed on Potentiometer.
1	0	Invalid.
1	1	Command executed on Potentiometer.

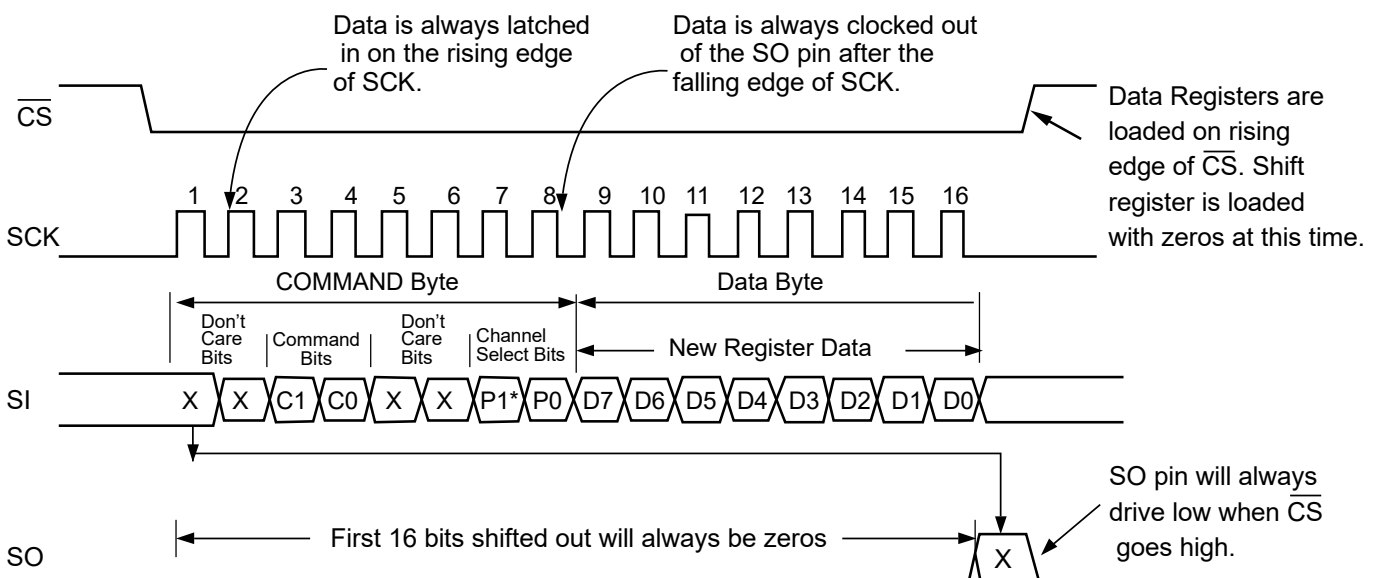


Figure 14. Timing Diagram for Writing Instructions or Data to a Digital Potentiometer (Mode 0)

Programming the Variable Resistor

Rheostat Operation— $\pm 15\%$ Resistor Tolerance

The ZJC2740 operates in rheostat mode when only two terminals are used as a variable resistor. The unused terminal can be floating, or it can be tied to Terminal W.

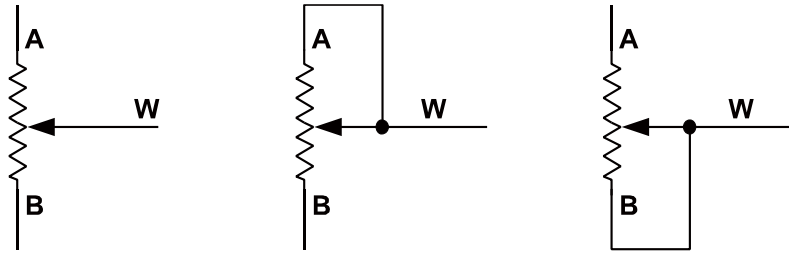


Figure 15. Rheostat Mode Configuration

The nominal resistance between Terminal A and Terminal B, R_{AB} , is 10 k Ω or 100 k Ω , and has 256 tap points accessed by the wiper terminal. The 8-bit data in the RDAC latch is decoded to select one of the 256 possible wiper settings. The general equations for determining the digitally programmed output resistance between Terminal W and Terminal B are

$$R_{WB}(D) = \frac{D}{256} \times R_{AB} + R_W \text{ From } 0x00 \text{ to } 0xFF$$

where:

- D is the decimal equivalent of the binary code in the 8-bit RDAC register.
- R_{AB} is the end to end resistance.
- R_W is the wiper resistance.

In potentiometer mode, similar to the mechanical potentiometer, the resistance between Terminal W and Terminal A also produces a digitally controlled complementary resistance, R_{WA} . R_{WA} also gives a maximum of 15% absolute. R_{WA} starts at the maximum resistance value and decreases as the data loaded into the latch increases. The general equations for this operation are

$$R_{AW}(D) = \frac{256 - D}{256} \times R_{AB} + R_W \text{ From } 0x00 \text{ to } 0xFF$$

where:

- D is the decimal equivalent of the binary code in the 8-bit RDAC register.
- R_{AB} is the end to end resistance.
- R_W is the wiper resistance.

Programming The Potentiometer Divider

Voltage Output Operation

The digital potentiometer easily generates a voltage divider at wiper-to-B and wiper-to-A that is proportional to the input voltage at A to B.

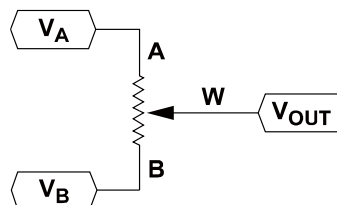


Figure 16. Potentiometer Mode Configuration

$$V_W(D) = \frac{R_{WB}(D)}{R_{AB}} \times V_A + \frac{R_{AW}(D)}{R_{AB}} \times V_B$$

Operation of the digital potentiometer in the divider mode results in a more accurate operation over temperature. The output voltage is dependent mainly on the ratio of the internal resistors, R_{AW} and R_{WB} , and not the absolute values.

Outline Dimensions

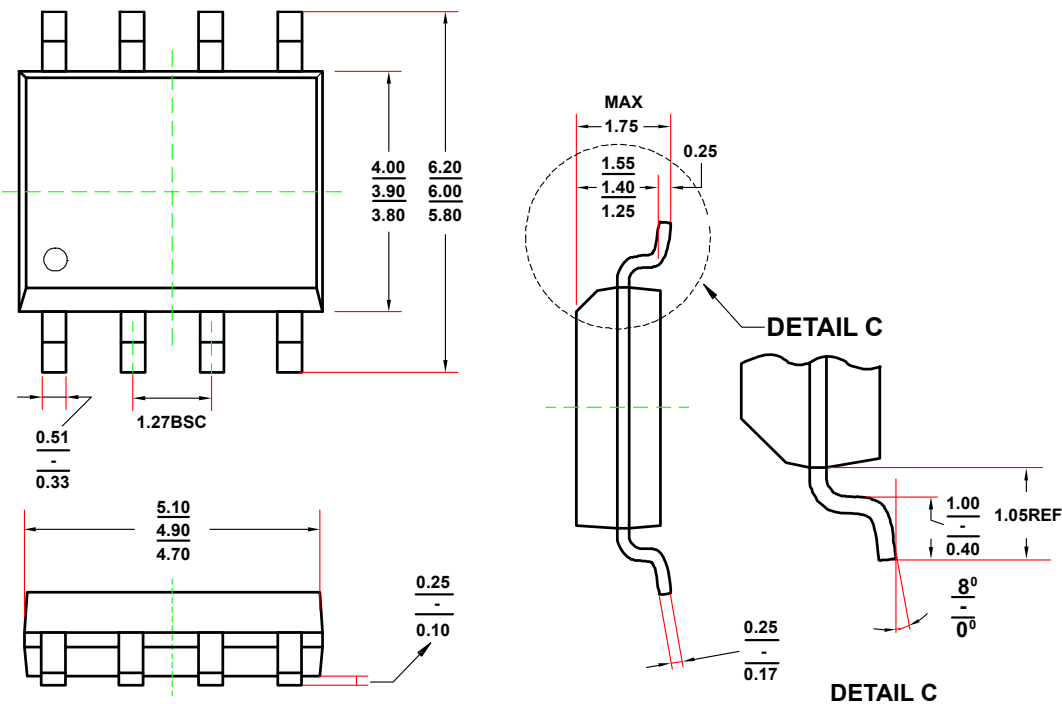


Figure 17. 8-Lead SOIC Package Dimensions shown in millimeters

Ordering Guide

Model	Orderable Device	Package	Marking	Supply Voltage (V)	Temperature Range (°C)	External Package
ZJC2740-10	ZJC2740-10ASABT	SOIC-8	274013	2.7 to 5.5	-40 to +125	Tube
	ZJC2740-10ASABR					13" reel
ZJC2740-100	ZJC2740-100ASABT	SOIC-8	274014	2.7 to 5.5	-40 to +125	Tube
	ZJC2740-100ASABR					13" reel

Product Order Model

ZJXXXXX X X X X X Q1

Q1: Automotive Grade

External Package: T = Tube; R = Reel

Temperature Range: A = -40 °C to 125 °C Automotive Grade 1, B = -40 °C to 125 °C; E = -40 °C to 85 °C

Number of Pins: R = 3; K = 5; T = 6; A = 8; B = 10; D = 14; E = 16; P = 20

Package Type: S = SOIC; U = MSOP, TSSOP, SOT; T = DFN, QFN; X = SC70; W = WLCSP; Z = TSOT23

Grade: B grade is better than A grade

Base: R = Voltage reference; A = Amplifier; C = Data Converter; G = Switches and Multiplexers; M = Others

Related Parts

Part Number	Description	Comments
ADC		
ZJC2020	20-bit 350 kSPS SAR ADC	Fully differential input, SINAD 101.4 dB, THD -118 dB
ZJC2000/2010	18-bit 400 kSPS/200 kSPS SAR ADC	Fully differential input, SINAD 99.3 dB, THD -113 dB
ZJC2001/2011	16-bit 500 kSPS/250 kSPS SAR ADC	Fully differential input, SINAD 95.3 dB, THD -113 dB
ZJC2002/2012	16-bit 500 kSPS/250 kSPS SAR ADC	Pseudo-differential unipolar input, SINAD 91.7 dB, THD -105 dB
ZJC2003/2013		Pseudo-differential bipolar input, SINAD 91.7 dB, THD -105 dB
ZJC2004/2014	18-bit 400 kSPS/200 kSPS SAR ADC	Pseudo-differential unipolar input, SINAD 94.2 dB, THD -105 dB
ZJC2005/2015		Pseudo-differential bipolar input, SINAD 94.2 dB, THD -105 dB
ZJC2007/2017	14-bit 600 kSPS/300 kSPS SAR ADC	Pseudo-differential unipolar input, SINAD 85 dB, THD -105 dB
ZJC2008/2018		Pseudo-differential bipolar input, SINAD 85 dB, THD -105 dB
ZJC2100/1-18	18-bit 400 kSPS/200 kSPS 4-ch differential SAR ADC, SINAD 99.3 dB, THD -113 dB	
ZJC2100/1-16	16-bit 500 kSPS/250 kSPS 4-ch differential SAR ADC, SINAD 95.3 dB, THD -113 dB	
ZJC2102/3-18	18-bit 400 kSPS/200 kSPS 8-ch pseudo-differential SAR ADC, SINAD 94.2 dB, THD -105 dB	
ZJC2102/3-16	16-bit 500 kSPS/250 kSPS 8-ch pseudo-differential SAR ADC, SINAD 91.7 dB, THD -105 dB	
ZJC2102/3-14	14-bit 600 kSPS/300 kSPS 8-ch pseudo-differential SAR ADC, SINAD 85 dB, THD -105 dB	
ZJC2104/5-18	18-bit 400 kSPS/200 kSPS 4-ch pseudo-differential SAR ADC, SINAD 94.2 dB, THD -105 dB	
ZJC2104/5-16	16-bit 500 kSPS/250 kSPS 4-ch pseudo-differential SAR ADC, SINAD 91.7 dB, THD -105 dB	
DAC		
ZJC2541-18/16/14	18/16/14-bit 1 MSPS single channel DAC with unipolar output	Power on reset to 0 V (ZJC2541) or $V_{REF}/2$ (ZJC2543), 1 nV-S glitch, SOIC-8, MSOP-10/8, DFN-10 packages
ZJC2543-18/16/14		
ZJC2542-18/16/14	18/16/14-bit 1 MSPS single channel DAC with bipolar output	Power on reset to 0 V (ZJC2542) or $V_{REF}/2$ (ZJC2544), 1 nV-S glitch, SOIC-14, TSSOP-16, QFN-16 packages
ZJC2544-18/16/14		
Amplifier		
ZJA3000-1/2/4	Single/Dual/Quad 36 V low bias current precision Op Amps	3 MHz, 35 μ V max Vos, 0.5 μ V/°C max TCvos, 25 pA max Ibias, 1 mA/ch, input to V- (ZJA3000 only), RRO, 4.5 V to 36 V
ZJA3001-1/2/4		
ZJA3018-2	OVP ± 75 V, 36 V, Low Power, High Precision Op Amp	1.3 MHz, 10 μ V max Vos, 0.5 μ V/°C max TCvos, 25 pA max Ibias, 0.5 mA/ch, OVP ± 75 V (ZJA3018 only), RRO, 4.5 V to 36 V
ZJA3008-2		
ZJA3512-2	Dual 36 V 7 MHz precision JFET Op Amps	7 MHz, 35 V/ μ S, 50 μ V max Vos, 1 μ V/°C max TCvos, 2 mA/ch, RRO, 9 V to 36 V
ZJA3216/06/02-1/2	Precision 20/10/5 MHz CMOS RRIO Op Amps	20/10/5 MHz, RRIO, 30 μ V max Vos, 1 μ V/°C max TCvos, 0.6 pA Ib, 2.7 V to 5.5 V
ZJA3600/1	36 V ultra-high precision in-amp	CMRR 105 dB min (G = 1), 25 pA max Ib, 25 μ V max Vosi, ± 2.4 V to ± 18 V, -40 °C to 125 °C
ZJA3611, ZJA3609	36 V precision wider bandwidth precision in-amp (G ≥ 10)	CMRR 120 dB min (G = 10), 25 pA max Ibias, 25 μ V max Vosi, 1.2 MHz BW (G = 10)
ZJA3676/7	Low power, G=1 Single/Dual 36 V difference amplifier	Input protection to ± 65 V, CMRR 104 dB min (G = 1), Vos 100 μ V max, gain error 15 ppm max, 500 kHz BW (G = 1), 330 μ A/channel, 2.7 V to 36 V
ZJA3678/9	Low power, G=0.5/2 Single/Dual 36 V difference amplifier	
ZJA3669	High Common-Mode Voltage Difference Amplifier	± 270 V CMV, 2.5 kV ESD, 96 dB min CMRR, 450 kHz BW, 4 V to 36 V, SOIC-8
ZJA3100	15 V precision fully differential amplifier	145 MHz, 447 V/ μ S, 50 nS to 16-bit, 50 μ V max Vos, 4.6 mA Iq, SOIC/MSOP-8, QFN-16
ZJA3236/26/22-2	Low-cost 20/10/5 MHz CMOS RRIO Op Amps	20/10/5 MHz, RRIO, 2 mV max Vos, 6 μ V/°C max TCvos, 0.6 pA Ib, 2.7 V to 5.5 V
ZJA3622/8	36 V low-cost precision in-amp	0.5 nA max Ibias, 125 μ V max Vosi, 625 kHz BW (G = 10), 3.3 mA Iq, ± 2.4 V to ± 18 V
Voltage Reference		
ZJR1004	40 V supply precision voltage reference	$V_{OUT} = 2.048/2.5/3/3.3/4.096/5/10$ V, 5 ppm/°C max drift -40 °C to 125 °C
ZJR1001/2	5.5 V low power voltage reference (ZJR1001 with noise filter option)	$V_{OUT} = 2.048/2.5/3/3.3/4.096/5$ V, 5 ppm/°C max drift -40 °C to 125 °C, $\pm 0.05\%$ initial error, 130 μ A, ZJR1001/2 in SOT23-6, ZJR1003 in SOIC/MSOP-8
ZJR1003		
ZJR1302	5.5 V low power compact precision voltage reference	$V_{OUT} = 2.048/2.5/3/3.3/4.096$ V, 30 ppm/°C max drift -40 °C to 125 °C, 130 μ A, SOT23-3
Switches and Multiplexers		
ZJG4438/4439	36 V fault protection 8:1/dual 4:1 multiplexer	Protection to ± 50 V power on & off, latch-up immune, Ron 270 Ω , 14.8 pC, t_{ON} 166 nS
ZJG4428/4429	36 V 8:1/dual 4:1 multiplexer	Latch-up immune, Ron 270 Ω , 14.8 pC charge injection, t_{ON} 166 nS
Quad Matching Resistor		
ZJM5400	± 75 V precision match resistors	Mismatch < 100 ppm, 10k:10k:10k:10k, 100k:100k:100k:100k, 100k:10k:10k:100k, 1k:1k:1k:1k, 1M:1M:1M:1M, 5k:1k:1k:5k, 5k:1.25k:1.25k:5k, 9k:1k:1k:9k, ESD: 3.5 kV