Quad Channel, 256 Position, I2C, Digital Potentiometer

Features

- ZJC2743-10: 10 kΩ Normal Resistance
- ZJC2743-100: 100 kΩ Normal Resistance
- Resistor Tolerance: 15% max
- Wiper Current: ±6 mA max
- Low Temperature Coefficient: ±35 ppm/°C
- Wide Bandwidth: 3 MHz (10 kΩ)
- Single Supply Operation: 2.7 V ~ 5.5 V
- Wide Operating Temperature: −40 °C to +125 °C
- Package: QFN-16 (3 mm × 3 mm)

Applications

- Portable Electronics Level Adjustment
- LCD Panel Brightness and Contrast Controls
- Programmable Filters, Delays, and Time Constants
- Programmable Power Supplies

General Description

The ZJC2743 potentiometers provide solution for 256-position adjustment applications, offering guaranteed low resistor tolerance errors of ±15% (max) and up to ±6 mA (max) current density in the Ax, Bx, and Wx pins.

The low resistor tolerance and low nominal temperature coefficient simplify open-loop applications as well as applications requiring tolerance matching.

The high bandwidth and low total harmonic distortion (THD) ensure optimal performance for ac signals, making the devices suitable for filter design.

The low wiper resistance of only 50 Ω at the ends of the resistor array allows for pin-to-pin connection.

The wiper values can be set through an I²C-compatible digital interface that also reads back the wiper register.

The ZJC2743-10 or ZJC2473-100 is available in a compact, 16-pin QFN package (3 mm × 3 mm). The devices are guaranteed to operate over the extended industrial temperature range of −40°C to +125°C.

Block Diagram

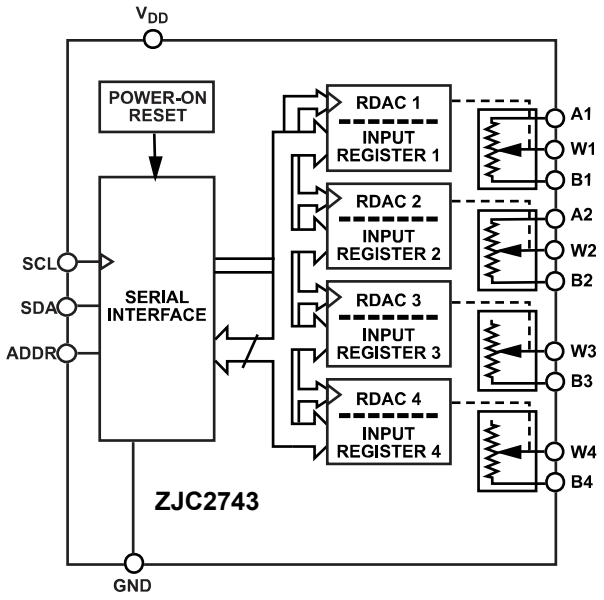

Figure 1. Block Diagram

Typical Characteristics

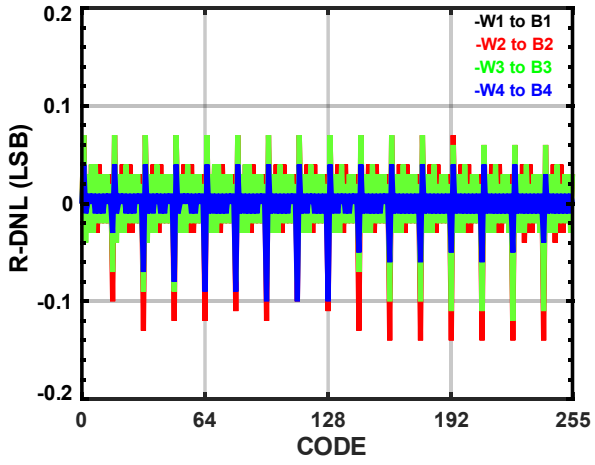

Figure 2. ZJC2743-10 R-DNL vs. Code

Table of Contents

Version (Release B)[1]

Apr. 2026 — Release B

Update Specifications

Mar. 2026 — Release A

Jul. 2025 — Initial

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Pin Configurations and Function Descriptions

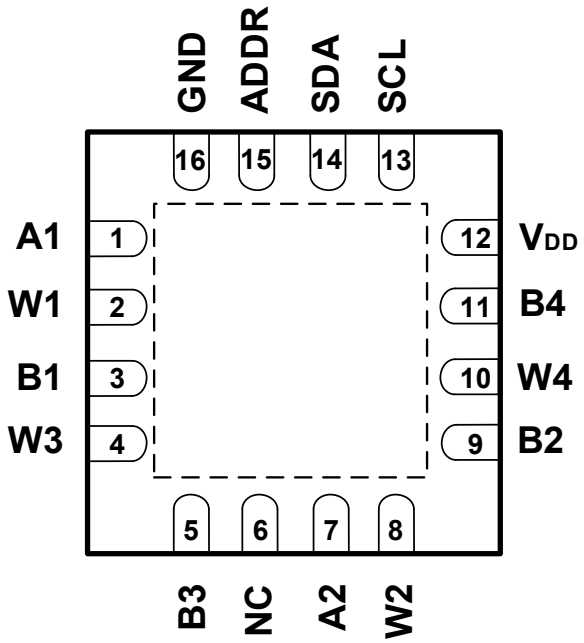

Figure 3. ZJC2743 Pin Configuration (16-lead QFN)

Mnemonic	Pin No.	I/O[1]	Description
A1	1	AI/O	Terminal A of RDAC1. GND ≤ V_A ≤ V_{DD}.
W1	2	AI/O	Wiper Terminal of RDAC1. GND ≤ V_W ≤ V_{DD}.
B1	3	AI/O	Terminal B of RDAC1. GND ≤ V_B ≤ V_{DD}.
W3	4	AI/O	Wiper Terminal of RDAC3. GND ≤ V_W ≤ V_{DD}.
B3	5	AI/O	Terminal B of RDAC3. GND ≤ V_B ≤ V_{DD}.
NC	6	NC	No Internal Connection.
A2	7	AI/O	Terminal A of RDAC2. GND ≤ V_A ≤ V_{DD}.
W2	8	AI/O	Wiper Terminal of RDAC2. GND ≤ V_W ≤ V_{DD}.
B2	9	AI/O	Terminal B of RDAC2. GND ≤ V_B ≤ V_{DD}.
W4	10	AI/O	Wiper Terminal of RDAC4. GND ≤ V_W ≤ V_{DD}.
B4	11	AI/O	Terminal B of RDAC4. GND ≤ V_B ≤ V_{DD}.
V_{DD}	12	P	Positive Power Supply. Decouple this pin with 0.1 µF ceramic capacitors and 10 µF capacitors.
SCL	13	DI	Serial Clock Line. Data is clocked in at the logic low transition
SDA	14	DI	Serial Data Input/Output.
ADDR	15	DI	Programmable Address for Multiple Package Decoding. (two level standard digital logic)
GND	16	G	Ground Pin, Logic Ground Reference.
EPAD		--	Internally Connect the Exposed Paddle to GND.

[1] AI: Analog Input; AO: Analog Output; P: Power; G: Ground; DI: Digital Input.

Absolute Maximum Ratings [1]

Parameter	Rating
V_{DD} to GND	-0.3 V to +6.0 V
V_A, V_W, V_B to GND	−0.3 V, V_{DD} + 0.3 V or +6 V (whichever is less)
I_A, I_W, I_B	±6 mA
Digital Inputs	-0.3 V to V_{DD} + 0.3 V or +6 V (whichever is less)
Operating Temperature Range, T_A	−40 °C to +125 °C
Storage Temperature Range	-65 °C to +150 °C
Maximum Reflow Temperature [2]	150 °C
Reflow Soldering	
Peak Temperature	260 °C
Time at Peak Temperature	20 sec to 40 sec
Package Power Dissipation	$(T_J \text{ max} - T_A)/\theta_{JA}$
Electrostatic Discharge (ESD) [3]	
Human Body Model (HBM) [4]	2.5 kV
Charged Device Model (CDM)	2.0 kV

Thermal Resistance [5]

Package Type	θ_{JA}	θ_{JC}	Unit
16-lead QFN	51	27	°C/W

[1] These ratings apply at 25 °C, unless otherwise noted. Stresses above these ratings may cause permanent damage. Exposure to absolute maximum conditions for extended periods may degrade device reliability. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those specified is not implied.

[2] IPC/JEDEC J–STD-020 Compliant.

[3] Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

[4] ANSI/ESDA/JEDEC JS-001 Compliant.

[5] θ_{JA} addresses the conditions for soldering devices onto circuit boards to achieve surface mount packaging.

Specifications

DC Characteristics: R_{AB} = 10 kΩ

The ● denotes the full temperature range (-40 °C to +125 °C) for specified performance. Unless otherwise noted, V_{DD} = 2.7 V to 5.5 V; -40 °C < T_A < +125 °C, unless otherwise noted.

Parameter	Symbol	Conditions		Min	Typ.[1]	Max	Unit
DC Characteristics—Rheostat Mode (All RDACs)							
Resolution	N	T_A = +25 °C		8			bits
Rheostat Integral Nonlinearity [2]	R-INL	V_{DD} ≥ 3.3 V	●	-0.6	±0.3	+0.6	LSB
		V_{DD} < 3.3 V	●	-0.9	±0.4	+0.9	LSB
Rheostat Differential Nonlinearity [2]	R-DNL		●	-0.5	±0.15	+0.5	LSB
Nominal Resistor Tolerance	Δ R_{AB}/R_{AB}		●	-15		+15	%
Resistance Temperature Coefficient [3]	$(\Delta R_{AB}/R_{AB})/\Delta T \times 10^6$		●		±35		ppm/°C
Wiper Resistance [3]	R_W		●		50	100	Ω
Nominal Resistance Match	R_{AB1} or R_{AB2}		●	-1	±0.2	+1	%
DC Characteristics—Potentiometer Divider Mode (All RDACs)							
Integral Nonlinearity [4]	INL		●	-0.5	±0.15	+0.5	LSB
Differential Nonlinearity [4]	DNL		●	-0.3	±0.1	+0.3	LSB
Full Scale Error	V_{WFSE}		●	-2	-1.2		LSB
Zero Scale Error	V_{WZSE}		●		1.2	2.0	LSB
Voltage Divider Temperature Coefficient [3]	$(\Delta V_W/V_W)/\Delta T \times 10^6$	Code = Half Scale			±5		ppm/°C
Resistor Terminals							
Maximum Continuous Current	I_A, I_B, and I_W		●	-6		6	mA
Terminal Voltage Range [5]				GND		V_{DD}	V
Capacitance A/B [3]	C_A, C_B	f = 1 MHz, measured to GND, Code = Half Scale			15		pF
Capacitance W [3]	C_W	f = 1 MHz, measured to GND, Code = Half Scale			15		pF
Common-mode Leakage Current		$V_A = V_W = V_B$	●		±15		nA
Digital Input							
Input Logic [3]							
High	V_{INH}		●	0.7× V_{DD}			V
Low	V_{INL}		●			0.3× V_{DD}	V
Input Hysteresis [3]	V_{HYST}		●	0.1× V_{DD}			V
Input Current [3]	I_{IN}		●			1	μA
Input Capacitance [3]	C_{IN}				3		pF

[1] Typical values represent average readings at 25 °C, V_{DD} = 5 V.
[2] Rheostat position non-linearity R-INL is the deviation from an ideal value measured between the maximum resistance and the minimum resistance wiper positions. R-DNL measures the relative step change from the ideal between successive tap positions. The maximum wiper current is limited to (0.7 × V_{DD})/R_{AB}.
[3] Guaranteed by design and characterization, not subject to production test.
[4] INL and DNL are measured at V_W with the device configured in the voltage divider or potentiometer mode. V_A = V_{DD} and V_B = 0 V.
[5] Resistor Terminal A, Resistor Terminal B, and Resistor Terminal W have no limitations on polarity with respect to each other.

Parameter	Symbol	Conditions		Min	Typ.[1]	Max	Unit
Digital Outputs							
Output High Voltage [6]	V_{OH}	$R_{PULL-UP}$ = 2.2 kΩ to V_{DD}	•			V_{DD}	V
Output Low Voltage [6]	V_{OL}	I_{SINK} = 3 mA	•			0.4	V
		I_{SINK} = 6 mA	•			0.6	V
Three-State Leakage Current			•	-1		+1	µA
Three-State Output Capacitance					3		pF
Power Supplies							
Power Supply Range	V_{DD}		•	2.7		5.5	V
Power Supply Current	I_{DD}	V_{IH} = V_{DD} or V_{IL} = GND	•		0.2		µA
Power Dissipation	P_{DISS}	V_{IH} = V_{DD} or V_{IL} = GND			1.1		µW
Power Supply Rejection Ratio	PSRR	ΔV_{DD} = V_{DD} ± 10%, Code = Full Scale	•		-60		dB
Dynamic Characteristics							
−3 dB Bandwidth	BW				3		MHz
Total Harmonic Distortion	THD	V_{DD} = 5 V, V_A = 1 V rms, V_B = 0 V, f = 1 kHz			-78		dB
Resistor Noise Density	e_{N_WB}	Code = Half Scale T_A = 25 °C, f = 10 kHz					
		Rheostat Mode			9		nV/√Hz
V_W Settling Time	t_S	V_A = 5 V, V_B = 0 V, from zero scale to full scale, ±0.5 LSB error band					
					2		µS
Analog Crosstalk	C_{TA}				-90		dB

[6] Guaranteed by design and characterization, not subject to production test.

DC Characteristics: R_{AB} = 100 kΩ

The ● denotes the full temperature range (-40 °C to +125 °C) for specified performance. Unless otherwise noted, V_{DD} = 2.7 V to 5.5 V; -40 °C < T_A < +125 °C, unless otherwise noted.

Parameter	Symbol	Conditions		Min	Typ.[1]	Max	Unit
DC Characteristics—Rheostat Mode (All RDACs)							
Resolution	N	T_A = +25 °C		8			bits
Rheostat Integral Nonlinearity [2]	R-INL	V_{DD} ≥ 3.3 V	●	-0.5	±0.2	+0.5	LSB
		V_{DD} < 3.3 V	●	-0.6	±0.25	+0.6	LSB
Rheostat Differential Nonlinearity [2]	R-DNL		●	-0.5	±0.1	+0.5	LSB
Nominal Resistor Tolerance	Δ R_{AB}/R_{AB}		●	-15		+15	%
Resistance Temperature Coefficient [3]	$(\Delta R_{AB}/R_{AB})/\Delta T \times 10^6$		●		±10		ppm/°C
Wiper Resistance [3]	R_W		●		50	100	Ω
Nominal Resistance Match	R_{AB1} or R_{AB2}		●	-1	±0.2	+1	%
DC Characteristics—Potentiometer Divider Mode (All RDACs)							
Integral Nonlinearity [4]	INL		●	-0.5	±0.1	+0.5	LSB
Differential Nonlinearity [4]	DNL		●	-0.3	±0.1	+0.3	LSB
Full Scale Error	V_{WFSE}		●	-0.5	-0.2		LSB
Zero Scale Error	V_{WZSE}		●		0.15	+0.5	LSB
Voltage Divider Temperature Coefficient [3]	$(\Delta_{VW}/_{VW})/\Delta_T \times 10^6$	Code = Half Scale			±5		ppm/°C
Resistor Terminals							
Maximum Continuous Current	I_A, I_B, and I_W		●	-6		6	mA
Terminal Voltage Range [5]				GND		V_{DD}	V
Capacitance A/B [3]	C_A, C_B	f = 1 MHz, measured to GND, Code = Half Scale			15		pF
Capacitance W [3]	C_W	f = 1 MHz, measured to GND, Code = Half Scale			15		pF
Common-mode Leakage Current		V_A = V_W = V_B	●		±15		nA
Digital Input							
Input Logic [3]							
High	V_{INH}		●	0.7× V_{DD}			V
Low	V_{INL}		●			0.3× V_{DD}	V
Input Hysteresis [3]	V_{HYST}		●	0.1× V_{DD}			V
Input Current [3]	I_{IN}		●			1	μA
Input Capacitance [3]	C_{IN}				3		pF

[1] Typical values represent average readings at 25 °C, V_{DD} = 5 V.
[2] Rheostat position non-linearity R-INL is the deviation from an ideal value measured between the maximum resistance and the minimum resistance wiper positions. R-DNL measures the relative step change from the ideal between successive tap positions. The maximum wiper current is limited to (0.7 × V_{DD})/R_{AB}.
[3] Guaranteed by design and characterization, not subject to production test.
[4] INL and DNL are measured at V_W with the device configured in the voltage divider or potentiometer mode. V_A = V_{DD} and V_B = 0 V.
[5] Resistor Terminal A, Resistor Terminal B, and Resistor Terminal W have no limitations on polarity with respect to each other.

Parameter	Symbol	Conditions		Min	Typ.[1]	Max	Unit
Digital Outputs							
Output High Voltage [6]	V_{OH}	$R_{PULL-UP}$ = 2.2 kΩ to V_{DD}	●			V_{DD}	V
Output Low Voltage [6]	V_{OL}	I_{SINK} = 3 mA	●			0.4	V
		I_{SINK} = 6 mA	●			0.6	V
Three-State Leakage Current			●	-1		+1	µA
Three-State Output Capacitance					3		pF
Power Supplies							
Power Supply Range	V_{DD}		●	2.7		5.5	V
Power Supply Current	I_{DD}	V_{IH} = V_{DD} or V_{IL} = GND	●		0.2		µA
Power Dissipation	P_{DISS}	V_{IH} = V_{DD} or V_{IL} = GND			1.1		µW
Power Supply Rejection Ratio	PSRR	ΔV_{DD} = V_{DD} ± 10%, Code = Full Scale	●		-60		dB
Dynamic Characteristics							
−3 dB Bandwidth	BW				0.4		MHz
Total Harmonic Distortion	THD	V_{DD} = 5 V, V_A = 1 V rms, V_B = 0 V, f = 1 kHz			-85		dB
Resistor Noise Density	e_{N_WB}	Code = Half Scale T_A = 25 °C, f = 10 kHz					
		Rheostat Mode			28.5		nV/√Hz
V_W Settling Time	t_S	V_A = 5 V, V_B = 0 V, from zero scale to full scale, ±0.5 LSB error band					
					12		µS
Analog Crosstalk	C_{TA}				-90		dB

[6] Guaranteed by design and characterization, not subject to production test.

Interface Timing Specifications

The ● denotes the full temperature range (-40 °C to +125 °C) for specified performance. Unless otherwise noted, V_{DD} = 2.7 V to 5.5 V; -40 °C < T_A < +125 °C, unless otherwise noted.

Parameter [1]	Mode	Symbol		Min	Typ.	Max	Unit
Serial Clock Frequency	Standard	f_{SCL}[2]	●			100	kHz
	Fast		●			400	kHz
SCL high time, t_{HIGH}	Standard	t_1	●	4.0			ns
	Fast		●	0.6			ns
SCL low time, t_{LOW}	Standard	t_2	●	4.7			ns
	Fast		●	1.3			ns
Data setup time, $t_{SU;\,DAT}$	Standard	t_3	●	250			ns
	Fast		●	100			ns
Data hold time, $t_{HD;\,DAT}$	Standard	t_4	●	0.1		3.45	µs
	Fast		●	0.1		0.9	µs
Setup time for a repeated start condition, $t_{SU;\,STA}$	Standard	t_5	●	4.7			µs
	Fast		●	0.6			µs
Hold time (repeated) for a start condition, $t_{HD;\,STA}$	Standard	t_6	●	4			µs
	Fast		●	0.6			µs
Bus free time between a stop and a start condition, t_{BUF}	Standard	t_7	●	4.7			µs
	Fast		●	1.3			µs
Setup time for a stop condition, $t_{SU;\,STO}$	Standard	t_8	●	4			µs
	Fast		●	0.6			µs
Rise time of SDA signal, t_{RDA}	Standard	t_9	●			1000	ns
	Fast		●	20+0.1C_L		300	ns
Fall time of SDA signal, t_{FDA}	Standard	t_{10}	●			300	ns
	Fast		●	20+0.1C_L		300	ns
Rise time of SCL signal, t_{RCL}	Standard	t_{11}	●			1000	ns
	Fast		●	20+0.1C_L		300	ns
Fall time of SCL signal, t_{FCL}	Standard	t_{12}	●			300	ns
	Fast		●	20+0.1C_L		300	ns

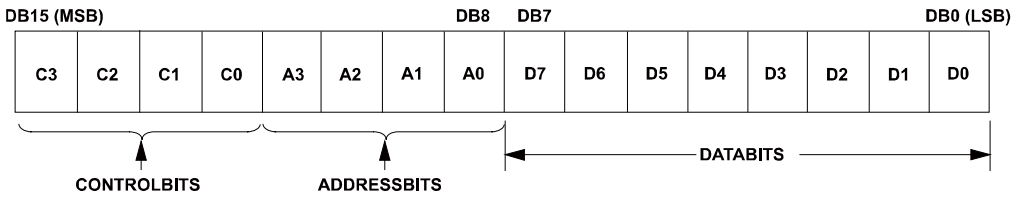

Figure 4. Input Shift Register Contents

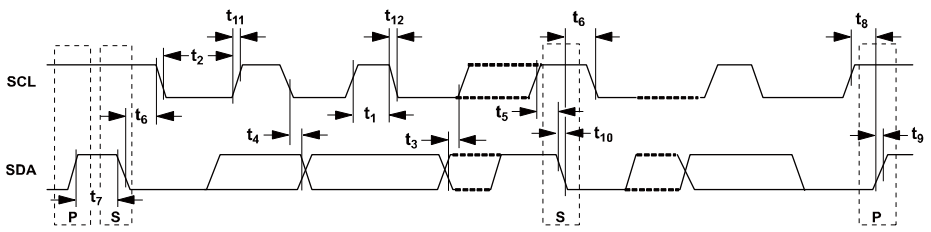

Figure 5. I²C Serial Interface Timing Diagram (Typical Write Sequence)

[1] Maximum bus capacitance is limited to 400 pF.
[2] The SDA and SCL timing is measured with the input filters always enabled.

Typical Performance Characteristics

Unless otherwise stated, T_A = 25 °C, V_{DD} = 5.0 V.

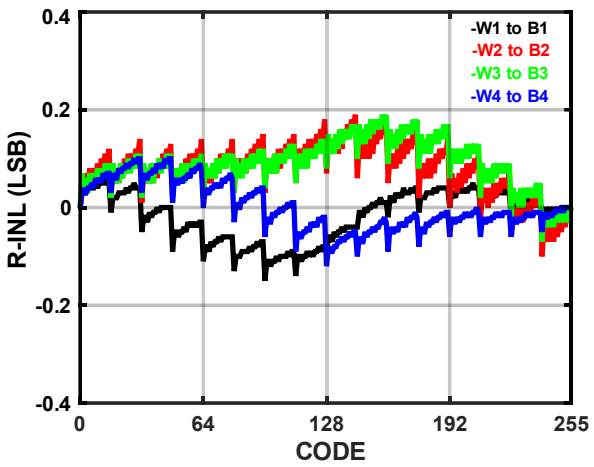

Figure 6. Rheostat-INL vs. Code (10 kΩ)

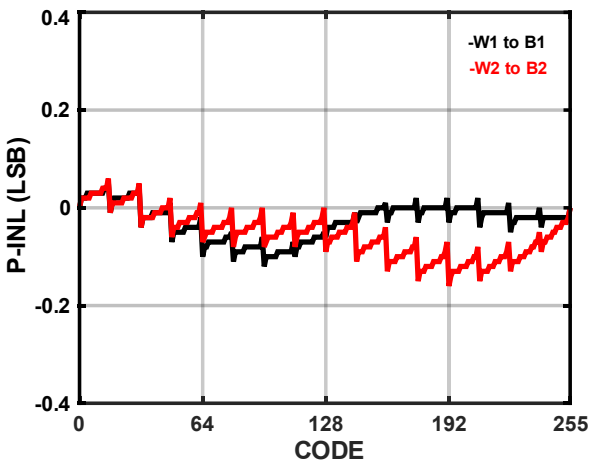

Figure 7. Potentio-INL vs. Code (10 kΩ)

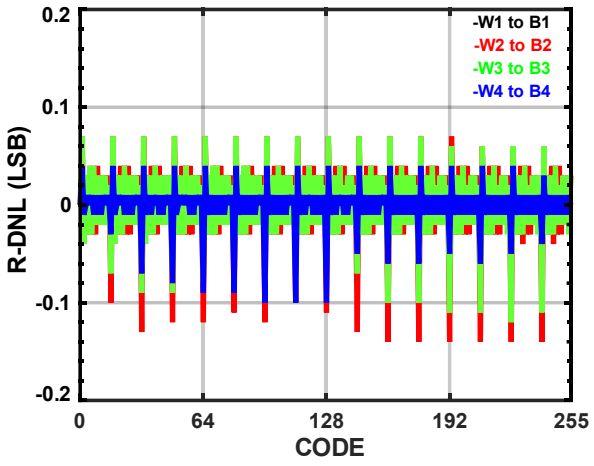

Figure 8. Rheostat-DNL vs. Code (10 kΩ)

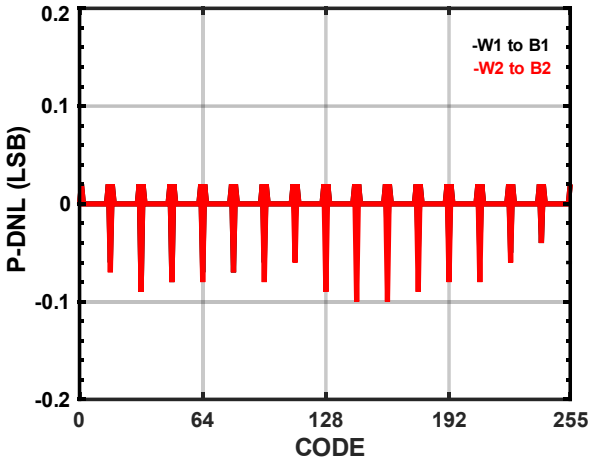

Figure 9. Potentio-DNL vs. Code (10 kΩ)

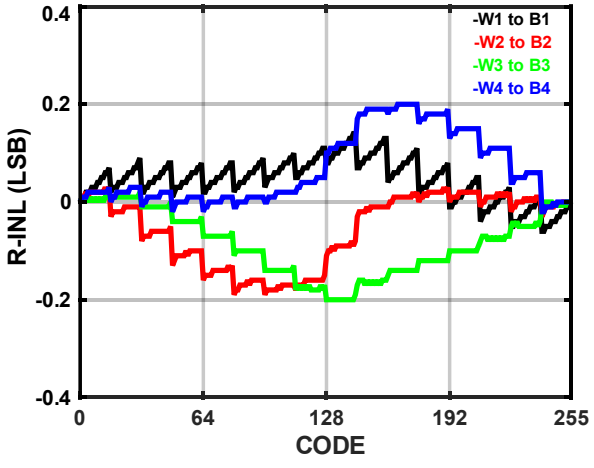

Figure 10. Rheostat-INL vs. Code (100 kΩ)

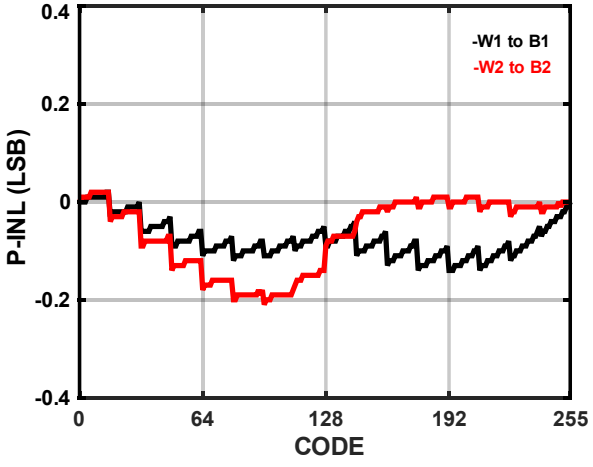

Figure 11. Potentio-INL vs. Code (100 kΩ)

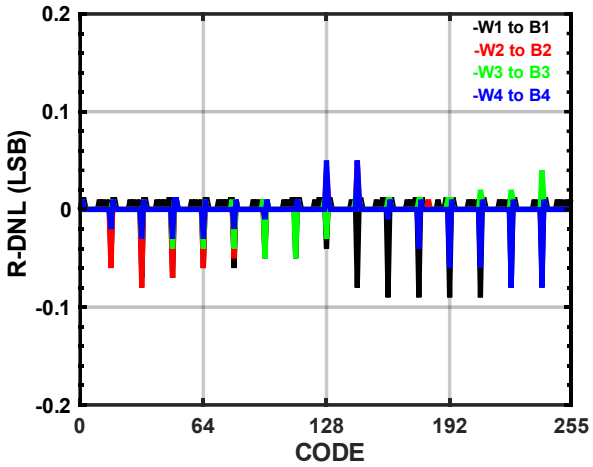

Figure 12. Rheostat-DNL vs. Code (100 kΩ)

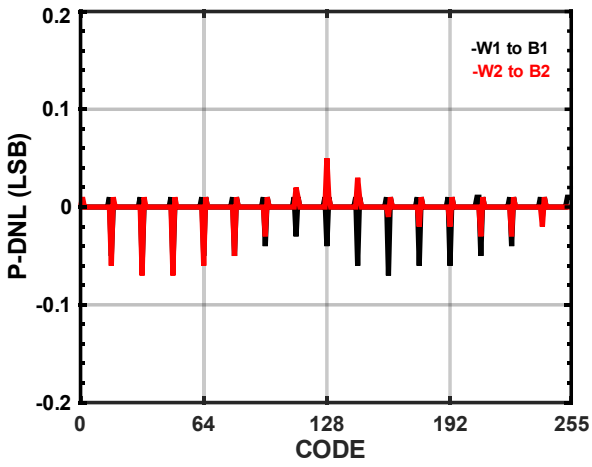

Figure 13. Potentio-DNL vs. Code (100 kΩ)

Theory of Operation

The facility to make hardwired changes to ADDR allows the user to incorporate two of these devices on one bus as outlined in Table 1.

ADDR Pin	7-Bit I²C Device Address
V_{DD}	0101000
GND	0101011

Table 1. I²C Address Selection

Control Modes

The ZJC2743 digital potentiometers include a set of user programming features to address the wide number of applications for these universal adjustment devices (see Table 1 and Table 4).

Key programming features include the following:

- Input register
- Low wiper resistance feature
- ±6 dB increment and decrement instructions
- Burst mode
- Software Reset
- Shutdown mode

Command Number	Control Bits [DB15:DB12]				Address Bits [DB11:DB8] [1]				Data Bits [DB7:DB0] [1]								
	C3	C2	C1	C0	A3	A2	A1	A0	D7	D6	D5	D4	D3	D2	D1	D0	Operation
0	0	0	0	0	X	X	X	X	X	X	X	X	X	X	X	X	NOP: do nothing
1	0	0	0	1	A3	A2	A1	A0	D7	D6	D5	D4	D3	D2	D1	D0	Write contents of serial register data to RDAC
2	0	0	1	0	A3	A2	A1	A0	D7	D6	D5	D4	D3	D2	D1	D0	Write contents of serial register data to input registe
3	0	0	1	1	X	A2	A1	A0	X	X	X	X	X	X	D1	D0	Read back contents D1 D0 Data 0 0 Input register 1 0 Control register 1 1 RDAC
6	0	1	0	1	A3	A2	A1	A0	X	X	X	X	X	X	X	1	+6 dB RDAC increment
7	0	1	0	1	A3	A2	A1	A0	X	X	X	X	X	X	X	0	-6 dB RDAC increment
8	0	1	1	0	A3	A2	A1	A0	X	X	X	X	X	X	X	X	Copy input register to RDAC (software LRDAC)
14	1	0	1	1	X	X	X	X	X	X	X	X	X	X	X	X	Software reset
15	1	1	0	0	A3	A2	A1	A0	X	X	X	X	X	X	X	D0	Software shutdown; D0 = 0: normal mode D0 = 1: device placed in shutdown mode
16	1	1	0	1	X	X	X	X	X	X	X	X	D3	D2	D1	D0	Write data to control registe

Table 2. Advance Commands Operation Truth Table

[1] X means don't care

A3	A2	A1	A0	Input Register	RDAC Register
1	X[1]	X	X	All channels	All channels
0	0	0	0	RDAC1	RDAC1
0	1	0	0	Not applicable	Not applicable
0	0	0	1	RDAC2	RDAC2
0	1	0	1	Not applicable	Not applicable
0	0	1	0	RDAC3	RDAC3
0	1	1	0	Not applicable	Not applicable
0	0	1	1	RDAC4	RDAC4
0	1	1	1	Not applicable	Not applicable

Table 3. Address Bits

Bit Name	Description
D0	0 = reset Input register and RDAC register to midscale (0x80). 1 = allows update of wiper position through digital interface (default
D1	Not used.
D2	Not used.
D3	Burst mode 0 = disabled (default) 1 = enabled (no disable after stop or repeat start condition)

Table 4. Control Register Bit Descriptions

Reset

The ZJC2743 can be reset through software by executing Command 14 (see Table 1). The reset command resets the RDAC registers to midscale code (0x80).

Shutdown Mode

The ZJC2743 can be placed in shutdown mode by executing the software shutdown command, Command 15 (see Table 1), and setting the LSB (D0) to 1. This feature places the RDAC in a zero power consumption state where the device operates in potentiometer mode, Terminal A is open-circuited, and the wiper, Terminal W, is connected to Terminal B; however, a finite wiper resistance is present. The contents of the RDAC register are unchanged by entering shutdown mode.

Programming the Variable Resistor

Rheostat Operation — ±15% Resistor Tolerance

The ZJC2743 operates in rheostat mode when only two terminals are used as a variable resistor. The unused terminal can be floating, or it can be tied to Terminal W, as shown in Figure 14.

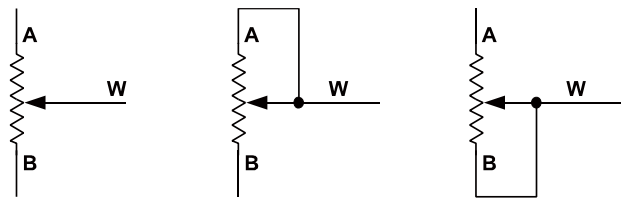

Figure 14. Rheostat Mode Configuration

[1] X means don't care.

The nominal resistance between Terminal A and Terminal B, R_{AB}, is 10 kΩ or 100 kΩ, and has 256 tap points accessed by the wiper terminal. The 8-bit data in the RDAC latch is decoded to select one of the 256 possible wiper settings. The general equations for determining the digitally programmed output resistance between Terminal W and Terminal B are

$$R_{WB}(D) = \frac{D}{256} \times R_{AB} + R_W \quad From\ 0x00\ to\ 0xFF$$

where:

- D is the decimal equivalent of the binary code in the 8-bit RDAC register.
- R_{AB} is the end to end resistance.
- R_W is the wiper resistance.

In potentiometer mode, similar to the mechanical potentiometer, the resistance between Terminal W and Terminal A also produces a digitally controlled complementary resistance, R_{WA}. R_{WA} also gives a maximum of 15% absolute. R_{WA} starts at the maximum resistance value and decreases as the data loaded into the latch increases. The general equations for this operation are

$$R_{AW}(D) = \frac{256 - D}{256} \times R_{AB} + R_W \quad From\ 0x00\ to\ 0xFF$$

where:

- D is the decimal equivalent of the binary code in the 8-bit RDAC register.
- R_{AB} is the end to end resistance.
- R_W is the wiper resistance.

Programming The Potentiometer Divider

Voltage Output Operation

The digital potentiometer easily generates a voltage divider at wiper-to-B and wiper-to-A that is proportional to the input voltage at A to B as shown in Figure 15.

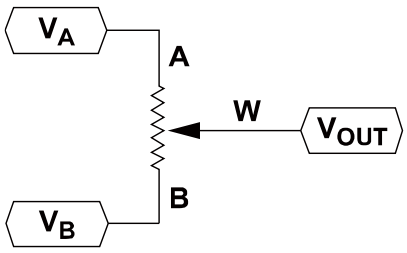

Figure 15. Potentiometer Mode Configuratio

$$V_W(D) = \frac{R_{WB}(D)}{R_{AB}} \times V_A + \frac{R_{AW}(D)}{R_{AB}} \times V_B$$

Operation of the digital potentiometer in the divider mode results in a more accurate operation over temperature. The output voltage is dependent mainly on the ratio of the internal resistors, R_{AW} and R_{WB}, and not the absolute values.

Outline Dimensions

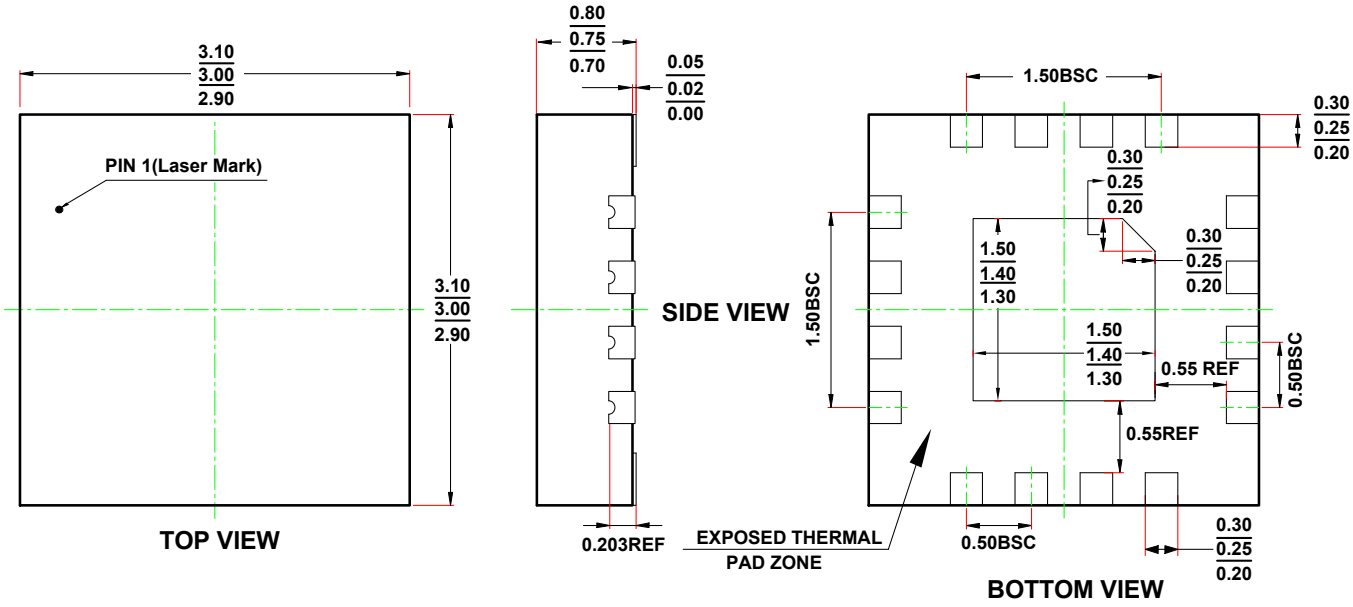

Figure 16. 16-Lead QFN Package Dimensions shown in millimeters

Ordering Guide

Model	Orderable Device	Package	Marking	Supply Voltage (V)	Temperature Range (°C)	External Package
ZJC2743	ZJC2743-10ATEBR	QFN-16	274313	2.7 V to 5.5 V	-40 to +125	13” reel
ZJC2743	ZJC2743-100ATEBR		274314			13” reel

Product Order Model

ZJXXXXX X X X X X Q1

- Q1: Automotive Grade
- External Package: T = Tube; R = Reel
- Temperature Range: A = -40 °C to 125 °C Automotive Grade 1, B = -40 °C to 125 °C; E = -40 °C to 85 °C
- Number of Pins: R = 3; K =5; T = 6, A = 8; B = 10; D = 14; E = 16; P = 20
- Package Type: S = SOIC; U = MSOP, TSSOP, SOT; T = DFN, QFN; X = SC70; W = WLCSP; Z = TSOT23
- Grade: B grade is better than A grade
- Base: R = Voltage reference; A = Amplifier; C = Data Converter; G = Switches and Multiplexers; M = Others

Related Parts

Part Number	Description	Comments
ADC		
ZJC2020	20-bit 350 kSPS SAR ADC	Fully differential input, SINAD 101.4 dB, THD -118 dB
ZJC2000/2010	18-bit 400 kSPS/200 kSPS SAR ADC	Fully differential input, SINAD 99.3 dB, THD -113 dB
ZJC2001/2011	16-bit 500 kSPS/250 kSPS SAR ADC	Fully differential input, SINAD 95.3 dB, THD -113 dB
ZJC2002/2012 ZJC2003/2013	16-bit 500 kSPS/250 kSPS SAR ADC	Pseudo-differential unipolar input, SINAD 91.7 dB, THD -105 dB Pseudo-differential bipolar input, SINAD 91.7 dB, THD -105 dB
ZJC2004/2014 ZJC2005/2015	18-bit 400 kSPS/200 kSPS SAR ADC	Pseudo-differential unipolar input, SINAD 94.2 dB, THD -105 dB Pseudo-differential bipolar input, SINAD 94.2 dB, THD -105 dB
ZJC2007/2017 ZJC2008/2018	14-bit 600 kSPS/300 kSPS SAR ADC	Pseudo-differential unipolar input, SINAD 85 dB, THD -105 dB Pseudo-differential bipolar input, SINAD 85 dB, THD -105 dB
ZJC2100/1-18 ZJC2100/1-16	18-bit 400 kSPS/200 kSPS 4-ch differential SAR ADC, SINAD 99.3 dB, THD -113 dB 16-bit 500 kSPS/250 kSPS 4-ch differential SAR ADC, SINAD 95.3 dB, THD -113 dB	
ZJC2102/3-18 ZJC2102/3-16 ZJC2102/3-14	18-bit 400 kSPS/200 kSPS 8-ch pseudo-differential SAR ADC, SINAD 94.2 dB, THD -105 dB 16-bit 500 kSPS/250 kSPS 8-ch pseudo-differential SAR ADC, SINAD 91.7 dB, THD -105 dB 14-bit 600 kSPS/300 kSPS 8-ch pseudo-differential SAR ADC, SINAD 85 dB, THD -105 dB	
ZJC2104/5-18 ZJC2104/5-16	18-bit 400 kSPS/200 kSPS 4-ch pseudo-differential SAR ADC, SINAD 94.2 dB, THD -105 dB 16-bit 500 kSPS/250 kSPS 4-ch pseudo-differential SAR ADC, SINAD 91.7 dB, THD -105 dB	
DAC		
ZJC2541-18/16/14 ZJC2543-18/16/14	18/16/14-bit 1 MSPS single channel DAC with unipolar output	Power on reset to 0 V (ZJC2541) or V_{REF}/2 (ZJC2543), 1 nV-S glitch, SOIC-8, MSOP-10/8, DFN-10 packages
ZJC2542-18/16/14 ZJC2544-18/16/14	18/16/14-bit 1 MSPS single channel DAC with bipolar output	Power on reset to 0 V (ZJC2542) or V_{REF}/2 (ZJC2544), 1 nV-S glitch, SOIC-14, TSSOP-16, QFN-16 packages
Amplifier		
ZJA3000-1/2/4 ZJA3001-1/2/4	Single/Dual/Quad 36 V low bias current precision Op Amps	3 MHz, 35 µV max Vos, 0.5 µV/°C max TCVos, 25 pA max Ibias, 1 mA/ch, input to V- (ZJA3000 only), RRO, 4.5 V to 36 V
ZJA3018-2 ZJA3008-2	OVP ±75 V, 36 V, Low Power, High Precision Op Amp 36 V, Low Power, High Precision Op Amp	1.3 MHz, 10 µV max Vos, 0.5 µV/°C max TCVos, 25 pA max Ibias, 0.5 mA/ch, OVP ±75 V (ZJA3018 only), RRO, 4.5 V to 36 V
ZJA3512-2	Dual 36 V 7 MHz precision JFET Op Amps	7 MHz, 35 V/µS, 50 µV max Vos, 1 µV/°C max TCVos, 2 mA/ch, RRO, 9 V to 36 V
ZJA3216/06/02-1/2	Precision 20/10/5 MHz CMOS RRIO Op Amps	20/10/5 MHz, RRIO, 30 µV max Vos, 1 µV/°C max TCVos, 0.6 pA Ib, 2.7 V to 5.5 V
ZJA3600/1	36 V ultra-high precision in-amp	CMRR 105 dB min (G = 1), 25 pA max Ib, 25 µV max Vosi, ±2.4 V to ±18 V, -40 °C to 125 °C
ZJA3611, ZJA3609	36 V precision wider bandwidth precision in-amp (G ≥ 10)	CMRR 120 dB min (G = 10), 25 pA max Ibias, 25 µV max Vosi, 1.2 MHz BW (G = 10)
ZJA3676/7 ZJA3678/9	Low power, G=1 Single/Dual 36 V difference amplifier Low power, G=0.5/2 Single/Dual 36 V difference amplifier	Input protection to ±65 V, CMRR 104 dB min (G = 1), Vos 100 µV max, gain error 15 ppm max, 500 kHz BW (G = 1), 330 µA/channel, 2.7 V to 36 V
ZJA3669	High Common-Mode Voltage Difference Amplifier	±270 V CMV, 2.5 kV ESD, 96 dB min CMRR, 450 kHz BW, 4 V to 36 V, SOIC-8
ZJA3100	15 V precision fully differential amplifier	145 MHz, 447 V/µS, 50 nS to 16-bit, 50 µV max Vos, 4.6 mA Iq, SOIC/MSOP-8, QFN-16
ZJA3236/26/22-2	Low-cost 20/10/5 MHz CMOS RRIO Op Amps	20/10/5 MHz, RRIO, 2 mV max Vos, 6 µV/°C max TCVos, 0.6 pA Ib, 2.7 V to 5.5 V
ZJA3622/8	36 V low-cost precision in-amp	0.5 nA max Ibias, 125 µV max Vosi, 625 kHz BW (G = 10), 3.3 mA Iq, ±2.4 V to ±18 V
Voltage Reference		
ZJR1004	40 V supply precision voltage reference	V_{OUT} = 2.048/2.5/3/3.3/4.096/5/10 V, 5 ppm/°C max drift -40 °C to 125 °C
ZJR1001/2 ZJR1003	5.5 V low power voltage reference (ZJR1001 with noise filter option)	V_{OUT} = 2.048/2.5/3/3.3/4.096/5 V, 5 ppm/°C max drift -40 °C to 125 °C, ±0.05% initial error, 130 µA, ZJR1001/2 in SOT23-6, ZJR1003 in SOIC/MSOP-8
ZJR1302	5.5 V low power compact precision voltage reference	V_{OUT} = 2.048/2.5/3/3.3/4.096 V, 30 ppm/°C max drift -40 °C to 125 °C, 130 µA, SOT23-3
Switches and Multiplexers		
ZJG4438/4439	36 V fault protection 8:1/dual 4:1 multiplexer	Protection to ±50 V power on & off, latch-up immune, Ron 270 Ω, 14.8 pC, t_{ON} 166 nS
ZJG4428/4429	36 V 8:1/dual 4:1 multiplexer	Latch-up immune, Ron 270 Ω, 14.8 pC charge injection, t_{ON} 166 nS
Quad Matching Resistor		
ZJM5400	±75 V precision match resistors	Mismatch < 100 ppm, 10k:10k:10k:10k, 100k:100k:100k:100k, 100k:10k:10k:100k, 1k:1k:1k:1k 1M:1M:1M:1M, 5k:1k:1k:5k, 5k:1.25k:1.25k:5k, 9k:1k:1k:9k, ESD: 3.5 kV