36 V, Rail-to-rail Input/Output, High Precision Op Amp with ZHIJINGTRIM™

Features

- Low Offset Voltage: 5 μV
- Low Offset Voltage Temperature Drift: 0.3 μV/°C
- Low Input Bias Current: 20 pA max
- High Common-mode Rejection Ratio: 128 dB
- High Open-loop Voltage Gain: 140 dB
- Rail-to-rail Input and Output
- Gain Bandwidth Product: 6 MHz, unit gain stable
- High Slew Rate: 19.5 V/μs
- Supply Current: 1.42 mA/amplifier
- Single/Dual Power Supply: ±2.25 V to ±18 V, 4.5 V to 36 V
- Differential Input Voltage Range to Supply Rail

Applications

- Multiplexed Data Acquisition System
- Test and Measurement Equipment
- SAR ADC Reference Buffers
- High-Side and Low-Side Current Sensing
- High Precision Comparator

General Description

The ZJA3092 family is a new generation of 36 V, ZHIJINGTRIM™ operational amplifiers.

These devices offer outstanding dc precision and ac performance, including rail-to-rail input/output, low offset (5 μV), low offset drift (0.3 μV/°C), and 6 MHz GBP.

Unique features such as differential input-voltage range to the supply rail, high output current (±70 mA), and high slew rate (19.5 V/μs) make the ZJA3092 a robust, high-performance operational amplifier for high-voltage industrial applications.

ZJA3092-2 is available in 8-lead narrow SOIC and MSOP packages. They are specified over the -40 °C to +125 °C temperature range.

Model	Channels	Package
ZJA3092-2	2	SOIC-8/MSOP-8

Typical Application

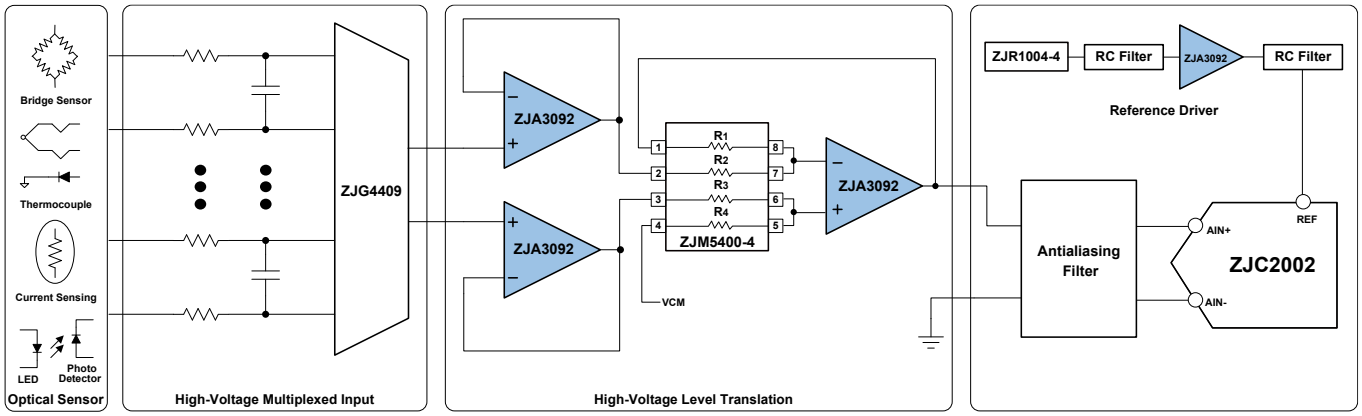

Table of Contents

Version (Release A)[1]

Revision History

Dec. 2025 — Release A

Aug. 2025 — Initial

[1] Information furnished by ZJW Microelectronics is believed to be accurate and reliable. However, no responsibility is assumed by ZJW Microelectronics for its use, nor for any infringements of patents or other rights of third parties that may result from its use. Specifications subject to change without notice. No license is granted by implication or otherwise under any patent or patent rights of ZJW Microelectronics. Trademarks and registered trademarks are the property of their respective owners.

Pin Configurations and Function Descriptions

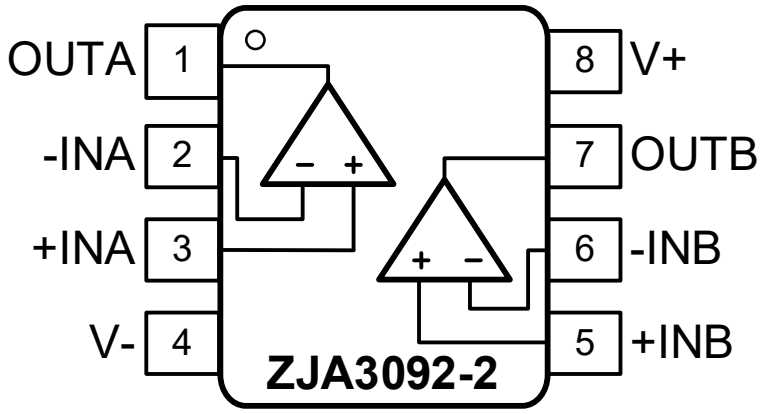

Figure 1. ZJA3092-2 Pin Configuration (8-lead SOIC and MSOP)

Mnemonic	Pin No.	I/O[1]	Description
OUTA	1	AO	Channel A output
-INA	2	AI	Channel A inverting input
+INA	3	AI	Channel A Non-inverting input
V-	4	P	Negative power supply
+INB	5	AI	Channel B Non-inverting input
-INB	6	AI	Channel B inverting input
OUTB	7	AO	Channel B output
V+	8	P	Positive power supply

[1] AI: Analog Input; P: Power; AO: Analog Output.

Absolute Maximum Ratings [1]

Parameter	Rating
Supply Voltage	40 V
Input Voltage	
Common-mode	(V-) – 0.3 V to (V+) + 0.3 V
Differential	(V+) – (V-) + 0.2 V
Output Short-Circuit Duration to GND[2]	Continuous
Operating Temperature Range	-40 °C to 125 °C
Storage Temperature Range	-65 °C to 150 °C
Junction Temperature Range	-65 °C to 150 °C

Thermal Resistance [3]

Package Type	θ_{JA}	θ_{JC}	Unit
SOIC-8	158	43	°C/W
MSOP-8	190	44	°C/W

[1] These ratings apply at 25 °C, unless otherwise noted. Stresses above these ratings may cause permanent damage. Exposure to absolute maximum conditions for extended periods may degrade device reliability. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those specified is not implied.

[2] Short-circuit to ground, one amplifier per package.

[3] θ_{JA} addresses the conditions for soldering devices onto circuit boards to achieve surface mount packaging.

Specifications

The ● denotes the specification which apply over the specified temperature range, otherwise specifications are at V_S = ±18 V, V_{CM} = 0 V, R_L = 10 kΩ connected to 0 V, and T_A = 25 °C.

Parameter	Symbol	Conditions		Min	Typ.	Max	Unit
Input Characteristics							
Offset Voltage	V_{OS}				5	25	μV
		T_A = 0 °C to 85 °C				65	μV
			●			100	μV
		V_{CM} = (V+) – 1.5 V			5	25	μV
		V_{CM} = (V+) – 1.5 V, T_A = 0 °C to 85 °C				65	μV
		V_{CM} = (V+) – 1.5 V	●			100	μV
Offset Voltage Drift	TCV_{OS}		●		0.3	1.2	μV/°C
		V_{CM} = (V+) – 1.5 V	●		0.3	1.2	μV/°C
Input Bias Current	I_B				5	20	pA
		T_A = 0 °C to 85 °C				1	nA
Input Offset Current	I_{OS}				1	4	pA
		T_A = 0 °C to 85 °C				0.1	nA
Input Voltage Rang	IVR		●	-18		18	V
Common-mode Rejection Ratio	CMRR	V_{CM} = -18 V to 15 V		112	128		dB
			●	104			dB
		V_{CM} = 16.5V to 18 V		102	116		dB
			●	92			dB
Open-loop Voltage Gain	A_{VOL}	R_L = 10 kΩ, V_O = ±17.7 V		130	140		dB
			●	118			dB
		R_L = 2 kΩ, V_O = ±17.1 V		130	140		dB
			●	116			dB
Input Resistance/Capacitance	R_{IN}/C_{IN}	Differential Mode			0.4/22		TΩ||pF
		Common Mode			4/7		TΩ||pF
Output Characteristics							
Output Voltage (High)	V_{OH}	R_L = 10 kΩ	●			110	mV
		R_L = 2 kΩ	●			500	mV
Output Voltage (Low)	V_{OL}	R_L = 10 kΩ	●			75	mV
		R_L = 2 kΩ	●			320	mV
Short Circuit Current	I_{SC}				±70		mA
Open-loop Output Impedance	Z_O	f = 1 MHz, I_O = 0 A			70		Ω
Power Supply							
Supply Current (per Amplifier)	I_{SY}	V_O = 0 V			1.42	1.55	mA
			●			1.65	mA
Power Supply Rejection Ratio	PSRR	V_S = ±4 V ~ ±18 V		132	140		dB
			●	124			
Dynamic Performance							
Slew Rate	SR	G = 1, 10-V Step			19.5		V/μs
Gain Bandwidth Product	GBP				6		MHz
-3 dB Bandwidth	BW_{-3dB}	G = 1			12		MHz
Settling Time		To 0.01%	V_S = ±18 V, G = 1, 10 V Step		1.1		μs
		To 0.001%	V_S = ±18 V, G = 1, 10 V Step		1.7		μs
Overload Recovery Time	t_{OR}	V_{IN} × G = V_S			60		ns
Total Harmonic Distortion + Noise	THD+N	G = 1, f = 1 kHz, V_O = 3.5 V_{RMS}			0.000045		%
Crosstalk		f = 100 kHz			120		dB
Noise Performance							
Input Voltage Noise	e_n	f = 0.1 Hz to 10 Hz	(V-) < V_{CM} < (V+) – 3 V		2.6		μV_{P-P}
			(V+) – 1.5 V < V_{CM} < (V+)		7.8		μV_{P-P}
		f = 1 kHz	(V-) < V_{CM} < (V+) – 3 V		12.8		$nV/\sqrt{Hz}$
			(V+) – 1.5 V < V_{CM} < (V+)		28.2		$nV/\sqrt{Hz}$
Input Current Noise Density	i_n	f = 1 kHz			2		$fA/\sqrt{Hz}$
Over Temperature Proctection							
Trigger Temperature	T_{IN}				150		°C
Exit Temperature	T_{OUT}				130		°C
Temperature Range							
Specified Temperature Range				-40		125	°C

Typical Performance Characteristics

Unless otherwise stated, T_A = 25 °C, V_S = ±18 V, V_{CM} = V_S/2, R_{LOAD} = 10 kΩ connected to V_S/2 and C_L = 100 pF.

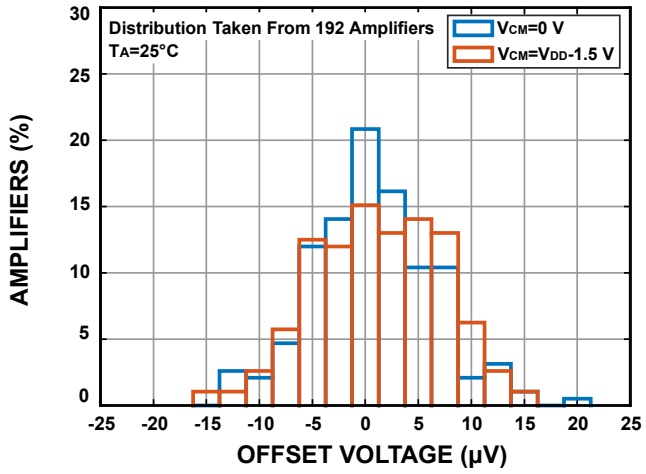

Figure 2. Offset Voltage Drift Distribution @ 25°C

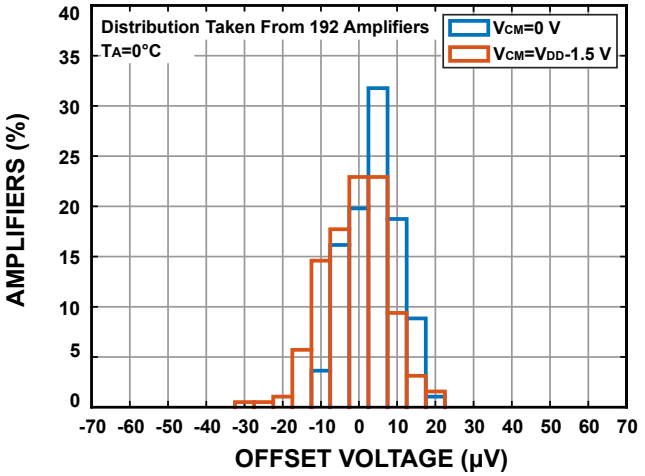

Figure 3. Offset Voltage Drift Distribution @ 0°C

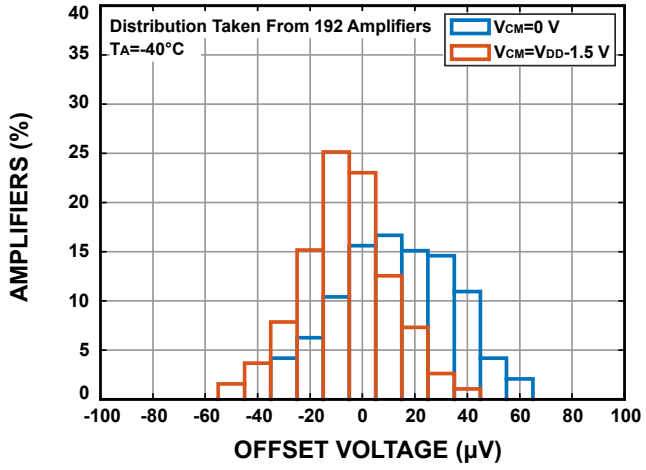

Figure 4. Offset Voltage Drift Distribution @ -40°C

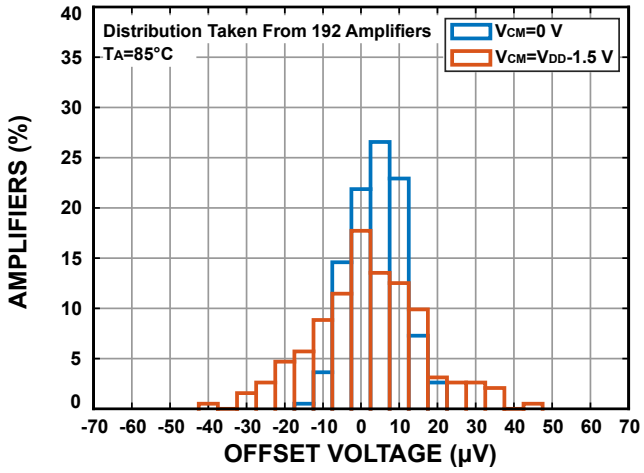

Figure 5. Offset Voltage Drift Distribution @ 85°C

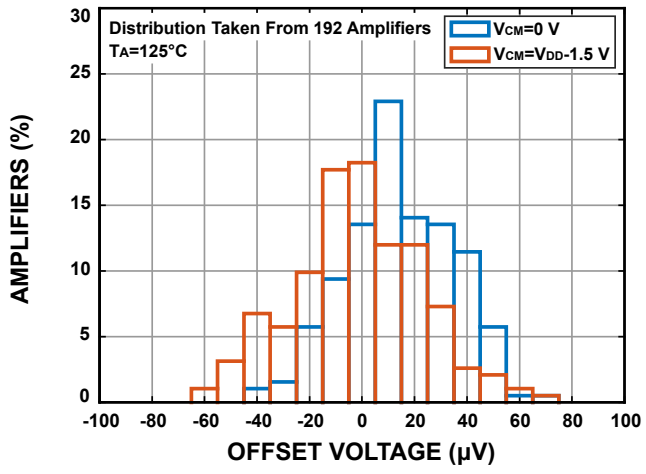

Figure 6. Offset Voltage Drift Distribution @ 125°C

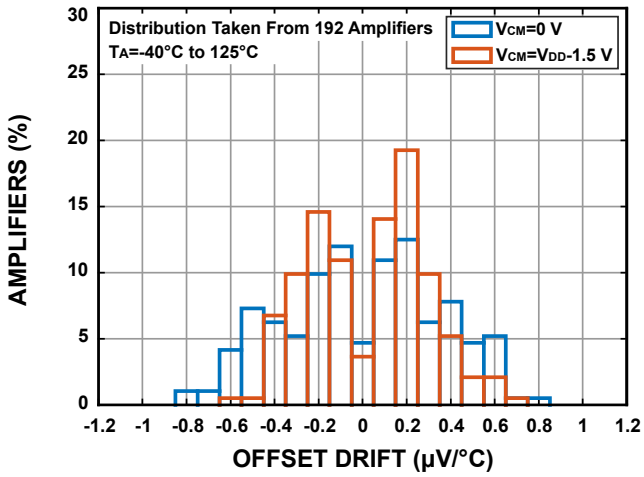

Figure 7. Offset Voltage Drift Distribution @ -40°C to 125°C

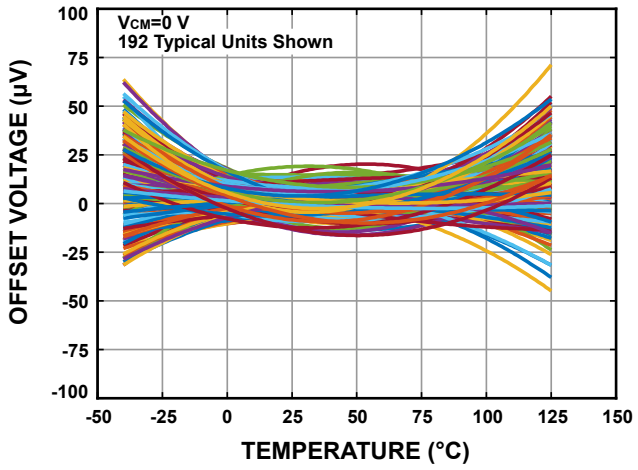

Figure 8. Offset Voltage vs Temperature

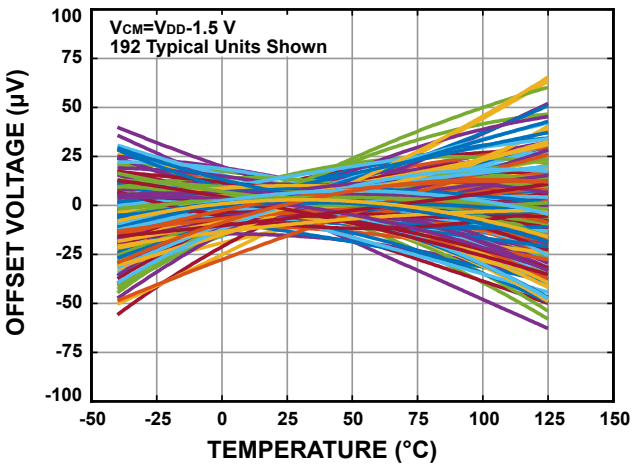

Figure 9. Offset Voltage vs Temperature

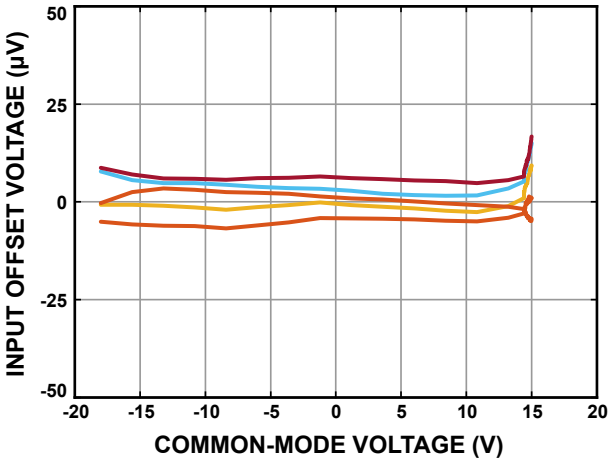

Figure 10. Offset Voltage vs. Common-Mode Voltage

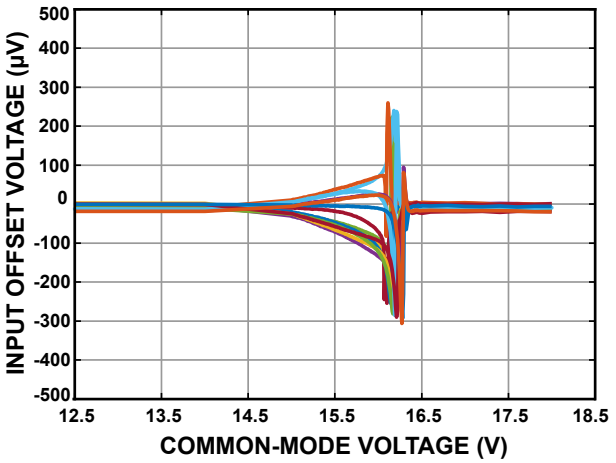

Figure 11. Offset Voltage vs. Common-Mode Voltage

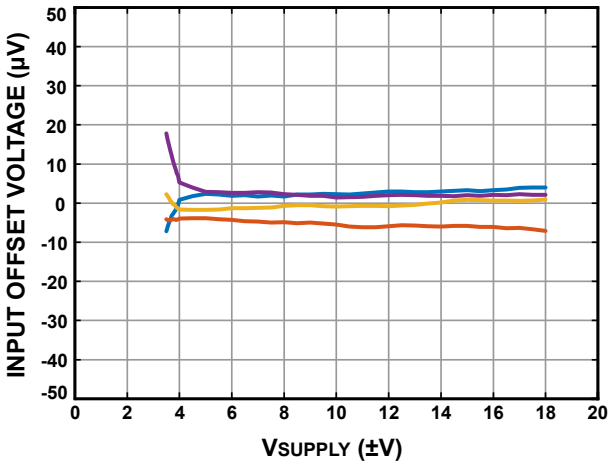

Figure 12. Offset Voltage vs. Power Supply

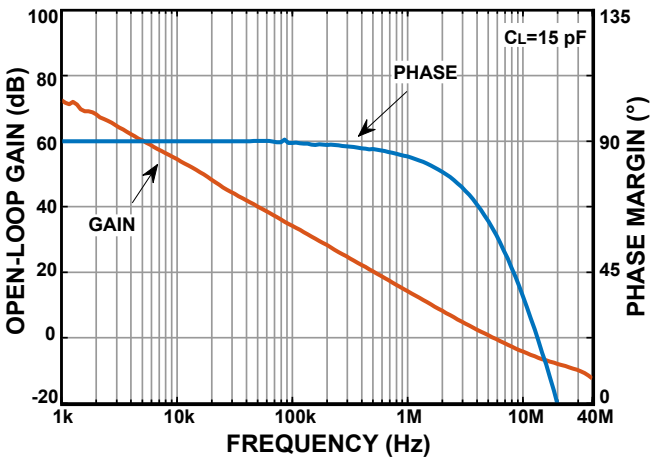

Figure 13. Open-Loop Gain and Phase vs. Frequency

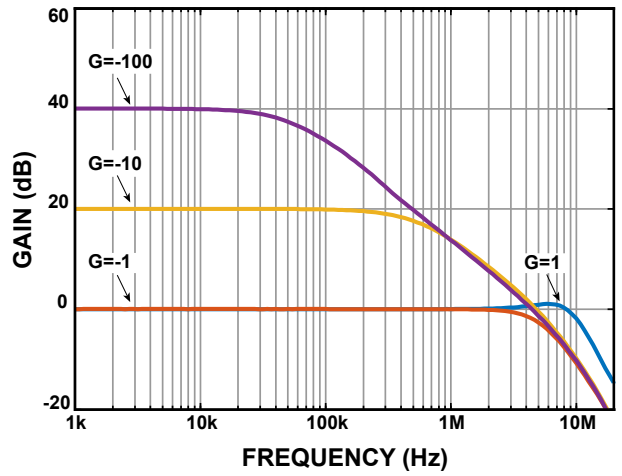

Figure 14. Closed-Loop Gain and Phase vs. Frequency

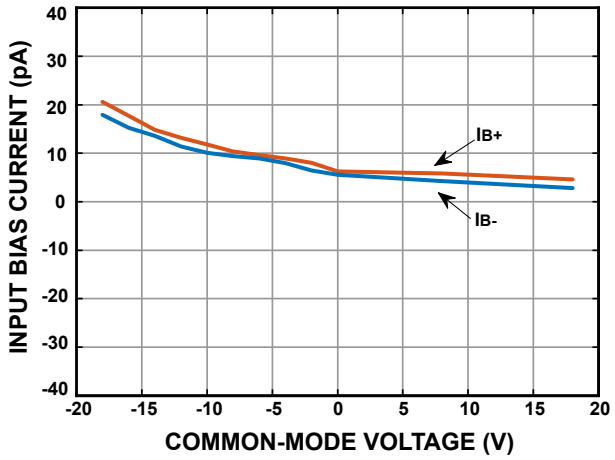

Figure 15. Input Bias Current vs. Common-Mode Voltage

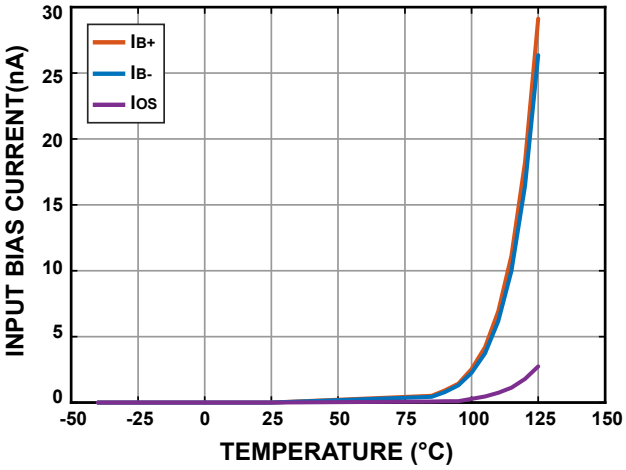

Figure 16. Input Bias Current vs. Temperature

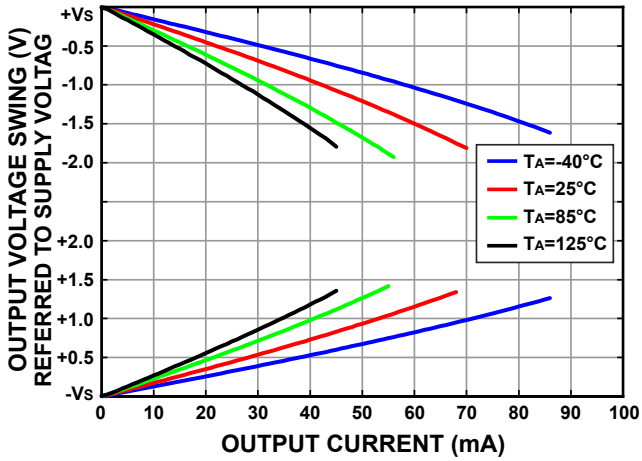

Figure 17. Output Voltage Swing vs. Output Current

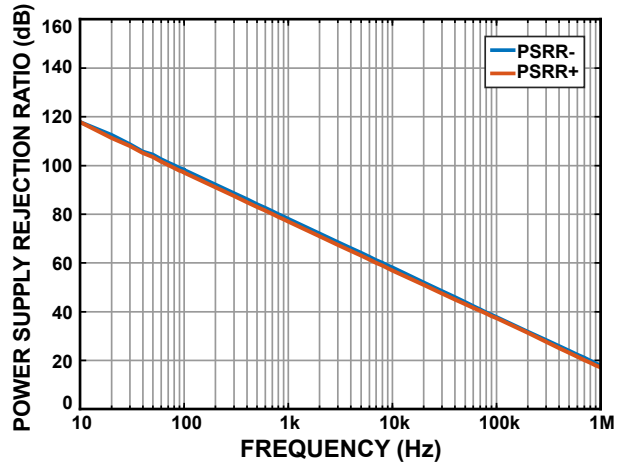

Figure 18. PSRR vs. Frequency

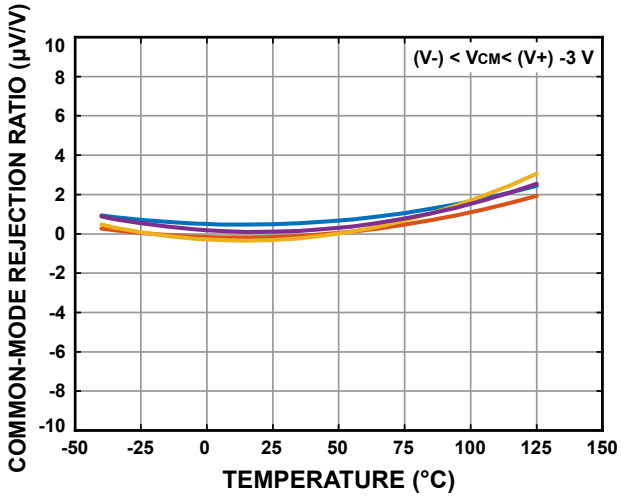

Figure 19. CMRR vs. Temperature

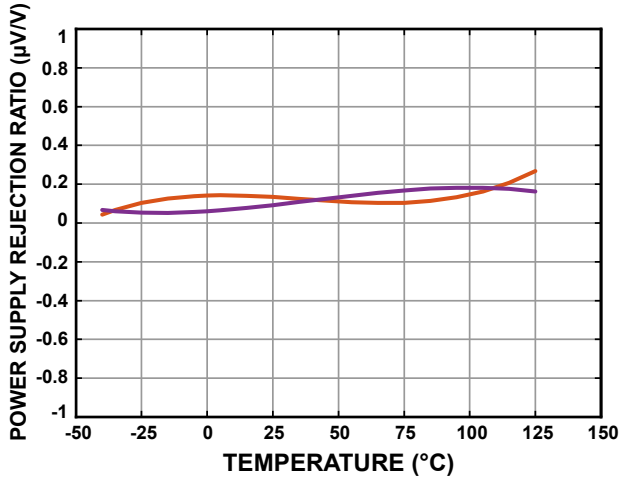

Figure 20. PSRR vs. Temperature

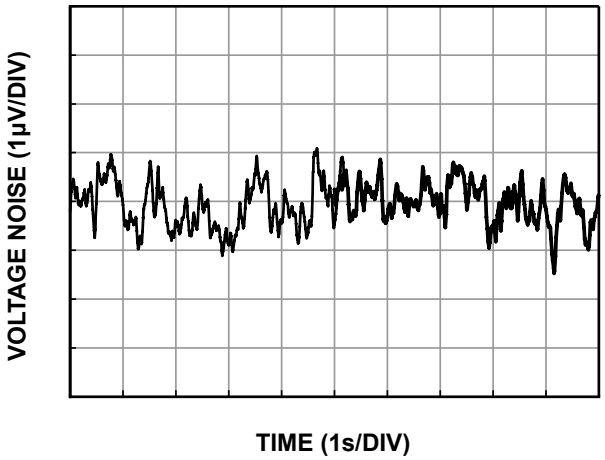

Figure 21. 0.1 Hz to 10 Hz Noise

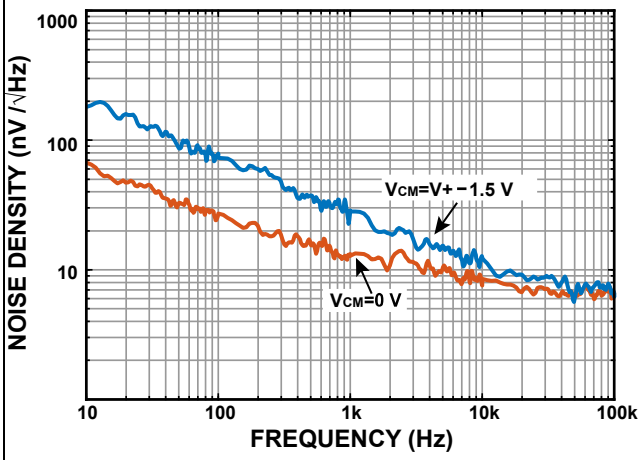

Figure 22. Input Voltage Noise Spectral Density vs. Frequency

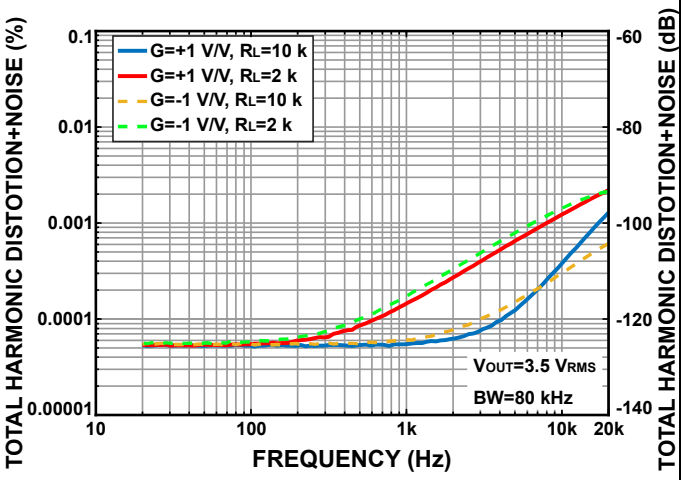

Figure 23. THD+N Ratio vs Frequency

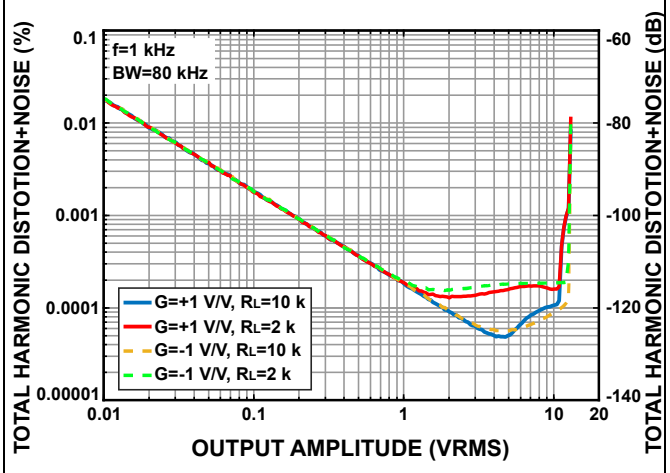

Figure 24. THD+N vs. Output Amplitude

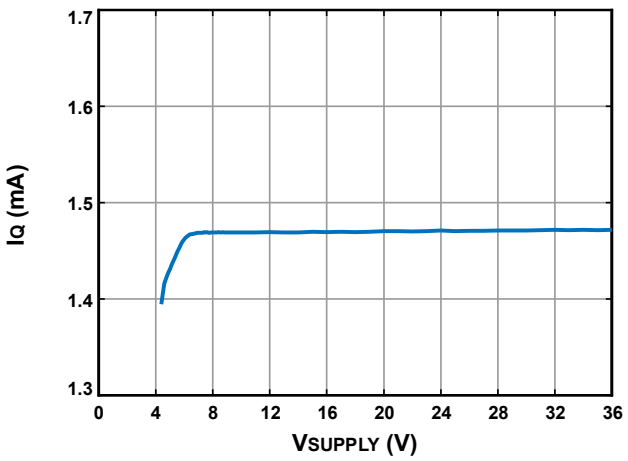

Figure 25. Quiescent Current vs. Supply Voltage

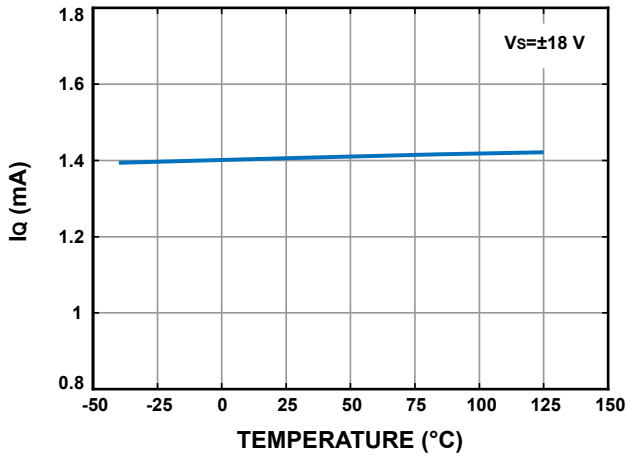

Figure 26. Quiescent Current vs. Temperature

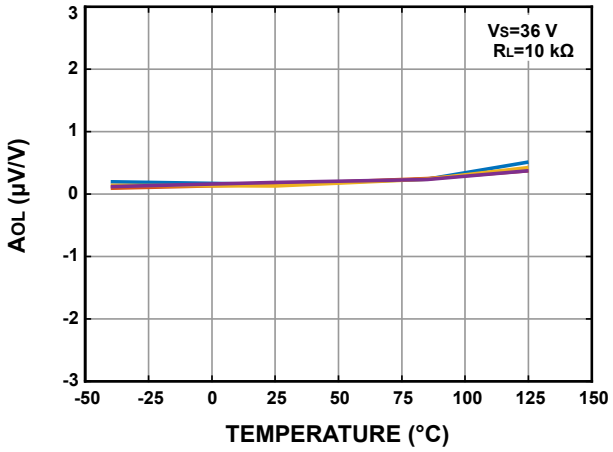

Figure 27. Open-Loop Gain vs. Temperature

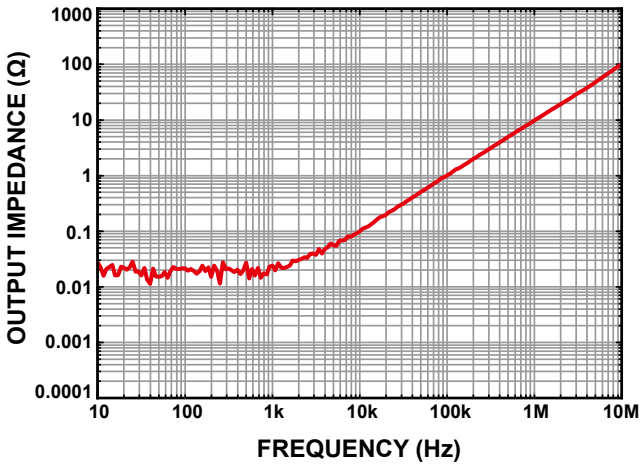

Figure 28. Output Impedance vs. Frequency

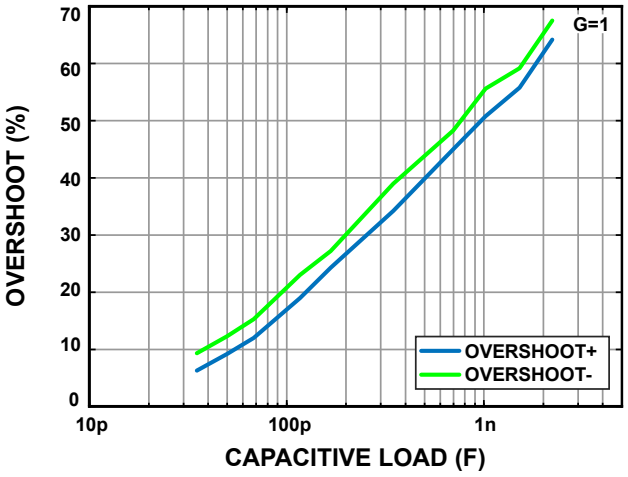

Figure 29. Small-Signal Overshoot vs. Capacitive Load (G=1)

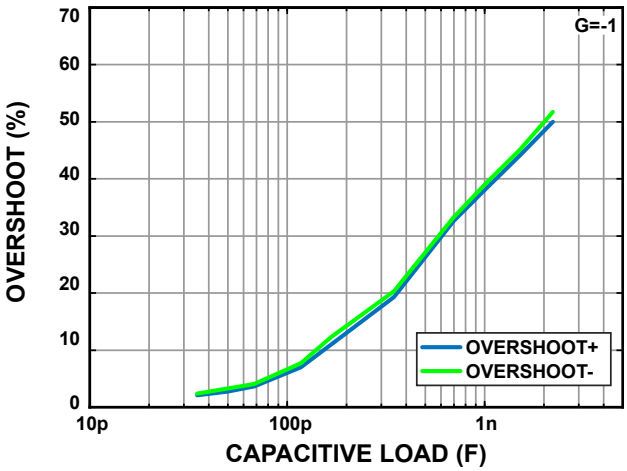

Figure 30. Small-Signal Overshoot vs. Capacitive Load (G=-1)

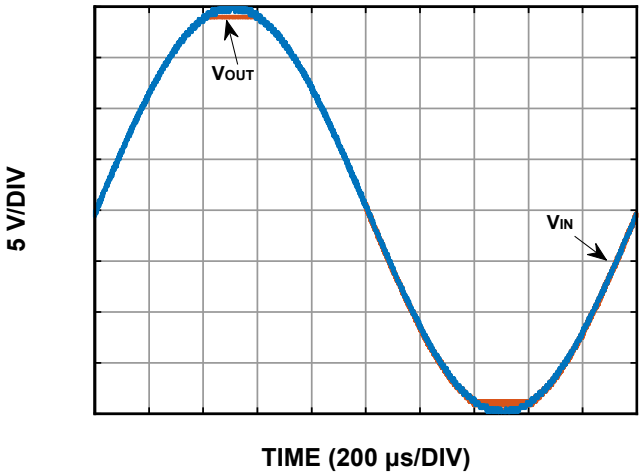

Figure 31. No Phase Reversal

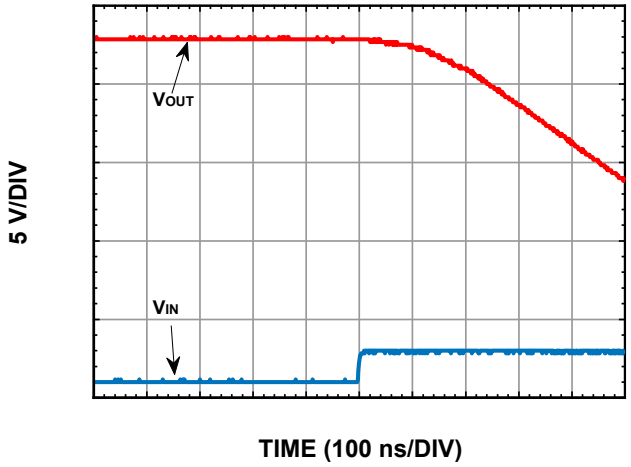

Figure 32. Positive Overload Recovery

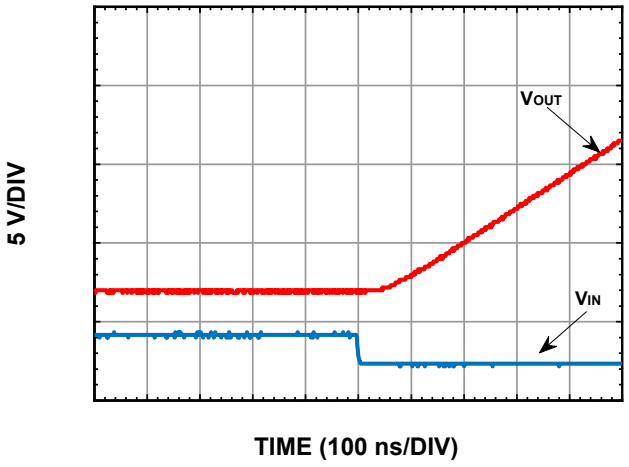

Figure 33. Negative Overload Recovery

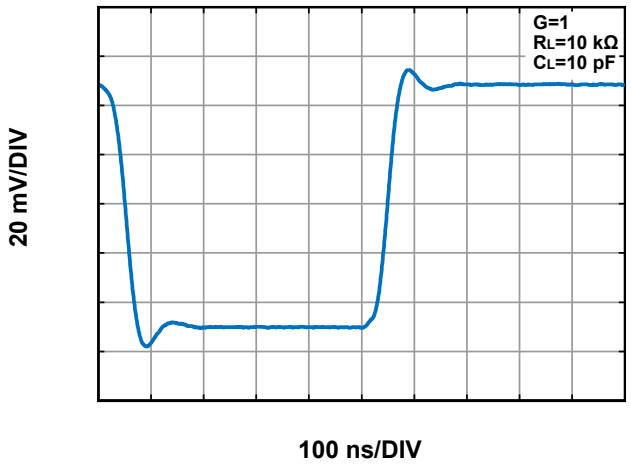

Figure 34. Small Signal Response (G=1)

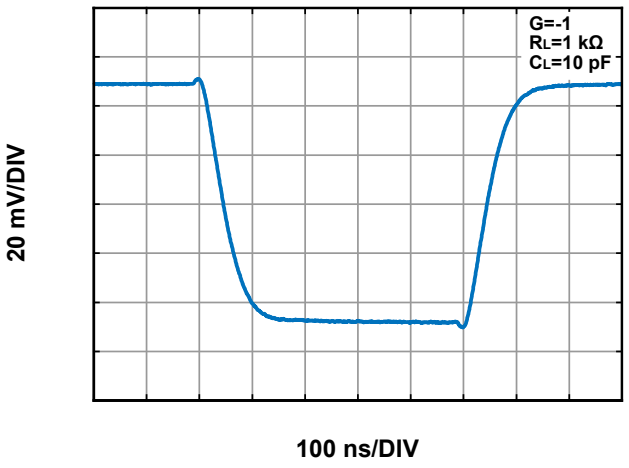

Figure 35. Small Signal Response (G=-1)

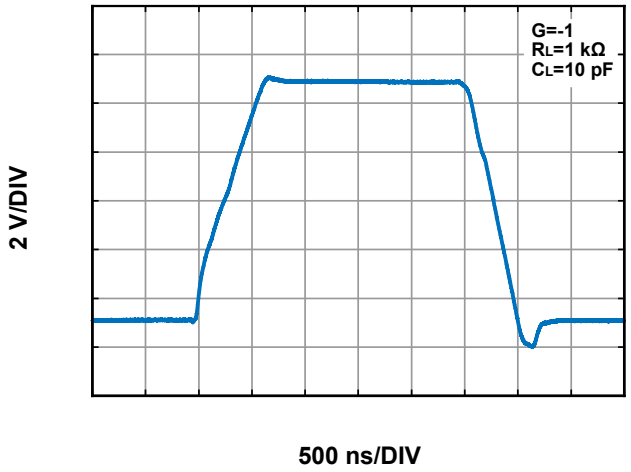

Figure 36. Large Signal Response (G=-1)

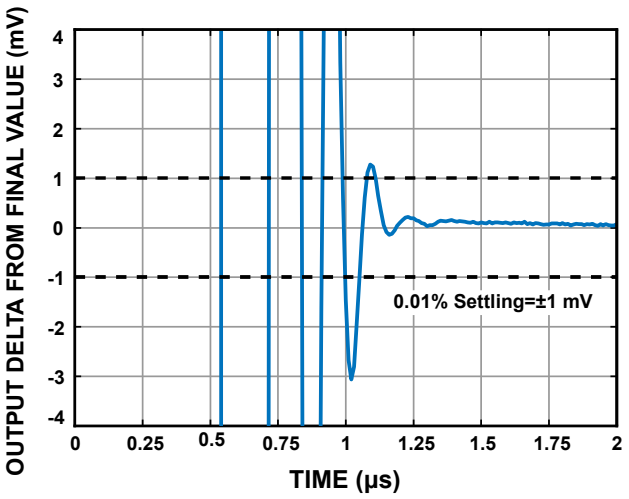

Figure 37. Settling Time (10 V Negative Step)

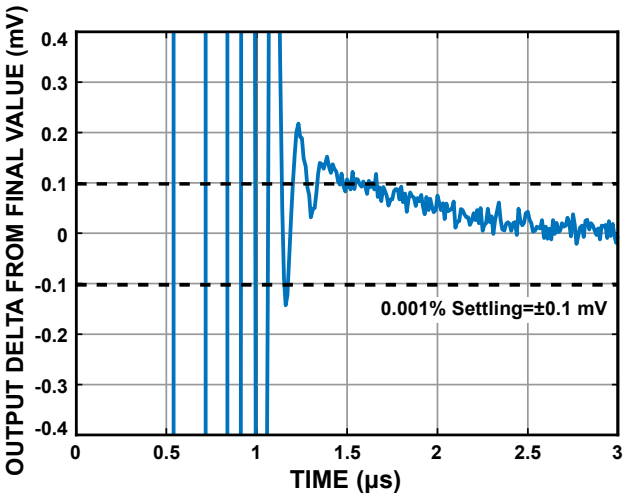

Figure 38. Settling Time (10 V Negative Step)

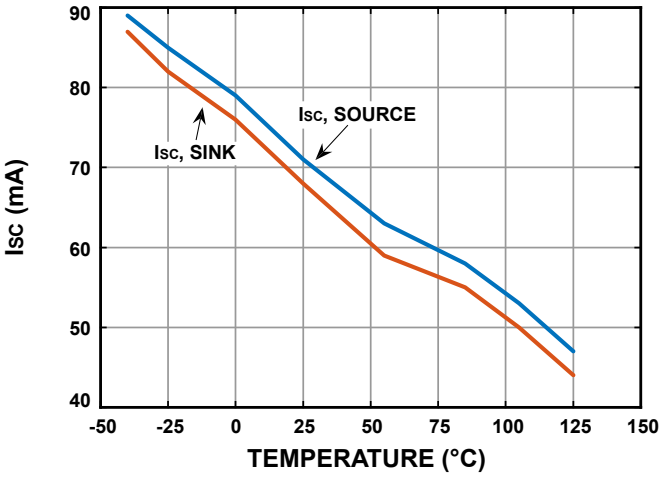

Figure 39. Short-Circuit Current vs. Temperature

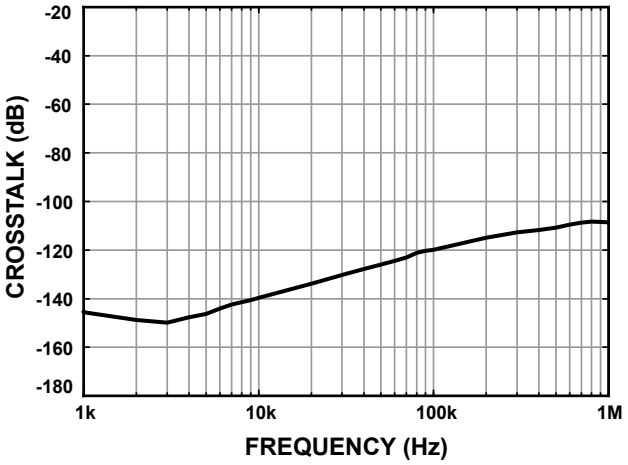

Figure 40. Crosstalk vs Frequency

Outline Information

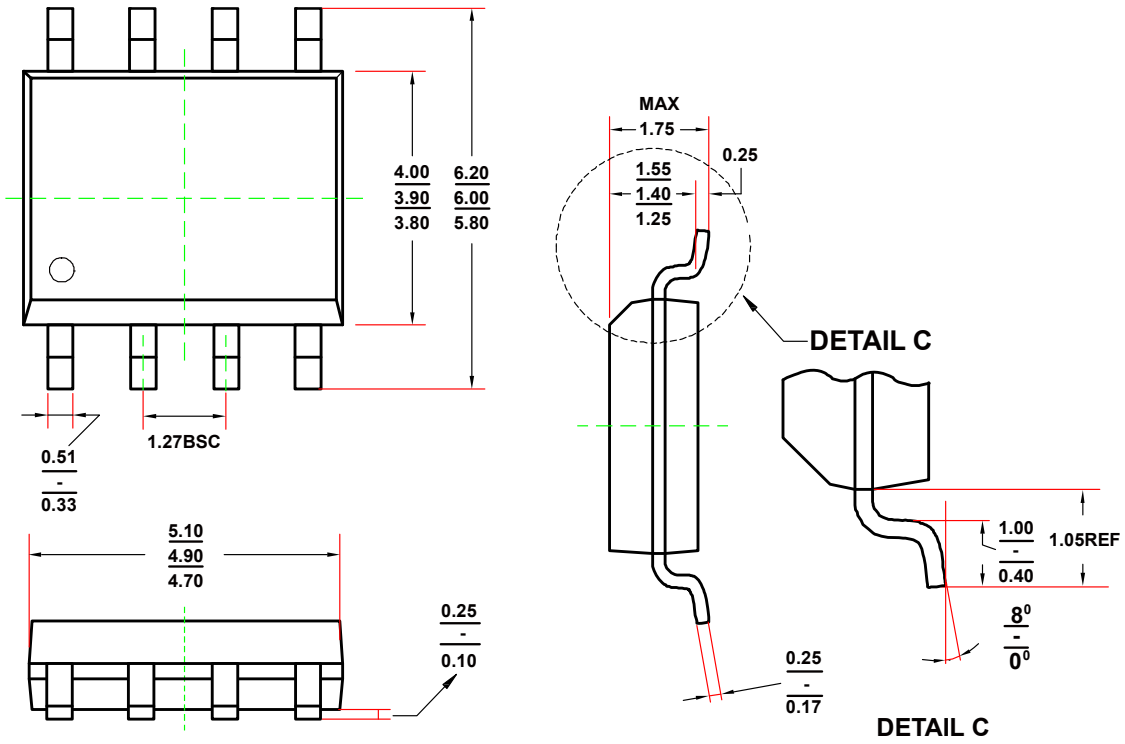

Figure 41. 8-Lead SOIC Package Dimensions shown in millimeters

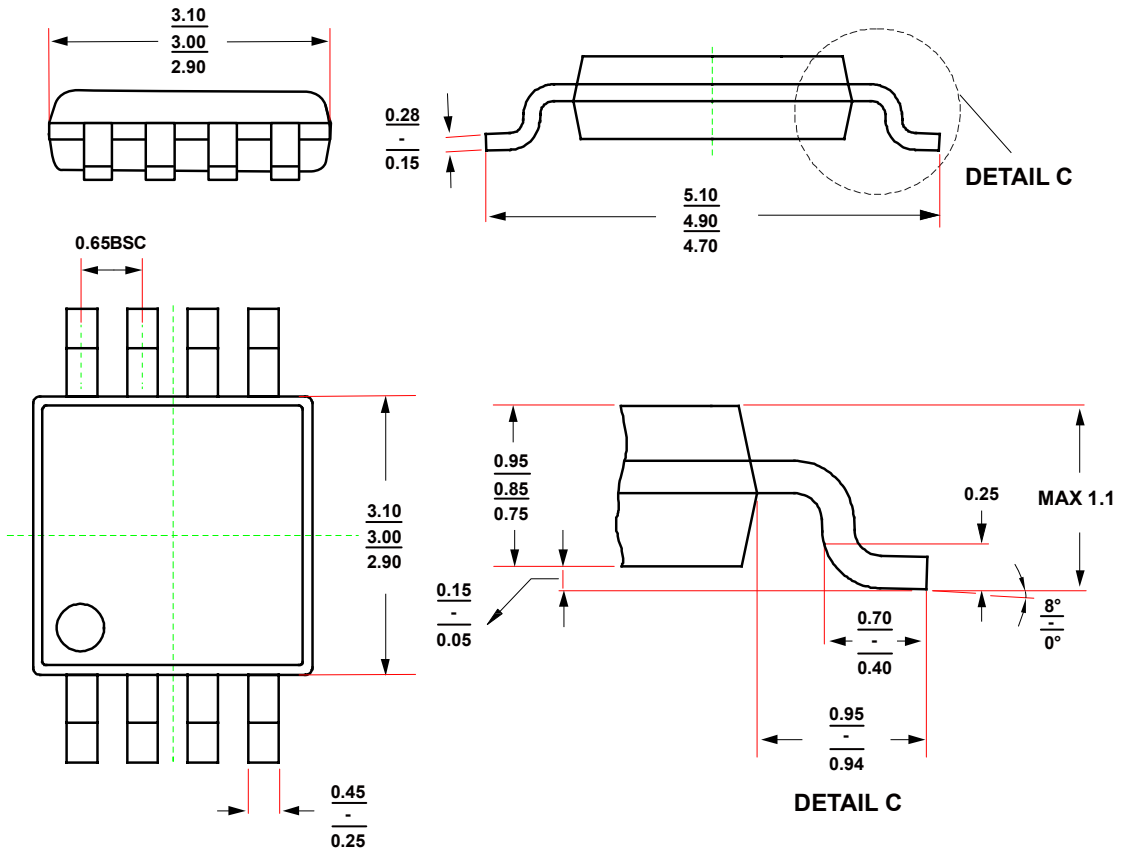

Figure 42. 8-Lead MSOP Package Dimensions shown in millimeters

Ordering Guide

Model	Orderable Device	Channels	Package	Temperature Range (°C)	External Package
ZJA3092-2	ZJA3092-2ASABT	2	SOIC-8	-40 to +125	Tube
	ZJA3092-2ASABR				13” Reel
	ZJA3092-2AUABT		MSOP-8		Tube
	ZJA3092-2AUABR				13” Reel

Product Order Model

ZJXXXX X X X X X Q1

- Q1: Automotive Grade
- External Package: T = Tube; R = Reel
- Temperature Range: A = -40 °C to 125 °C Automotive Grade 1, B = -40 °C to 125 °C; E = -40 °C to 85 °C
- Number of Pins: R = 3; K =5; T = 6, A = 8; B = 10; D = 14; E = 16; P = 20
- Package Type: S = SOIC; U = MSOP, TSSOP, SOT; T = DFN, QFN; X = SC70; W = WLCSP; Z = TSOT23
- Grade: B grade is better than A grade
- Base: R = Voltage reference; A = Amplifier; C = Data Converter; G = Switches and Multiplexers; M = Others

Related Parts

Part Number	Description	Comments
ADC		
ZJC2020	20-bit 350 kSPS SAR ADC	Fully differential input, SINAD 101.4 dB, THD -118 dB
ZJC2000/2010	18-bit 400 kSPS/200 kSPS SAR ADC	Fully differential input, SINAD 99.3 dB, THD -113 dB
ZJC2001/2011	16-bit 500 kSPS/250 kSPS SAR ADC	Fully differential input, SINAD 95.3 dB, THD -113 dB
ZJC2002/2012 ZJC2003/2013	16-bit 500 kSPS/250 kSPS SAR ADC	Pseudo-differential unipolar input, SINAD 91.7 dB, THD -105 dB Pseudo-differential bipolar input, SINAD 91.7 dB, THD -105 dB
ZJC2004/2014 ZJC2005/2015	18-bit 400 kSPS/200 kSPS SAR ADC	Pseudo-differential unipolar input, SINAD 94.2 dB, THD -105 dB Pseudo-differential bipolar input, SINAD 94.2 dB, THD -105 dB
ZJC2007/2017 ZJC2008/2018	14-bit 600 kSPS/300 kSPS SAR ADC	Pseudo-differential unipolar input, SINAD 85 dB, THD -105 dB Pseudo-differential bipolar input, SINAD 85 dB, THD -105 dB
ZJC2100/1-18 ZJC2100/1-16	18-bit 400 kSPS/200 kSPS 4-ch differential SAR ADC, SINAD 99.3 dB, THD -113 dB 16-bit 500 kSPS/250 kSPS 4-ch differential SAR ADC, SINAD 95.3 dB, THD -113 dB	
ZJC2102/3-18 ZJC2102/3-16 ZJC2102/3-14	18-bit 400 kSPS/200 kSPS 8-ch pseudo-differential SAR ADC, SINAD 94.2 dB, THD -105 dB 16-bit 500 kSPS/250 kSPS 8-ch pseudo-differential SAR ADC, SINAD 91.7 dB, THD -105 dB 14-bit 600 kSPS/300 kSPS 8-ch pseudo-differential SAR ADC, SINAD 85 dB, THD -105 dB	
ZJC2104/5-18 ZJC2104/5-16	18-bit 400 kSPS/200 kSPS 4-ch pseudo-differential SAR ADC, SINAD 94.2 dB, THD -105 dB 16-bit 500 kSPS/250 kSPS 4-ch pseudo-differential SAR ADC, SINAD 91.7 dB, THD -105 dB	
DAC		
ZJC2541-18/16/14 ZJC2543-18/16/14	18/16/14-bit 1 MSPS single channel DAC with unipolar output	Power on reset to 0 V (ZJC2541) or V_{REF}/2 (ZJC2543), 1 nV-S glitch, SOIC-8, MSOP-10/8, DFN-10 packages
ZJC2542-18/16/14 ZJC2544-18/16/14	18/16/14-bit 1 MSPS single channel DAC with bipolar output	Power on reset to 0 V (ZJC2542) or V_{REF}/2 (ZJC2544), 1 nV-S glitch, SOIC-14, TSSOP-16, QFN 16 packages
Amplifier		
ZJA3000-1/2/4 ZJA3001-1/2/4	Single/Dual/Quad 36 V low bias current precision Op Amps	3 MHz, 35 µV max Vos, 0.5 µV/°C max TCVos, 25 pA max Ibias, 1 mA/ch, input to V- (ZJA3000 only), RRO, 4.5 V to 36 V
ZJA3018-2 ZJA3008-2	OVP ±75 V, 36 V, Low Power, High Precision Op Amp 36 V, Low Power, High Precision Op Amp	1.3 MHz, 10 µV max Vos, 0.5 µV/°C max TCVos, 25 pA max Ibias, 0.5 mA/ch, OVP ±75 V (ZJA3018 only), RRO, 4.5 V to 36 V
ZJA3512-2	Dual 36 V 7 MHz precision JFET Op Amps	7 MHz, 35 V/µS, 50 µV max Vos, 1 µV/°C max TCVos, 2 mA/ch, RRO, 9 V to 36 V
ZJA3216/06/02-1/2	Precision 20/10/5 MHz CMOS RRIO Op Amps	20/10/5 MHz, RRIO, 30 µV max Vos, 1 µV/°C max TCVos, 0.6 pA Ib, 2.7 V to 5.5 V
ZJA3600/1	36 V ultra-high precision in-amp	CMRR 105 dB min (G = 1), 25 pA max Ib, 25 µV max Vosi, ±2.4 V to ±18 V, -40 °C to 125 °C
ZJA3611, ZJA3609	36 V precision wider bandwidth precision in-amp (G ≥ 10)	CMRR 120 dB min (G = 10), 25 pA max Ibias, 25 µV max Vosi, 1.2 MHz BW (G = 10)
ZJA3676/7 ZJA3678/9	Low power, G = 1 Single/Dual 36 V difference amplifier Low power, G = 0.5/2 Single/Dual 36 V difference amplifier	Input protection to ±65 V, CMRR 104 dB min (G = 1), Vos 100 µV max, gain error 15 ppm max, 500 kHz BW (G = 1), 330 µA/channel, 2.7 V to 36 V
ZJA3669	High Common-Mode Voltage Difference Amplifier	±270 V CMV, 2.5 kV ESD, 96 dB min CMRR, 450 kHz BW, 4 V to 36 V, SOIC-8
ZJA3100	15 V precision fully differential amplifier	145 MHz, 447 V/µS, 50 nS to 16-bit, 50 µV max Vos, 4.6 mA Iq, SOIC/MSOP-8, QFN-16
ZJA3236/26/22-2	Low-cost 20/10/5 MHz CMOS RRIO Op Amps	20/10/5 MHz, RRIO, 2 mV max Vos, 6 µV/°C max TCVos, 0.6 pA Ib, 2.7 V to 5.5 V
ZJA3622/8	36 V low-cost precision in-amp	0.5 nA max Ibias, 125 µV max Vosi, 625 kHz BW (G = 10), 3.3 mA Iq, ±2.4 V to ±18 V
Voltage Reference		
ZJR1004	40 V supply precision voltage reference	V_{OUT} = 2.048/2.5/3/3.3/4.096/5/10 V, 5 ppm/°C max drift -40 °C to 125 °C
ZJR1001/2 ZJR1003	5.5 V low power voltage reference (ZJR1001 with noise filter option)	V_{OUT} = 2.048/2.5/3/3.3/4.096/5 V, 5 ppm/°C max drift -40 °C to 125 °C, ±0.05% initial error, 130 µA, ZJR1001/2 in SOT23-6, ZJR1003 in SOIC/MSOP-8
ZJR1302	5.5 V low power compact precision voltage reference	V_{OUT} = 2.048/2.5/3/3.3/4.096 V, 30 ppm/°C max drift -40 °C to 125 °C, 130 µA, SOT23-3
Switches and Multiplexers		
ZJG4438/4439	36 V fault protection 8:1/dual 4:1 multiplexer	Protection to ±50 V power on & off, latch-up immune, Ron 270 Ω, 14.8 pC, t_{ON} 166 nS
ZJG4428/4429	36 V 8:1/dual 4:1 multiplexer	Latch-up immune, Ron 270 Ω, 14.8 pC charge injection, t_{ON} 166 nS
Quad Matching Resistor		
ZJM5400	±75 V precision match resistors	Mismatch < 100 ppm, 10k:10k:10k:10k, 100k:100k:100k:100k, 100k:10k:10k:100k, 1k:1k:1k:1k 1M:1M:1M:1M, 5k:1k:1k:5k, 5k:1.25k:1.25k:5k, 9k:1k:1k:9k, ESD: 3.5 kV