Precision 20 MHz CMOS Rail-to-Rail Input/Output Operational Amplifiers

Features

- Continuous Time Amplifier, No Chopper or Auto-zero Glitch
- Low Offset Voltage: 50 μV max
- Low Offset Voltage Drift: 0.2 μV/°C
  1 μV/°C max
- Low Input Bias Current: 0.6 pA
  3 pA max
- Low Noise: 6 nV/√Hz @1 kHz
  4 nV/√Hz @10 kHz
  0.1 Hz to 10 Hz 1.4 μV_{P-P}
- High Unit Gain Bandwidth: 20 MHz
- High Slew Rate: 6.8 V/μs
- Fast Settling Time: 0.5 μs to 0.01%
- Supply Current: 1.8 mA per amplifier
- Wide Supply Voltage: 2.7 V to 5.5 V; ±1.35 V to ±2.75 V
- Rail-to-rail Input and Output
- Drive Large Capacitive Load Up to 10 nF
- Large Output Current: ±150 mA
- Wide Temperature Range: -40 °C to +125 °C

Applications

- Multi-parameter Patient Monitor
- Chemistry and Gas Analyzer
- Multi-pole Filters
- Sensor Analog Front End
- ASIC Input or Output Amplifiers
- ADC Input Driver and DAC Output Buffer
- Photodiode Trans-impedance Amplifier

General Description

The ZJA3216 and ZJA3217 are rail-to-rail input and output, single-supply amplifiers featuring very low offset voltage, wide signal bandwidth, and low input voltage and current noise. The parts use a proprietary trimming technique that achieves superior precision without chopping glitches. The ZJA3216 and ZJA3217 are fully specified to operate from 2.7 V to 5 V single supply.

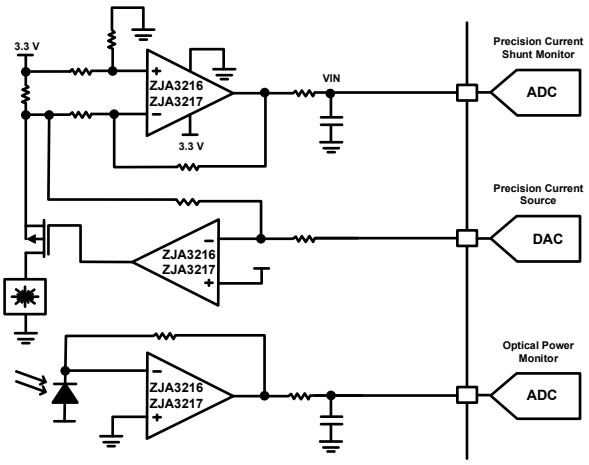
The combination of 20 MHz bandwidth, low offset, low noise, and low input bias current makes these amplifiers useful in a wide variety of applications. Filters, integrators, photodiode amplifiers, and high impedance sensors all benefit from the combination of these features. AC applications benefit from the wide bandwidth and low distortion.

Applications for the parts include portable and low power instrumentation, audio amplification for portable devices and multi-pole filters. The ability to operate rail-to-rail both at the input and at the output enables designers to buffer ADCs, DACs, ASICs, and other wide output swing devices in single-supply systems.

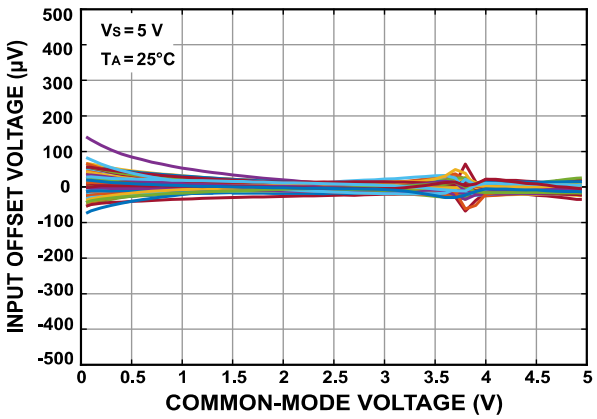
ZJA3216-1 and ZJA3217 are available in 5-lead SOT23 package. ZJA3216-2 is available in 8-lead narrow SOIC, 8-lead MSOP and 8-ball WLCSP packages. ZJA3216-4 is available in 14-lead SOIC and 14-lead TSSOP packages. All of them are specified over the -40 °C to +125 °C extended industrial temperature range.

Model	Channels	Package
ZJA3217	1	SOT23-5
ZJA3216	1	SOT23-5
	2	SOIC/MSOP/WLCSP-8
	4	SOIC/TSSOP-14

Typical Application



Typical Characteristics



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Version (Release D)[1]

Revision History

Nov. 2025 — Release D

Update Unit gain bandwidth changed from 24 MHz to 20 MHz

Update Outline Information and Product Order Model

Aug. 2025 — Release C

Added 8-ball WLCSP package

Jan. 2025 — Release B

Change ZJA3217 Pin Configuration

Nov. 2024

Added ZJA3217

Oct. 2024 — Release A

Jul. 2024 — Initial

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Pin Configurations and Function

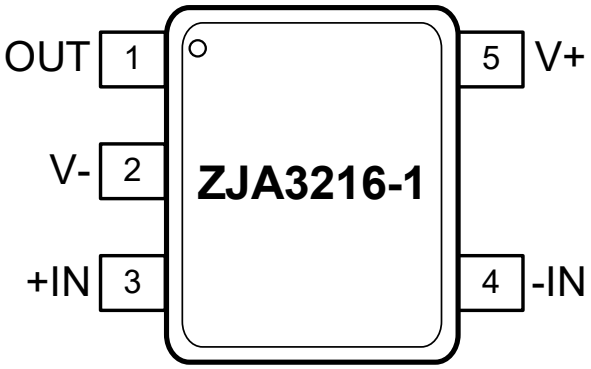

Figure 1. ZJA3216-1 Pin Configuration (5-lead SOT23)

Mnemonic	Pin No.	I/O[1]	Description
OUT	1	AO	Amplifier output
V-	2	P	Negative power supply
+IN	3	AI	Amplifier non-inverting input
-IN	4	AI	Amplifier inverting input
V+	5	P	Positive power supply

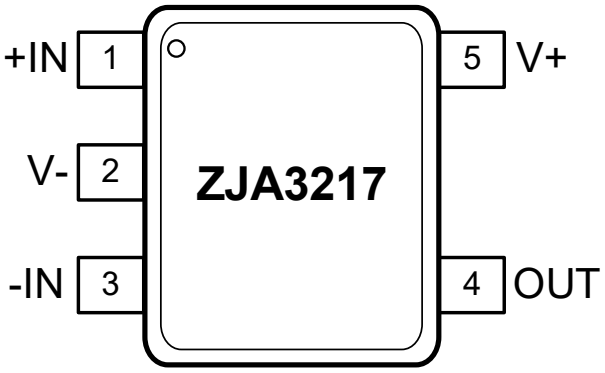

Figure 2. ZJA3217 Pin Configuration (5-lead SOT23)

Mnemonic	Pin No.	I/O[1]	Description
+IN	1	AI	Amplifier non-inverting input
V-	2	P	Negative power supply
-IN	3	AI	Amplifier inverting input
OUT	4	AO	Amplifier output
V+	5	P	Positive power supply

[1] AI: Analog Input; P: Power; AO: Analog Output.

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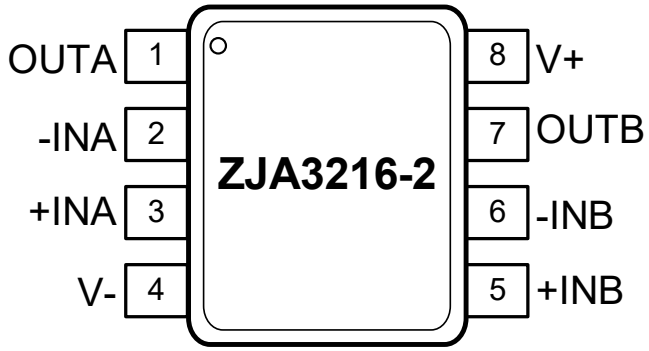

Figure 3. ZJA3216-2 Pin Configuration (8-lead SOIC and MSOP)

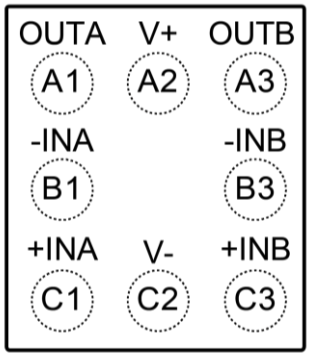

Figure 4. ZJA3216-2 Pin Configuration (8-ball WLCSP)

Mnemonic	SOIC/MSOP-8 Pin No.	WLCSP-8 Ball No.	I/O[1]	Description
OUTA	1	A1	AO	Channel A output
-INA	2	B1	AI	Channel A inverting input
+INA	3	C1	AI	Channel A Non-inverting input
V-	4	C2	P	Negative power supply
+INB	5	C3	AI	Channel B Non-inverting input
-INB	6	B3	AI	Channel B inverting input
OUTB	7	A3	AO	Channel B output
V+	8	A2	P	Positive power supply

[1] AI: Analog Input; P: Power; AO: Analog Output.

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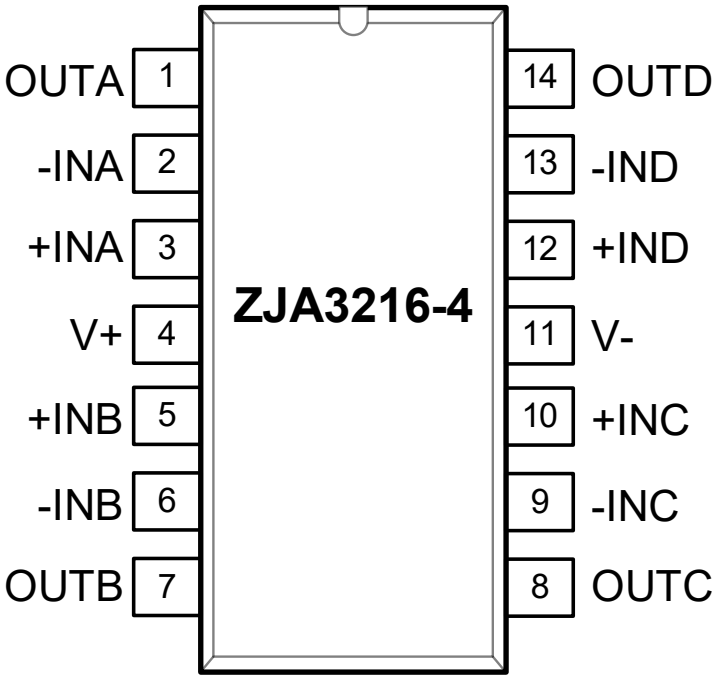

Figure 5. ZJA3216-4 Pin Configuration (14-lead SOIC and TSSOP)

Mnemonic	Pin No.	I/O[1]	Description
OUTA	1	AO	Channel A output
-INA	2	AI	Channel A inverting input
+INA	3	AI	Channel A non-inverting input
V+	4	P-	Positive power supply
+INB	5	AI	Channel B non-inverting input
-INB	6	AI	Channel B inverting input
OUTB	7	AO	Channel B output
OUTC	8	AO	Channel C output
-INC	9	AI	Channel C inverting input
+INC	10	AI	Channel C non-inverting input
V-	11	P	Negative power supply
+IND	12	AI	Channel D non-inverting input
-IND	13	AI	Channel D inverting input
OUTD	14	AO	Channel D output

[1] AI: Analog Input; P: Power; AO: Analog Output.

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Absolute Maximum Ratings [1]

Parameter	Rating
Supply Voltage	6 V
Input Voltage	V- to V+
Output Short-Circuit Duration to GND	Indefinite
Operating Temperature Range	-40 °C to 125 °C
Storage Temperature Range	-65 °C to 150 °C
Junction Temperature Range	-65 °C to 150 °C
Lead Temperature, Soldering (10 sec)	300 °C
ESD Rating (ESD) [2]	
Human Body Model (HBM) [3]	6 kV
Charge Device Model (CDM) [4]	2 kV

Thermal Resistance [5]

Package Type	θ_{JA}	θ_{JC}	Unit
5-lead SOT23	230	76	°C/W
8-lead SOIC	158	43	°C/W
8-lead MSOP	190	44	°C/W
8-ball WLCSP	115		°C/W
14-lead SOIC	120	36	°C/W
14-lead TSSOP	240	43	°C/W

[1] These ratings apply at 25 °C, unless otherwise noted.
Stresses above these ratings may cause permanent damage. Exposure to absolute maximum conditions for extended periods may degrade device reliability. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those specified is not implied.

[2] Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

[3] ANSI/ESDA/JEDEC JS-001 Compliant

[4] ANSI/ESDA/JEDEC JS-002 Complaint

[5] θ_{JA} addresses the conditions for soldering devices onto circuit boards to achieve surface mount packaging.

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Specifications

The ● denotes the specification which apply over the full operating temperature range, otherwise specifications are at V_S = 5 V, V_{CM} = V_S / 2, T_A = 25 °C, unless otherwise noted.

Parameter	Symbol	Conditions		Min	Typ.	Max	Unit
INPUT CHARACTERISTICS							
Offset Voltage	V_{OS}	V_{CM} = 2.5 V and 4.5 V	●		10 70	50 150	μV μV
		V_{CM} = 2.5 V and 4.5 V, WLCSP-8			35		μV
		V_{CM} = 0 V to 5 V	●			500	μV
Offset Voltage Drift	$\Delta V_{OS}/\Delta T$	-40 °C < T_A < +125 °C	●		0.2	1	μV/°C
Input Bias Current	I_B		●		0.6	3 1000	pA pA
		-40 °C < T_A < +85 °C				80	pA
Input Offset Current	I_{OS}		●			5 400	pA pA
		-40 °C < T_A < +85 °C				20	pA
Input Capacitance	C_{DIFF}	Differential			3.2		pF
	C_{CM}	Common-Mode			7.4		pF
Input Voltage Range	IVR			0		5	V
Common-Mode Rejection Ratio	CMRR	V_{CM} = 0 V to 4.5 V		80	105		dB
Large Signal Voltage Gain	A_{VO}	R_L = 2 kΩ, V_O = 0.5 V to 4.5 V		110	140		dB
OUTPUT CHARACTERISTICS							
Output Voltage High	V_{OH}	I_L = 1 mA	●	4.98 4.97	4.988		V V
		I_L = 10 mA	●	4.85 4.80	4.895		V V
Output Voltage Low	V_{OL}	I_L = 1 mA	●		12	20 30	mV mV
		I_L = 10 mA	●		105	150 200	mV mV
Output Current	I_{OUT}				±150		mA
Closed-Loop Output Impedance	Z_{OUT}	f = 1 MHz, A_V = 1			5.6		Ω
POWER SUPPLY							
Supply Current Per Amplifier	I_S	I_{OUT} = 0 mA	●		1.8	2 2.1	mA mA
Power Supply Rejection Ratio	PSRR	V_S = 2.7 V to 5.5 V		80	103		dB
DYNAMIC PERFORMANCE							
Slew Rate	SR	R_L = 2 kΩ			6.8		V/μs
Unit Gain Bandwidth	UGB				20		MHz
Settling Time		To 0.01%			0.5		μs
THD + Noise	THD + N				0.0004		%
Phase Margin	Φ_M				49		Degree
Channel Separation	C_S	f = 10 kHz			-115		dB
		f = 100 kHz			-110		dB
NOISE PERFORMANCE							
Voltage Noise Density	e_n	f = 1 kHz			6		$nV/\sqrt{Hz}$
		f = 10 kHz			4.2		$nV/\sqrt{Hz}$
Peak-to-Peak Voltage Noise	e_{nP-P}	0.1 Hz to 10 Hz			1.4		μV_{P-P}
Current Noise Density	i_n	f = 1 kHz			0.4		$fA/\sqrt{Hz}$

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The ● denotes the specification which apply over the full operating temperature range, otherwise specifications are at V_S = 2.7 V, V_{CM} = V_S / 2, T_A = 25 °C, unless otherwise noted.

Parameter	Symbol	Conditions		Min	Typ.	Max	Unit
INPUT CHARACTERISTICS							
Offset Voltage	V_{OS}	Vs = 3.5 V, V_{CM} = 1.75 V and 3.0 V			40	160	μV
		Vs = 3.5 V, V_{CM} = 1.75 V and 3.0 V, WLCSP-8			35		μV
		Vs = 2.7 V, V_{CM} = 0 V to 2.7 V	●			500	μV
Offset Voltage Drift	$\Delta V_{OS}/\Delta T$	-40 °C < T_A < +125 °C	●		0.2	1	μV/°C
Input Bias Current	I_B		●		0.6	3 1000	pA pA
		-40 °C <T_A < +85 °C				80	pA
Input Offset Current	I_{OS}		●			5 400	pA pA
		-40 °C < T_A < +85 °C				20	pA
Input Capacitance	C_{DIFF}	Differential			3.2		pF
	C_{CM}	Common-Mode			7.4		pF
Input Voltage Range	IVR			0		2.7	V
Common-Mode Rejection Ratio	CMRR	V_{CM} = 0 V to 2.2 V		70	95		dB
Large Signal Voltage Gain	A_{VO}	R_L = 2 kΩ, V_O = 0.5 V to 2.2 V		100	135		dB
OUTPUT CHARACTERISTICS							
Output Voltage High	V_{OH}	I_L = 1 mA	●	2.65 2.65	2.683		V V
Output Voltage Low	V_{OL}	I_L = 1 mA	●		17	50 50	mV mV
Output Current	I_{OUT}				±50		mA
Closed-Loop Output Impedance	Z_{OUT}	f = 1 MHz, A_V = 1			5.6		Ω
POWER SUPPLY							
Supply Current Per Amplifier	I_S	I_{OUT} = 0 mA	●		1.8	2 2.1	mA mA
Power Supply Rejection Ratio	PSRR	V_S = 2.7 V to 5.5 V		80	103		dB
DYNAMIC PERFORMANCE							
Slew Rate	SR	R_L = 2 kΩ			6.8		V/μs
Unit Gain Bandwidth	UGB				20		MHz
Settling Time		To 0.01%			0.5		μs
THD + Noise	THD + N				0.0004		%
Phase Margin	Φ_M				43		Degree
Channel Separation	C_S	f = 10 kHz			-115		dB
		f = 100 kHz			-110		dB
NOISE PERFORMANCE							
Voltage Noise Density	e_n	f = 1 kHz			6		$nV/\sqrt{Hz}$
		f = 10 kHz			4.2		$nV/\sqrt{Hz}$
Current Noise Density	i_n	f = 1 kHz			0.4		$fA/\sqrt{Hz}$
Peak-to-Peak Voltage Noise	e_{nP-P}	0.1 Hz to 10 Hz			1.4		μV_{P-P}

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Typical Performance Characteristics

Unless otherwise stated, T_A = 25 °C, V_S = 5 V, R_L = 2 kΩ.

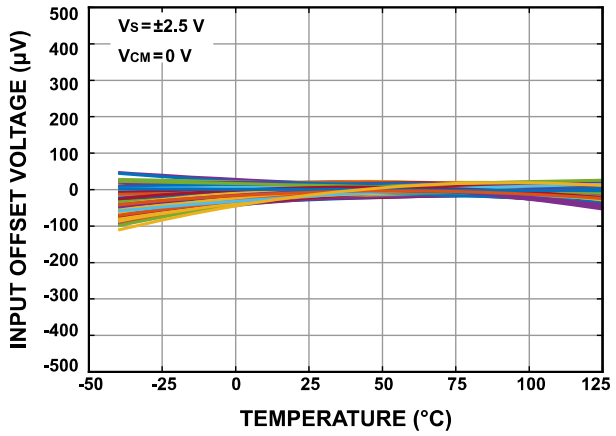

Figure 6. Input Offset Voltage vs. Temperature

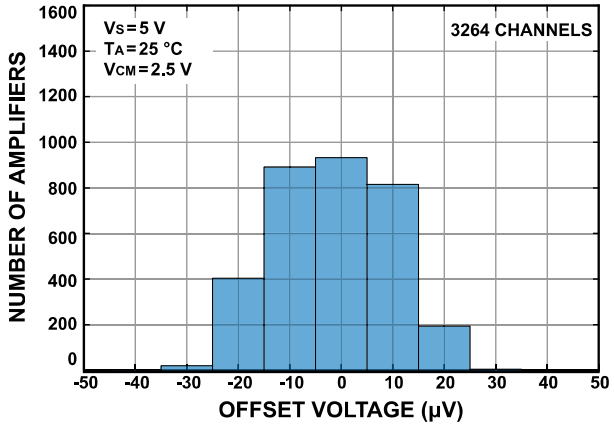

Figure 7. Input Offset Voltage Distribution

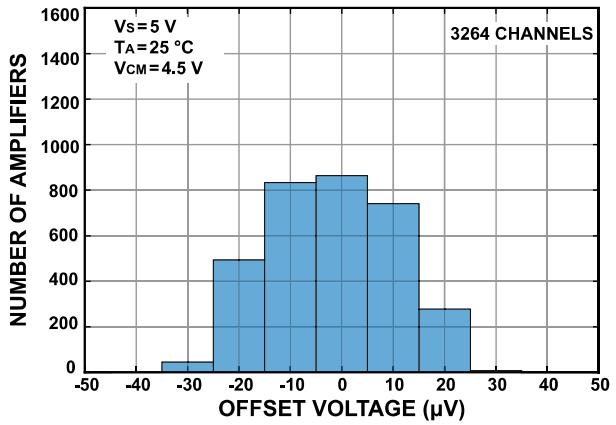

Figure 8. Input Offset Voltage Distribution

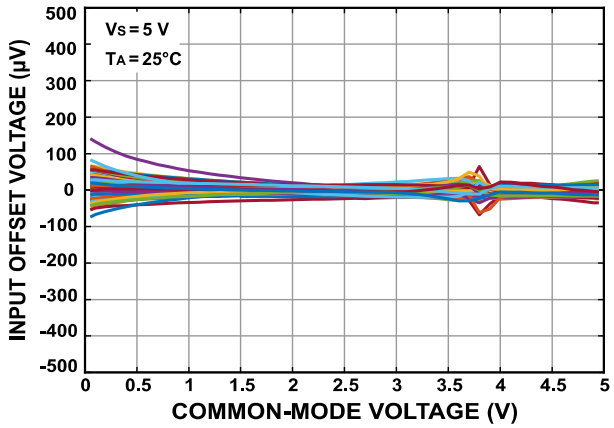

Figure 9. Input Offset vs. Common Mode Voltage

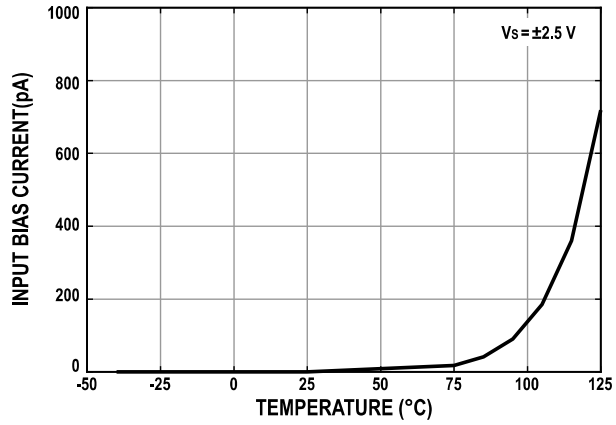

Figure 10. Input Bias Current vs. Temperature

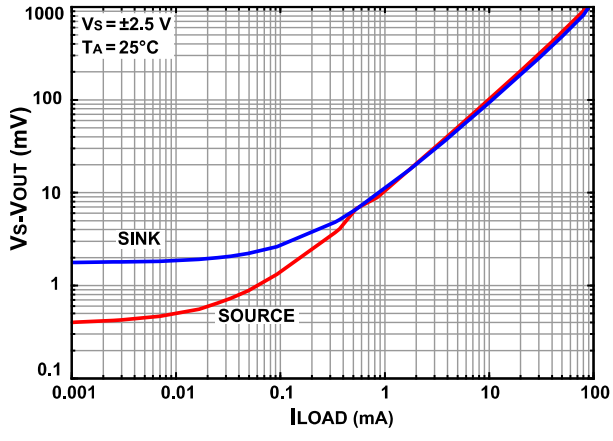

Figure 11. Output Voltage to Supply Rail vs. Load Current

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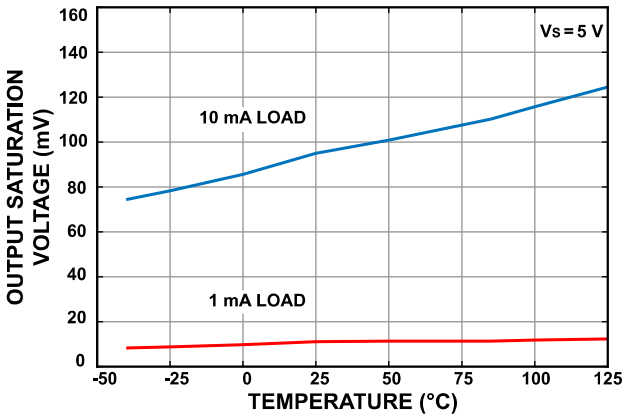

Figure 12. Output Saturation Voltage vs. Temperature

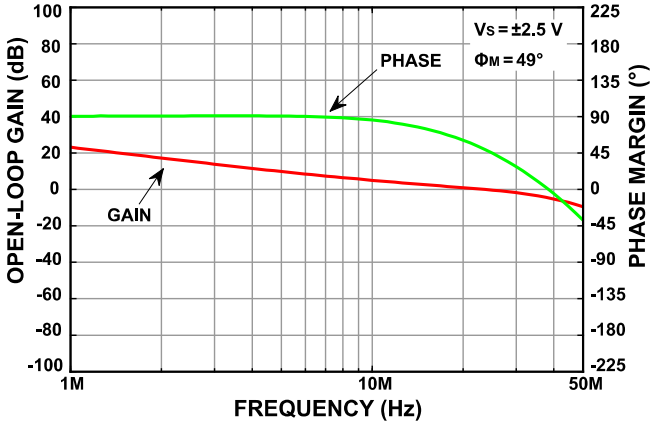

Figure 13. Open-Loop Gain and Phase vs. Frequency

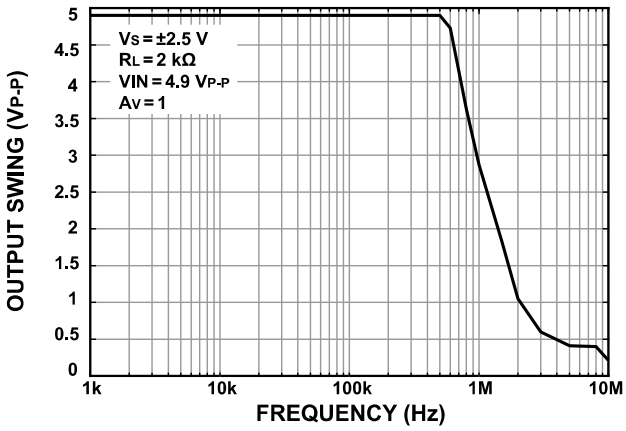

Figure 14. Close-Loop Output Swing vs. Frequency

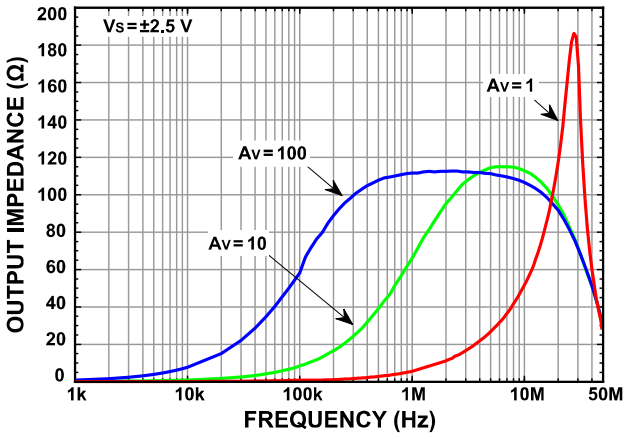

Figure 15. Output Impedance vs. Frequency

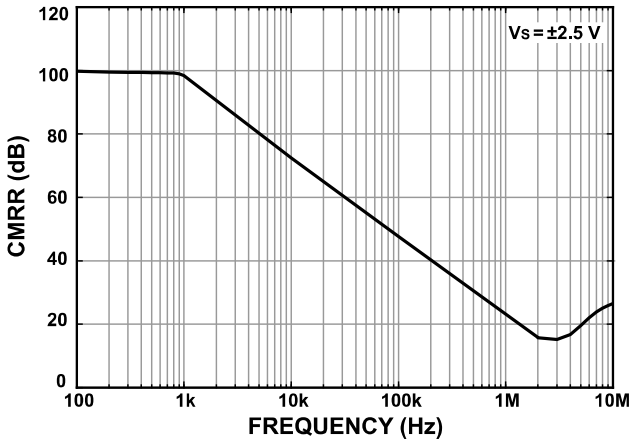

Figure 16. CMRR vs. Frequency

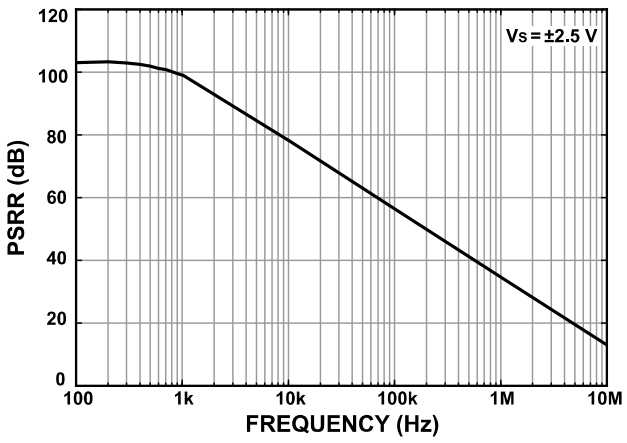

Figure 17. PSRR vs. Frequency

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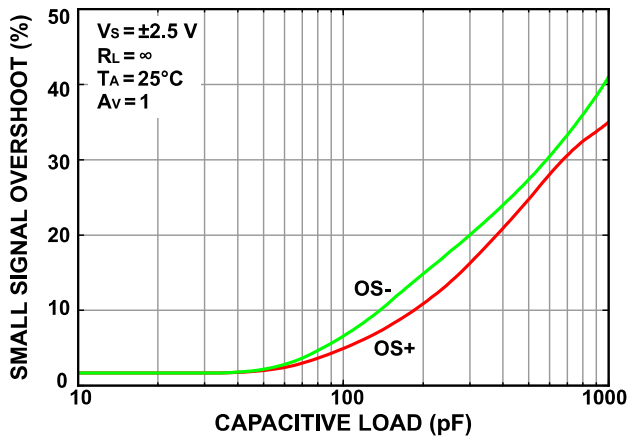

Figure 18. Small-Signal Overshoot vs. Load Capacitance

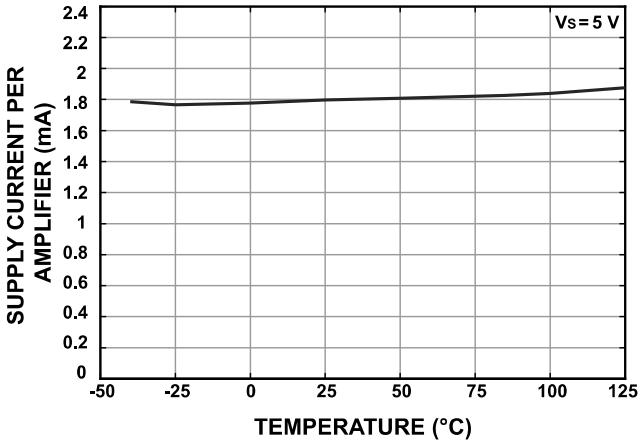

Figure 19. Supply Current vs. Temperature

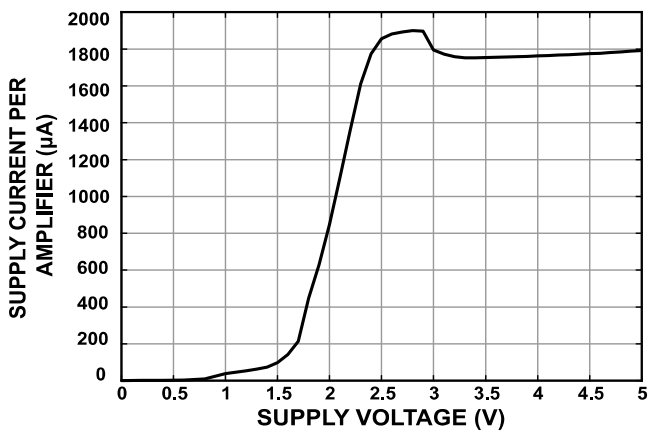

Figure 20. Supply Current per Amplifier vs. Supply Voltage

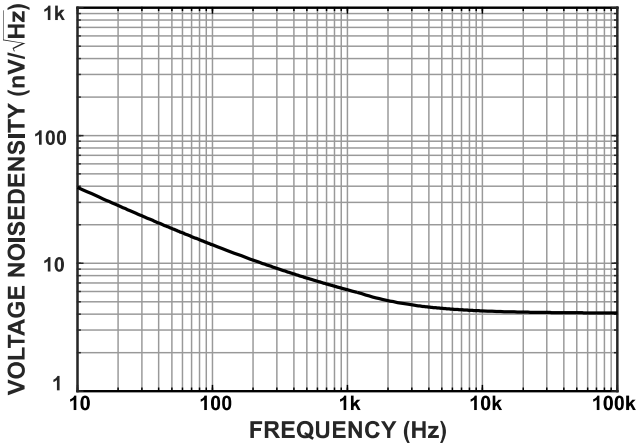

Figure 21. Voltage Noise Density vs. Frequency

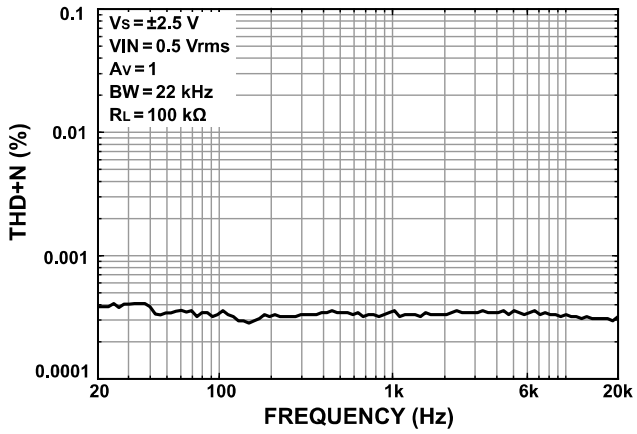

Figure 22. THD+Noise vs. Frequency

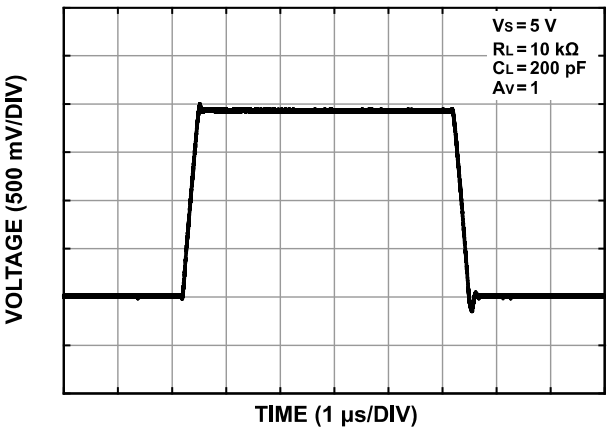

Figure 23. Large Signal Transient Response

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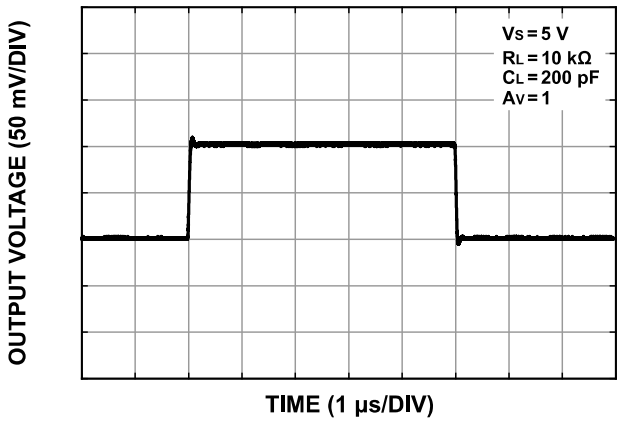

Figure 24. Small Signal Transient Response

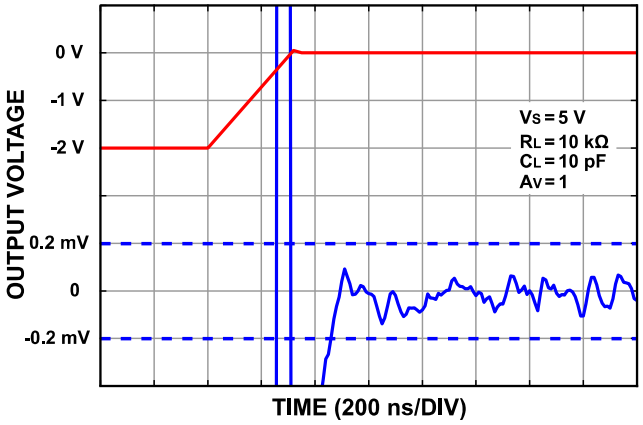

Figure 25. Rising Edge Settling

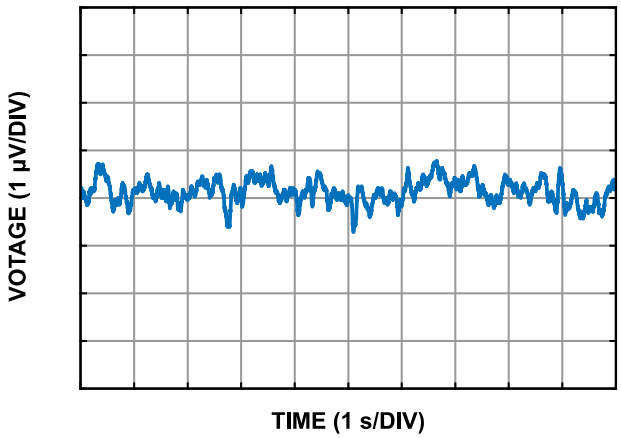

Figure 26. 0.1 Hz to 10 Hz Input Voltage Noise

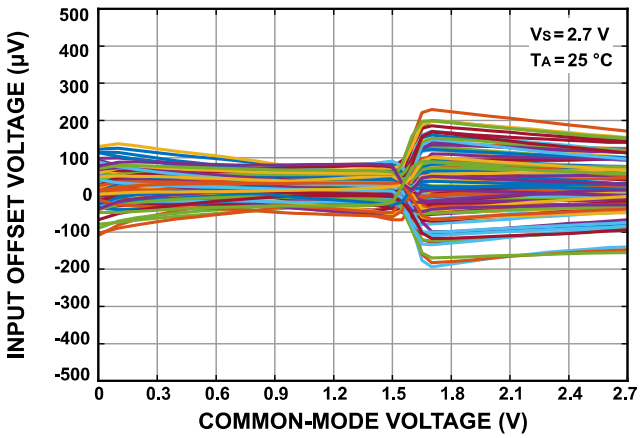

Figure 27. Input Offset vs. Common-Mode Voltage

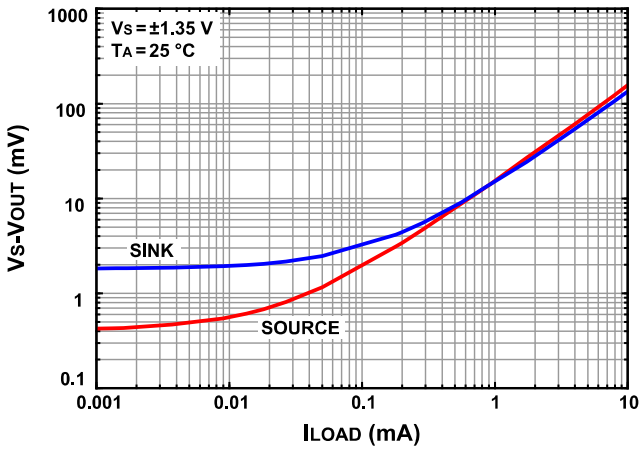

Figure 28. Output Saturation Voltage vs. Temperature

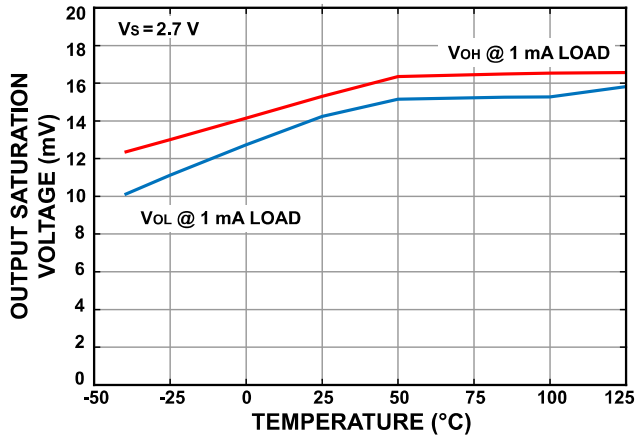

Figure 29. Output Saturation Voltage vs. Temperature

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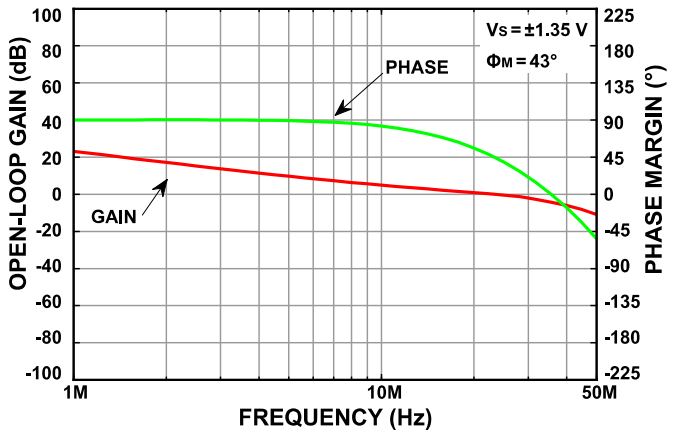

Figure 30. Open-Loop Gain and Phase vs. Frequency

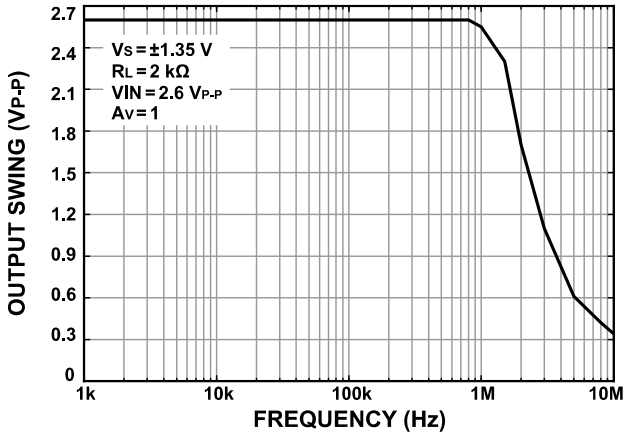

Figure 31. Close-Loop Output Swing vs. Frequency

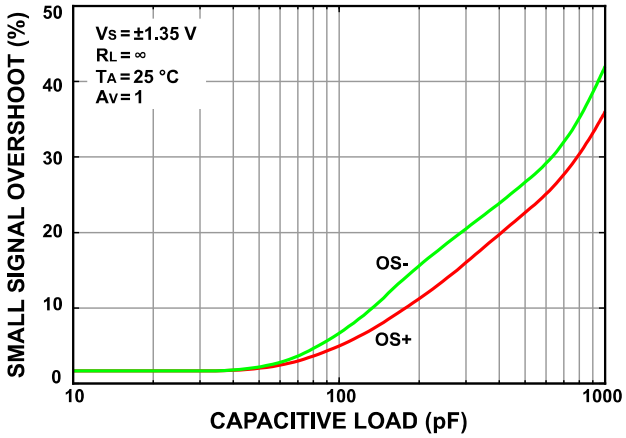

Figure 32. Small-Signal Overshoot vs. Load Capacitance

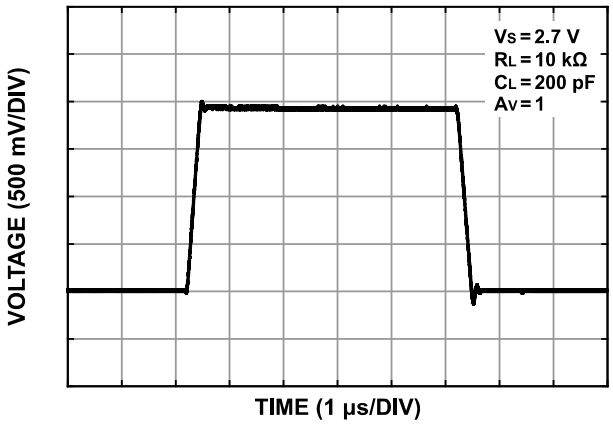

Figure 33. Large Signal Transient Response

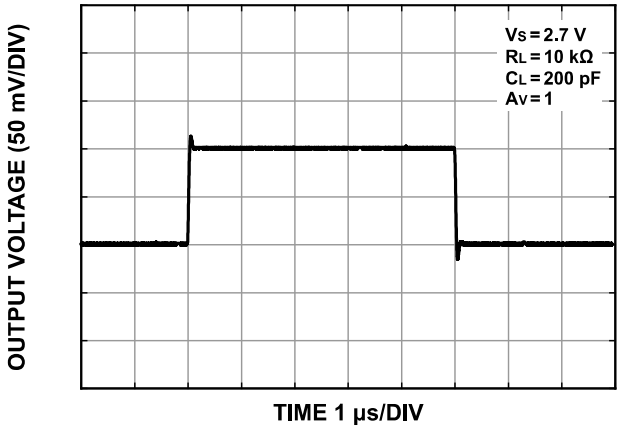

Figure 34. Small Signal Transient Response

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General Application Information

Output Phase Reversal

Phase reversal is a change of polarity in the transfer function of the amplifier. This can occur when the voltage applied at the input of an amplifier exceeds the maximum common-mode voltage. Phase reversal can cause permanent damage to the device and may result in system lockups. The ZJA3216-1, ZJA3216-2, ZJA3216-4 and ZJA3217 do not exhibit phase reversal when input voltages are beyond the supplies.

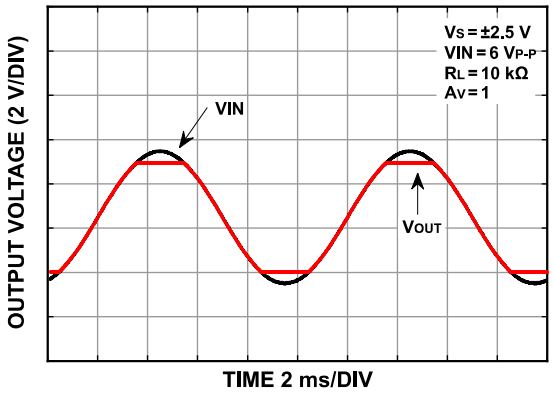

Figure 35. No Phase Reversal

THD+Noise

ZJA3216/7 features low total harmonic distortion (THD) and excellent gain linearity, making these amplifiers a great choice for precision circuits with high closed-loop gain and for audio application circuits. Figure 36 demonstrates that when configured with positive unity gain (the worst case) and driving a 100 kΩ load, the total distortion and noise of ZJA3216/7 is approximately 0.0004%.

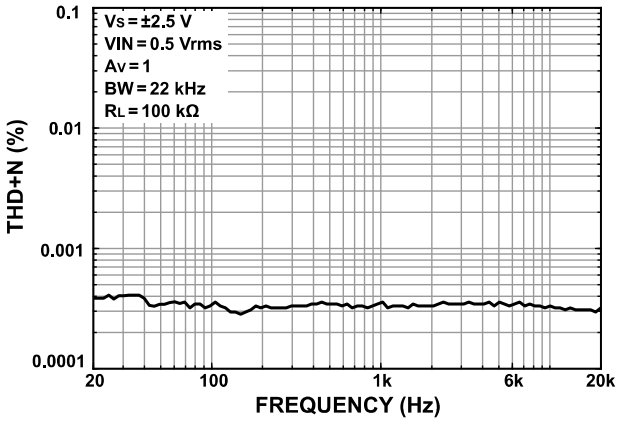

Figure 36. THD+N vs. Frequency

Total Noise Including Source Resistors

The low input current noise and input bias current of the ZJA3216/7 make it the ideal amplifier for circuits with substantial input source resistance. Input offset voltage increases by less than 15 nV per 500 Ω of source resistance at room temperature. The total noise density of the circuit is

$$e_{nTOTAL} = \sqrt{e_n^2 + (i_n R_s)^2 + 4kTR_s}$$

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Where:

e_n is the input voltage noise density of the parts.
i_n is the input current noise density of the parts.
R_S is the source resistance at the noninverting terminal.
K is Boltzman's constant (1.38×10^{-23} J/K).
T is the ambient temperature in Kelvin (T = 273 + °C).

For $R_S < 3.9$ kΩ, e_n dominates and $e_{nTOTAL} \approx e_n$.

The current noise of the ZJA3216/7 is so low that its contribution does not become a significant term unless R_S is greater than 165 MΩ, an impractical value for most applications.

The total equivalent rms noise over a specific bandwidth is expressed as:

$$e_{nRMS} = e_{nTOTAL}\sqrt{BW}$$

Where BW is the bandwidth in Hertz.

Note that the above analysis is valid for frequencies larger than 300 Hz and assumes flat noise above 10 kHz. For lower frequencies, flicker noise (1/f) must be considered.

Settling Time

Settling time is the time required for the amplifier output to reach a stable state and remain within a percentage of its step value. The pulse has been applied to the input terminal. Thanks to its high slew rate of 6.8 V/μs and 20 MHz bandwidth, ZJA3216/7 settles to within 0.01% in less than 500 ns, for a 2 V step in positive unity gain. This makes it an excellent choice as a buffer at the output of DACs whose settling time is typically less than 1 μs.

In addition to fast settling time and fast slew rate, the low offset voltage drift and input offset current of ZJA3216/7 allows full accuracy of a 16-bit converter over the entire operating temperature range.

Overload Recovery Time

Overload recovery, also known as overspeed recovery, refers to the time it takes the output of an amplifier to recover from a saturated condition to its linear region. This recovery time is particularly long, which is crucial for the application of amplifiers that must promptly response to small signal in the presence of excessive large transient. Figure 37 shows the positive overload recovery of ZJA3216/7. The output recovers from saturation within approximately 1.2 μs.

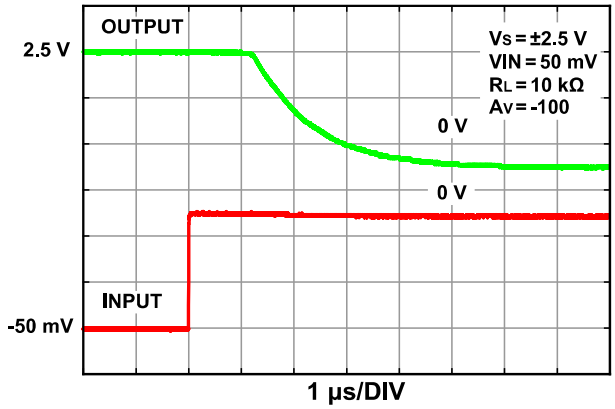

Figure 37. Positive Overload Recovery

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The negative overdrive recovery time is also approximately 1.2 μs as shown in Figure 38. In addition to the fast recovery time, ZJA3216/7 show excellent positive and negative recovery time symmetry. This is an important feature of transient signal rectification, as the output signal is kept equally undistorted throughout any given period.

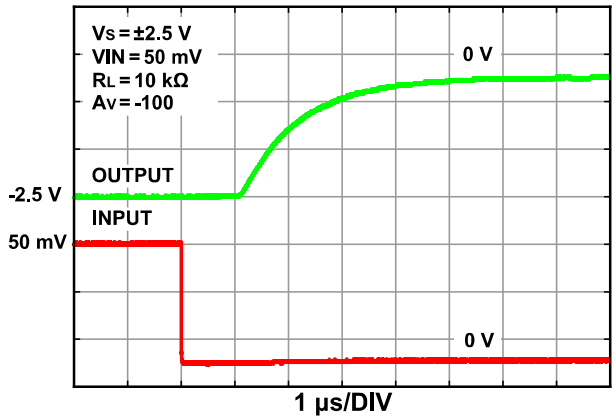

Figure 38. Negative Overload Recovery

Capacitive Load Drive

ZJA3216/7 is unconditionally stable under all gains in both inverted and non-inverting configurations. It is capable of directly driving up to 10 nF capacitive load, without oscillation under positive unity gain configuration (worst case configuration). However, as with most amplifiers, driving larger capacitive loads in a unity gain configuration may cause excessive overshoot and/or ringing, or even oscillation. A simple snubber network reduces the amount of overshoot and ringing significantly. The advantage of this configuration is that the output swing of the amplifier will not decrease, as R_S is located outside the feedback loop.

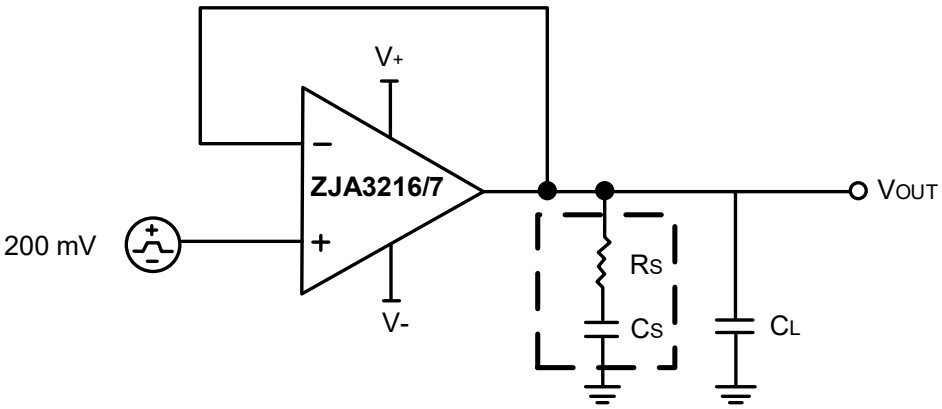

Figure 39. Snubber Network Configuration

Figure 40 shows a scope plot of the output of ZJA3216/7 in response to a 100 mV pulse. The circuit is configured as unity gain (worst case), with a load capacitance of 200 pF, and no ringing is observed at the output.

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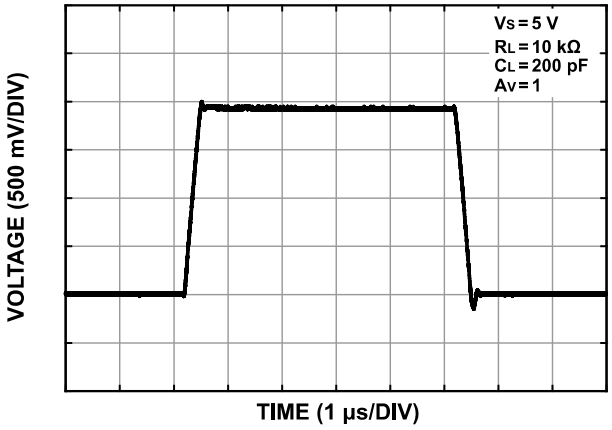

Figure 40. ZJA3216/7 Directly Drive Large Capacitive Load

However, further increase of capacitive load eventually undermines stability and leads to ringing as shown in Figure 41 for Cload of 10 nF. By adding a simple snubber network, it is able to eliminate the ringing as displayed in Figure 42.

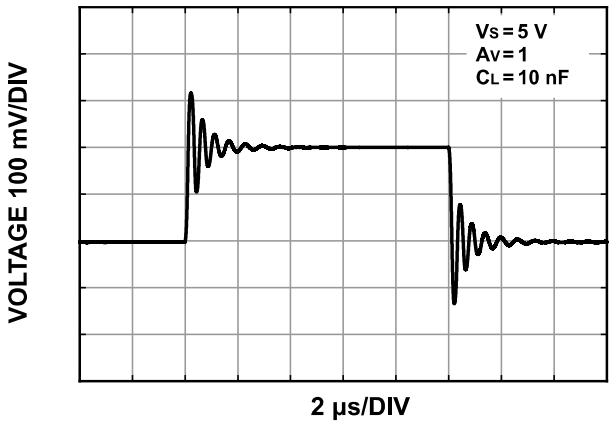

Figure 41. Direct Capacitive Load Drive of 10 nF

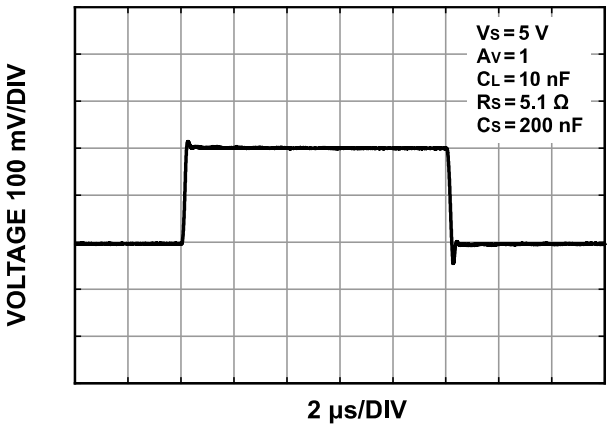

Figure 42. Capacitive Load Drive of 10 nF with Snubber

The optimal values of R_S and C_S depend on the load capacitance and input capacitance of ZJA3216/7, which is summarized in Table 1.

C_L	R_S (Ω)	C_S
1 nF	100	10 nF
2 nF	50	10 nF
5 nF	20	10 nF

Table 1. Optimum Values for Capacitive Loads

Open-Loop Gain and Phase Response

In addition to impressive low noise, low offset voltage and offset current, ZJA3216/7 has excellent loop gain and phase response even when driving heavy resistive or capacitive load. When the output is loaded with 2.5 kΩ resistor, ZJA3216/7 has unity gain frequency of 20 MHz and a phase margin of 49°. Comparing to amplifiers with similar bandwidth, ZJA3216/7 is much more stable, showing much less peaking in transient response and thus much faster settling time.

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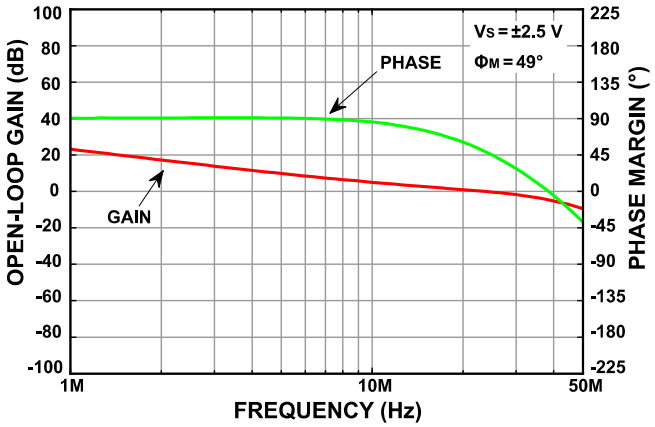

Figure 43. Frequency Response of ZJA3216/7

Photodiode Circuits

Common applications for I-V conversion include photodiode circuits, where the amplifier is used to convert a current, generated by a photo diode placed at the inverting input terminal, into an output voltage.

ZJA3216/7's low input bias current, wide bandwidth, and low noise make it an excellent choice for various photodiode applications, including fiber optic controls, motion sensors, and bar code readers.

The circuit shown in Figure 44 uses a silicon diode with zero bias voltage. This is known as a Photovoltaic Mode; this configuration limits the overall noise and is suitable for instrumentation applications.

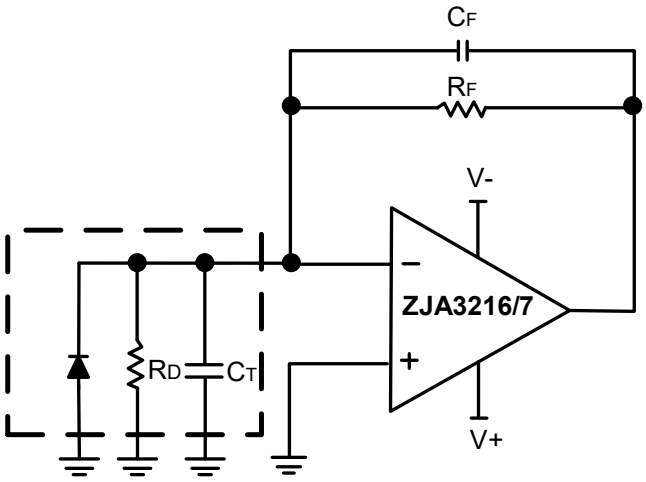

Figure 44. Equivalent Preamplifier Photodiode Circuit

A larger signal bandwidth can be attained at the expense of additional output noise. The total input capacitance (C_T) consists of the sum of the diode capacitance (typically 3 pF to 4 pF) and the amplifier's input capacitance (12 pF), which includes external parasitic capacitance. C_T creates a pole in the frequency response, which may lead to an unstable system. To ensure stability and optimize the bandwidth of the signal, a capacitor is placed in the feedback loop of the circuit shown in Figure 44. It creates a zero and yields a bandwidth whose corner frequency is $1 / (2\pi (R_F C_F))$.

The value of R_F can be determined by the ratio V/I_D, where V is the desired output voltage of the op amp and I_D is the diode current. For example, if I_D is 100 µA and a 10 V output voltage is desired, R_F should be 100 kΩ. R_D is a junction resistance that drops typically by a factor of 2 for every 10 °C increase in temperature. A typical value for R_D is 1000 MΩ. Since $R_D >> R_F$, the circuit behavior is not impacted by the effect of the junction resistance. The maximum signal bandwidth is

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$$f_{MAX} = \sqrt{\frac{f_T}{2\pi R_F C_T}}$$

where f_T is the unity gain frequency of the amplifier.

Using the parameters above, $C_F \approx 1$ pF, which yields a signal bandwidth of about 2.6 MHz.

$$C_F = \sqrt{\frac{C_T}{2\pi R_F f_T}}$$

where f_T is the unity gain frequency of the op amp, achieves a phase margin, Φm, of approximately 45°.

A higher phase margin can be obtained by increasing the value of C_F. Setting C_F to twice the previous value yields approximately $\Phi_m = 65°$ and a maximally flat frequency response, but reduces the maximum signal bandwidth by 50%.

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Outline Information

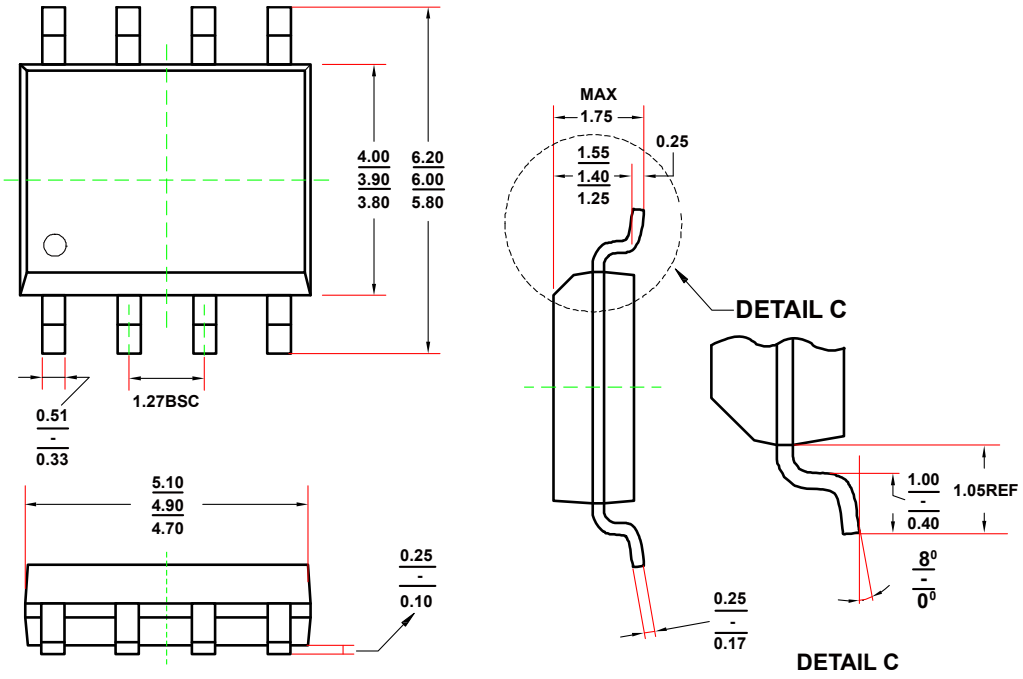

Figure 45. 8-Lead SOIC Package Dimensions shown in millimeters

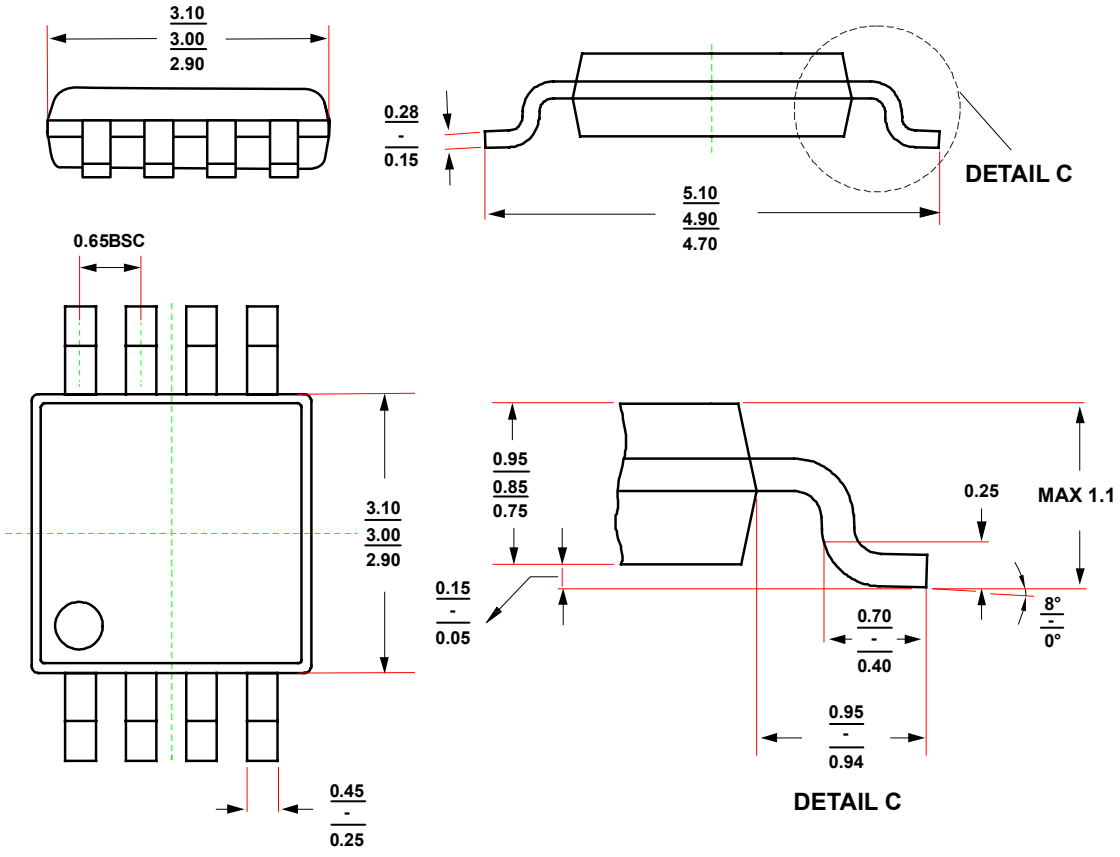

Figure 46. 8-Lead MSOP Package Dimensions shown in millimeters

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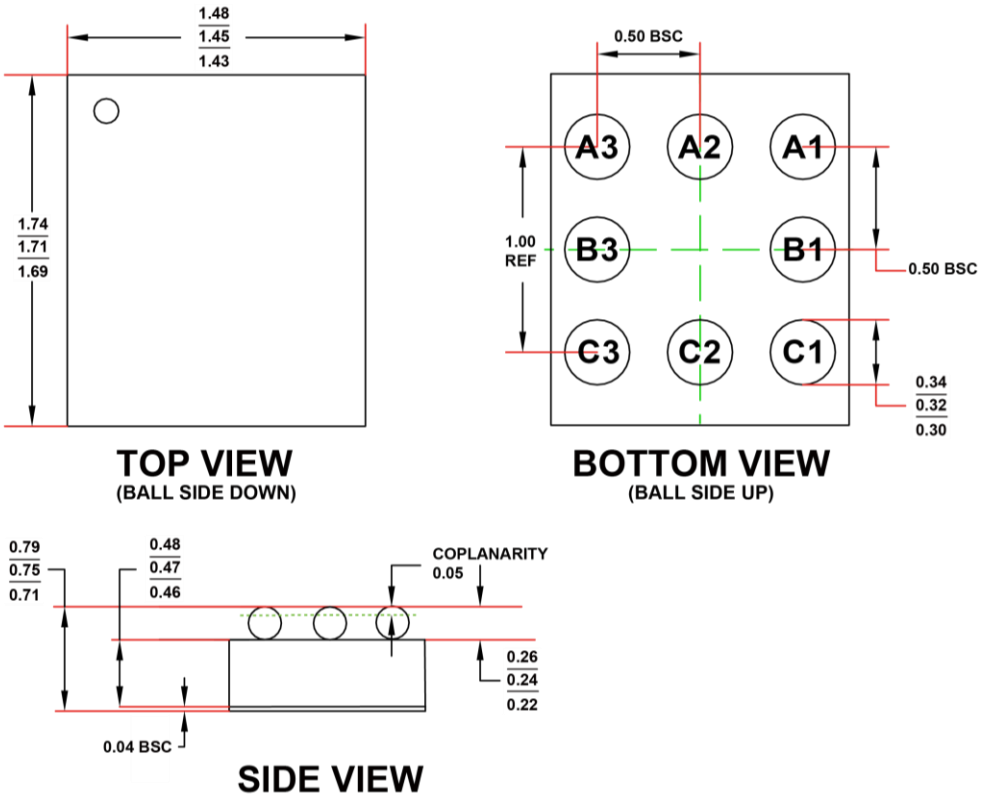

Figure 47. 8-Ball WLCSP Package Dimensions shown in millimeters

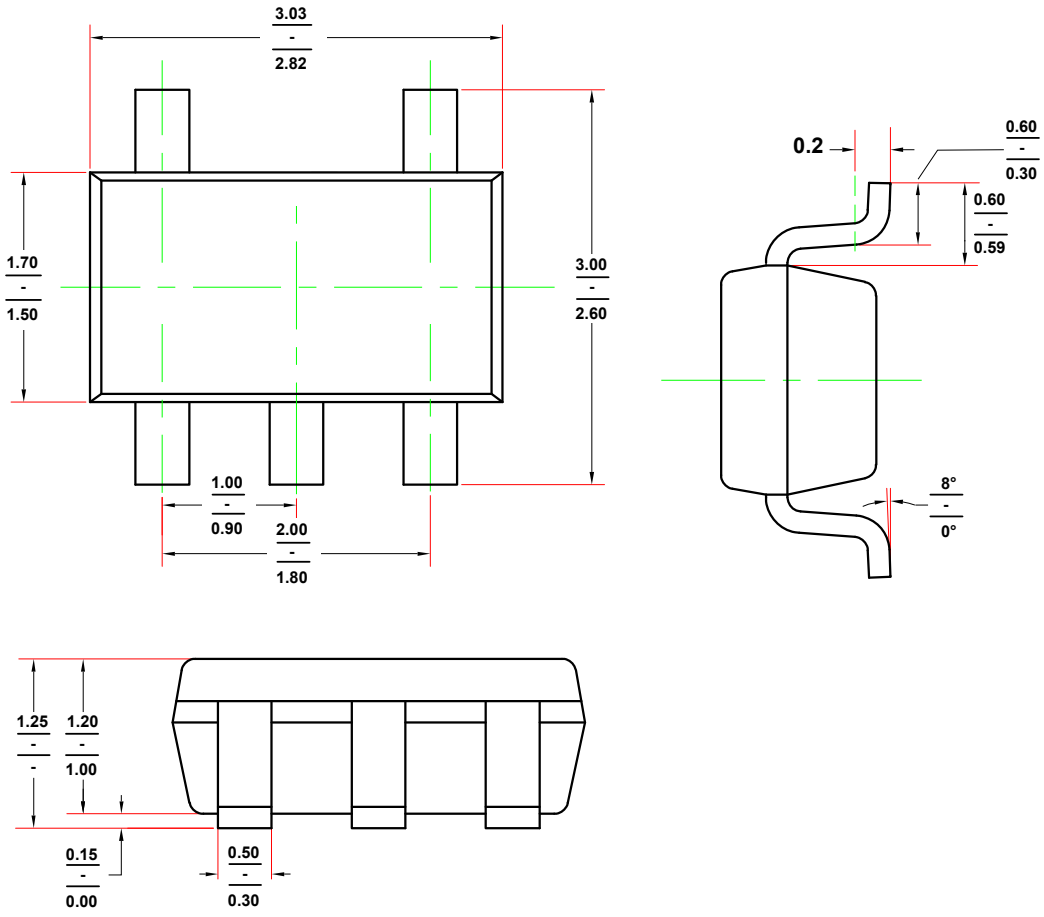

Figure 48. 5-Lead SOT23 Package Dimensions shown in millimeters

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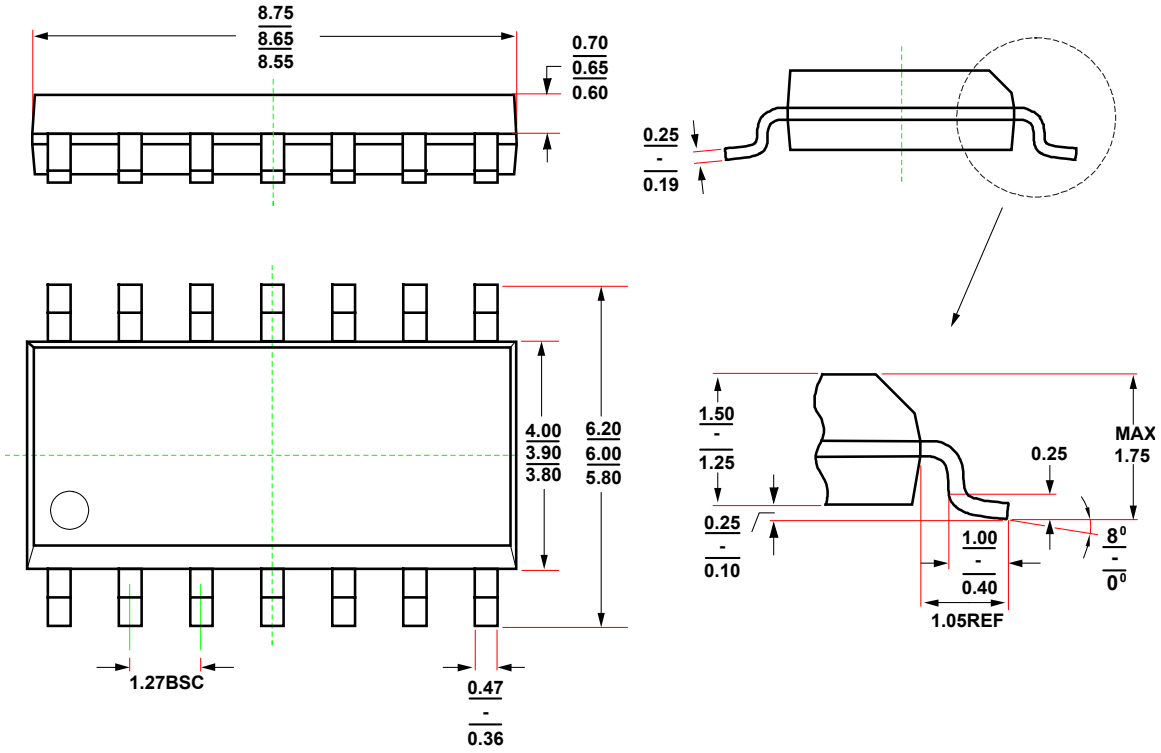

Figure 49. 14-Lead SOIC Package Dimensions shown in millimeters

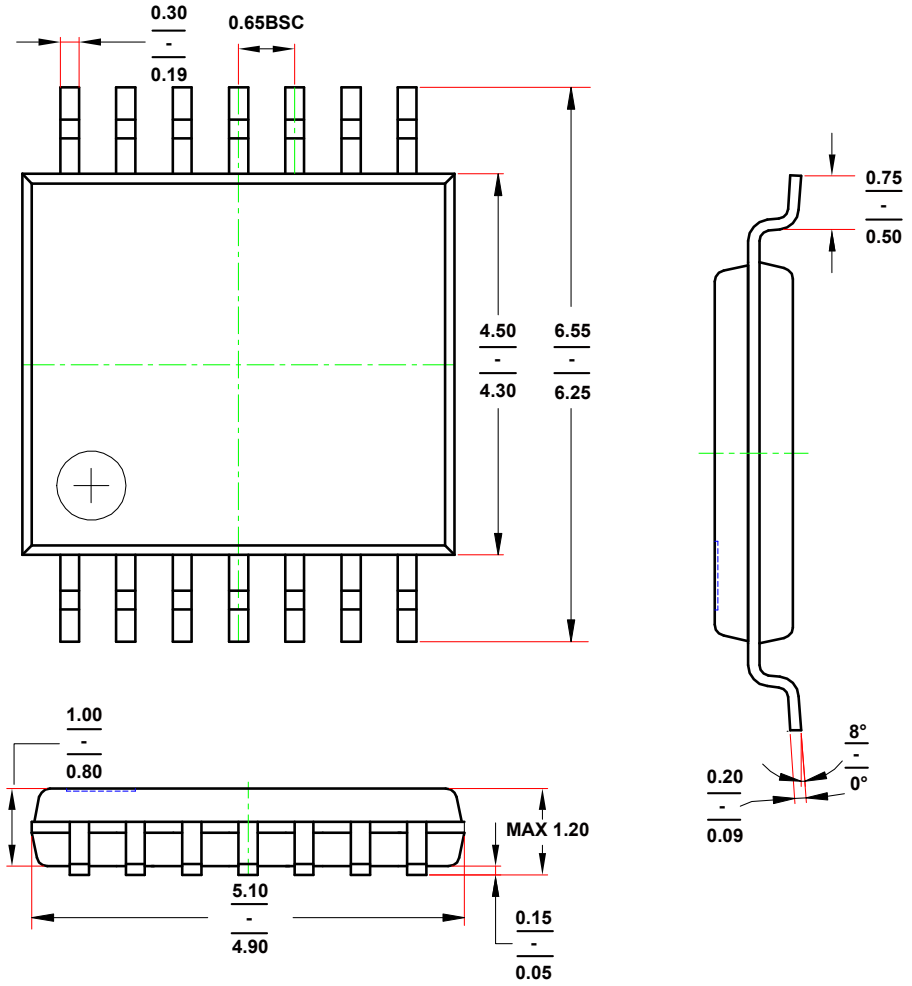

Figure 50. 14-Lead TSSOP Package Dimensions shown in millimeters

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Ordering Guide

Model	Orderable Device	Channels	Package	Temperature Range (°C)	External Package
ZJA3216-1	ZJA3216-1AUKBR	1	SOT23-5	-40 to +125	7” Reel
ZJA3216-2	ZJA3216-2ASABT	2	SOIC-8	-40 to +125	Tube
	ZJA3216-2ASABR				13” Reel
	ZJA3216-2AUABT		MSOP-8		Tube
	ZJA3216-2AUABR				13” Reel
	ZJA3216-2AWABR		WLCSP-8		7” Reel
ZJA3216-4	ZJA3216-4ASDBT	4	SOIC-14	-40 to +125	Tube
	ZJA3216-4ASDBR				13” Reel
	ZJA3216-4AUDBT		TSSOP-14		Tube
	ZJA3216-4AUDBR				13” Reel
ZJA3217	ZJA3217AUKBR	1	SOT23-5	-40 to +125	7” Reel

Product Order Model

ZJXXXXX X X X X X Q1

- Q1: Automotive Grade
- External Package: T = Tube; R = Reel
- Temperature Range: A = -40 °C to 125 °C Automotive Grade 1, B = -40 °C to 125 °C; E = -40 °C to 85 °C
- Number of Pins: R = 3; K =5; T = 6, A = 8; B = 10; D = 14; E = 16; P = 20
- Package Type: S = SOIC; U = MSOP, TSSOP, SOT; T = DFN, QFN; X = SC70; W = WLCSP; Z = TSOT23
- Grade: B grade is better than A grade
- Base: R = Voltage reference; A = Amplifier; C = Data Converter; G = Switches and Multiplexers; M = Others

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Related Parts

Part Number	Description	Comments
ADC		
ZJC2020	20-bit 350 kSPS SAR ADC	Fully differential input, SINAD 101.4 dB, THD -118 dB
ZJC2000/2010	18-bit 400 kSPS/200 kSPS SAR ADC	Fully differential input, SINAD 99.3 dB, THD -113 dB
ZJC2001/2011	16-bit 500 kSPS/250 kSPS SAR ADC	Fully differential input, SINAD 95.3 dB, THD -113 dB
ZJC2002/2012 ZJC2003/2013	16-bit 500 kSPS/250 kSPS SAR ADC	Pseudo-differential unipolar input, SINAD 91.7 dB, THD -105 dB Pseudo-differential bipolar input, SINAD 91.7 dB, THD -105 dB
ZJC2004/2014 ZJC2005/2015	18-bit 400 kSPS/200 kSPS SAR ADC	Pseudo-differential unipolar input, SINAD 94.2 dB, THD -105 dB Pseudo-differential bipolar input, SINAD 94.2 dB, THD -105 dB
ZJC2007/2017 ZJC2008/2018	14-bit 600 kSPS/300 kSPS SAR ADC	Pseudo-differential unipolar input, SINAD 85 dB, THD -105 dB Pseudo-differential bipolar input, SINAD 85 dB, THD -105 dB
ZJC2009	Small size, 12-bit 1 MSPS SAR ADC	Single-ended input, SOT23-6, 2.3 V to 5 V, SINAD 73 dB, THD -89 dB
ZJC2100/1-18 ZJC2100/1-16	18-bit 400 kSPS/200 kSPS 4-ch differential SAR ADC, SINAD 99.3 dB, THD -113 dB 16-bit 500 kSPS/250 kSPS 4-ch differential SAR ADC, SINAD 95.3 dB, THD -113 dB	
ZJC2102/3-18 ZJC2102/3-16 ZJC2102/3-14	18-bit 400 kSPS/200 kSPS 8-ch pseudo-differential SAR ADC, SINAD 94.2 dB, THD -105 dB 16-bit 500 kSPS/250 kSPS 8-ch pseudo-differential SAR ADC, SINAD 91.7 dB, THD -105 dB 14-bit 600 kSPS/300 kSPS 8-ch pseudo-differential SAR ADC, SINAD 85 dB, THD -105 dB	
ZJC2104/5-18 ZJC2104/5-16	18-bit 400 kSPS/200 kSPS 4-ch pseudo-differential SAR ADC, SINAD 94.2 dB, THD -105 dB 16-bit 500 kSPS/250 kSPS 4-ch pseudo-differential SAR ADC, SINAD 91.7 dB, THD -105 dB	
DAC		
ZJC2541-18/16/14 ZJC2543-18/16/14	18/16/14-bit 1 MSPS single channel DAC with unipolar output	Power on reset to 0 V (ZJC2541) or V_{REF}/2 (ZJC2543), 1 nV-S glitch, SOIC-8, MSOP-10/8, DFN-10 packages
ZJC2542-18/16/14 ZJC2544-18/16/14	18/16/14-bit 1 MSPS single channel DAC with bipolar output	Power on reset to 0 V (ZJC2542) or V_{REF}/2 (ZJC2544), 1 nV-S glitch, SOIC-14, TSSOP-16, QFN-16 packages
Amplifier		
ZJA3000-1/2/4 ZJA3001-1/2/4	Single/Dual/Quad 36 V low bias current precision Op Amps	3 MHz, 35 µV max Vos, 0.5 µV/°C max TCVos, 25 pA max Ibias, 1 mA/ch, input to V- (ZJA3000 only), RRO, 4.5 V to 36 V
ZJA3018-2 ZJA3008-2	OVP ±75 V, 36 V, Low Power, High Precision Op Amp 36 V, Low Power, High Precision Op Amp	1.3 MHz, 10 µV max Vos, 0.5 µV/°C max TCVos, 25 pA max Ibias, 0.5 mA/ch, OVP ±75 V (ZJA3018 only), RRO, 4.5 V to 36 V
ZJA3512-2	Dual 36 V 7 MHz precision JFET Op Amps	7 MHz, 35 V/µS, 50 µV max Vos, 1 µV/°C max TCVos, 2 mA/ch, RRO, 9 V to 36 V
ZJA3216/06/02-1/2	Precision 20/10/5 MHz CMOS RRIO Op Amps	20/10/5 MHz, RRIO, 30 µV max Vos, 1 µV/°C max TCVos, 0.6 pA Ib, 2.7 V to 5.5 V
ZJA3600/1	36 V ultra-high precision in-amp	CMRR 105 dB min (G = 1), 25 pA max Ib, 25 µV max Vosi, ±2.4 V to ±18 V, -40 °C to 125 °C
ZJA3611, ZJA3609	36 V precision wider bandwidth precision in-amp (G ≥ 10)	CMRR 120 dB min (G = 10), 25 pA max Ibias, 25 µV max Vosi, 1.2 MHz BW (G = 10)
ZJA3676/7 ZJA3678/9	Low power, G=1 Single/Dual 36 V difference amplifier Low power, G=0.5/2 Single/Dual 36 V difference amplifier	Input protection to ±65 V, CMRR 104 dB min (G = 1), Vos 100 µV max, gain error 15 ppm max, 500 kHz BW (G = 1), 330 µA/channel, 2.7 V to 36 V
ZJA3669	High Common-Mode Voltage Difference Amplifier	±270 V CMV, 2.5 kV ESD, 96 dB min CMRR, 450 kHz BW, 4 V to 36 V, SOIC-8
ZJA3100	15 V precision fully differential amplifier	145 MHz, 447 V/µS, 50 nS to 16-bit, 50 µV max Vos, 4.6 mA Iq, SOIC/MSOP-8, QFN-16
ZJA3236/26/22-2	Low-cost 20/10/5 MHz CMOS RRIO Op Amps	20/10/5 MHz, RRIO, 2 mV max Vos, 6 µV/°C max TCVos, 0.6 pA Ib, 2.7 V to 5.5 V
ZJA3622/8	36 V low-cost precision in-amp	0.5 nA max Ibias, 125 µV max Vosi, 625 kHz BW (G = 10), 3.3 mA Iq, ±2.4 V to ±18 V
Voltage Reference		
ZJR1004	40 V supply precision voltage reference	V_{OUT} = 2.048/2.5/3/3.3/4.096/5/10 V, 5 ppm/°C max drift -40 °C to 125 °C
ZJR1001/2 ZJR1003	5.5 V low power voltage reference (ZJR1001 with noise filter option)	V_{OUT} = 2.048/2.5/3/3.3/4.096/5 V, 5 ppm/°C max drift -40 °C to 125 °C, ±0.05% initial error, 130 µA, ZJR1001/2 in SOT23-6, ZJR1003 in SOIC/MSOP-8
ZJR1302	5.5 V low power compact precision voltage reference	V_{OUT} = 2.048/2.5/3/3.3/4.096 V, 30 ppm/°C max drift -40 °C to 125 °C, 130 µA, SOT23-3
Switches and Multiplexers		
ZJG4438/4439	36 V fault protection 8:1/dual 4:1 multiplexer	Protection to ±50 V power on & off, latch-up immune, Ron 270 Ω, 14.8 pC, t_{ON} 166 nS
ZJG4428/4429	36 V 8:1/dual 4:1 multiplexer	Latch-up immune, Ron 270 Ω, 14.8 pC charge injection, t_{ON} 166 nS
Quad Matching Resistor		
ZJM5400	±75 V precision match resistors	Mismatch < 100 ppm, 10k:10k:10k:10k, 100k:100k:100k:100k, 100k:10k:10k:100k, 1k:1k:1k:1k 1M:1M:1M:1M, 5k:1k:1k:5k, 5k:1.25k:1.25k:5k, 9k:1k:1k:9k, ESD: 3.5 kV

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