8-Channel, 16/12-Bit, Voltage Output DAC with Reference

Features

- 16/12-bit Resolution
- 8 Channel Buffered Voltage Output
- DNL: ±0.8 LSB for 16-bit
- INL: ±1.5 LSB for 16-bit
- 5 µs Settling Time
- Low Glitch: 2 nV-s
- Internal 2.5 V Reference: 5 ppm/°C (ZJC2676-16R/12R only)
- Power Supply: 2.7 V to 5.5 V
- 0.2 mA per Channel at 5.0 V
- Package: QFN (LFCSP)-20 or TSSOP-20
- Operating Temperature Range: -40 °C to +125 °C

Application

- Precision Control Equipment
- Optical Networking
- Industrial Automation

General Description

ZJC2676-16/12(R) (hereinafter referred to as ZJC2676-16/12R with internal reference, or ZJC2676-16 without internal reference) is an 8-channel, buffered voltage-output 16/12-bit resolution precision digital-to-analog converter (DAC). It includes a 2.5 V, 5 ppm/°C internal reference (ZJC2676-16/12R only). Monotonicity is guaranteed and can guarantee DNL/INL accuracy over temperature range of -40 °C to +125 °C. Register (for QFN-20) or pin (for TSSOP-20) configurable gain options 1 or 2 provide full-scale output voltages of 2.5 V or 5 V.

It can operate from a single 2.7 V to 5.5 V V_{DD} supply, while V_{IO} enables digital serial interface from 1.7 V to 5.5 V.

The ZJC2676-16/12(R) has an internal power-on-reset circuitry which makes it power up and maintain all the DAC outputs at either zero scale or midscale until a valid code is configured. ZJC2676-16/12(R) in QFN-20 outputs power up to zero scale; ZJC2676-16/12(R) in TSSOP-20 outputs power up to zero scale (RSTSEL pin low) or midscale (RSTSEL pin high).

Block Diagram

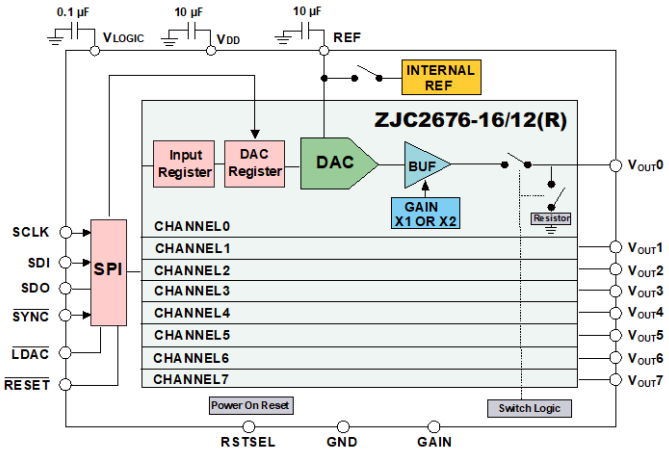

Figure 1. ZJC2676-16/12(R)Family Block Diagram

Typical Performance Characteristics

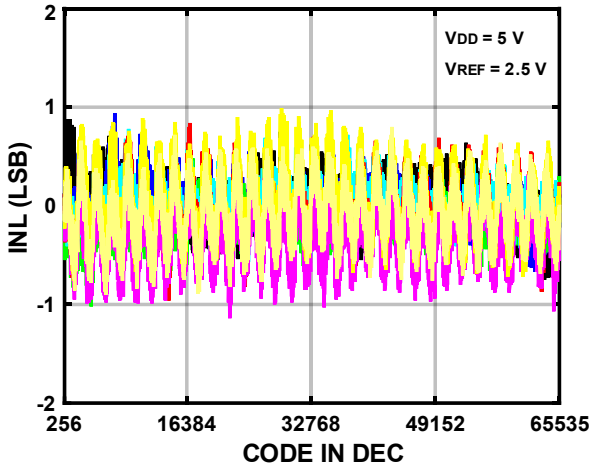

Figure 2. ZJC2676-16R Typical INL

16-bit DAC series models are as follows:

Resolution(bit)	DAC Model	Internal Reference	Power-on Output	Pin Control	Package
16	ZJC2676-16R	Yes	Zero	NA	QFN-20
		Yes	Zero scale or Midscale	RSTSEL	TSSOP-20
	ZJC2676-16	No	Zero	NA	QFN-20
		No	Zero scale or Midscale	RSTSEL	TSSOP-20
12	ZJC2676-12R	Yes	Zero	NA	QFN-20
		Yes	Zero scale or Midscale	RSTSEL	TSSOP-20
	ZJC2676-12	No	Zero	NA	QFN-20
		No	Zero scale or Midscale	RSTSEL	TSSOP-20

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Version History (Release B) [1]

Apr. 2026 — Release B

Update Family Block Diagram and Related Parts

Aug. 2025

Update Ordering Guide and Product Order Model

Jun. 2025 — Release A

Mar. 2025 — Preliminary

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Pin Configuration and Function

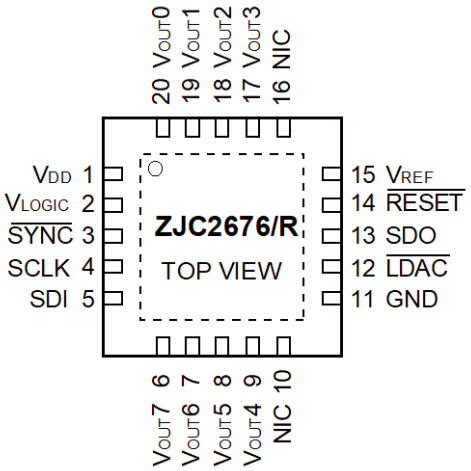

Figure 3. ZJC2676-16/12(R) in 20-Pin QFN (LFCSP)

Mnemonic	Pin No.	Pin Type	Description
V_{DD}	1	Power Supply	Supply voltage input.
V_{LOGIC}	2	Power Supply	Digital interface supply voltage. This pin sets the I/O operating voltage.
$\overline{SYNC}$	3	Digital Input	Active low chip selection. When the signal goes low, it enables the serial interface input shift register. In asynchronous mode, a write to the DAC data register results in an immediate update of the DAC active register and DAC output on $\overline{SYNC}$ rising edge.
SCLK	4	Digital Input	Serial interface clock.
SDI	5	Digital Input	Serial data input. Data bits are clocked into the input shift register on each falling edge of the SCLK while $\overline{SYNC}$ is low.
$V_{OUT}7$	6	Analog Output	DAC channel 7 analog output voltage.
$V_{OUT}6$	7	Analog Output	DAC channel 6 analog output voltage.
$V_{OUT}5$	8	Analog Output	DAC channel 5 analog output voltage.
$V_{OUT}4$	9	Analog Output	DAC channel 4 analog output voltage.
NIC	10	NC	No Internal Connection.
GND	11	Ground	Ground.
$\overline{LDAC}$	12	Digital Input	Load DAC. $\overline{LDAC}$ operates in two modes, asynchronously and synchronously. For asynchronous mode, $\overline{LDAC}$ should be tied low, and DAC outputs update on $\overline{SYNC}$ rising edge; For asynchronous mode, Putting this pin low allows any or all DAC registers to be updated which allows all DAC outputs to update simultaneously.
SDO	13	Digital Output	Serial data output. The SDO pin is in high impedance when $\overline{SYNC}$ pin is high. Data are clocked out of the input shift register on rising edges of the SCLK.
$\overline{RESET}$	14	Digital Input	Asynchronous Input. The $\overline{RESET}$ input is falling edge sensitive. When $\overline{RESET}$ is low, all $\overline{LDAC}$ pulses are ignored. When $\overline{RESET}$ is activated, the input registers and the DAC registers are updated with zero scale.
V_{REF}	15	Analog Input or Output	When using the internal reference, this is the reference output voltage pin (default); When using an external reference, this is the reference input pin.
NIC	16	NC	No Internal Connection.
$V_{OUT}3$	17	Analog Output	DAC channel 3 analog output voltage.
$V_{OUT}2$	18	Analog Output	DAC channel 2 analog output voltage.
$V_{OUT}1$	19	Analog Output	DAC channel 1 analog output voltage.
V_{OUT}	20	Analog Output	DAC channel 0 analog output voltage.
EP	EP	Exposed PAD	The exposed pad should be tied to GND.

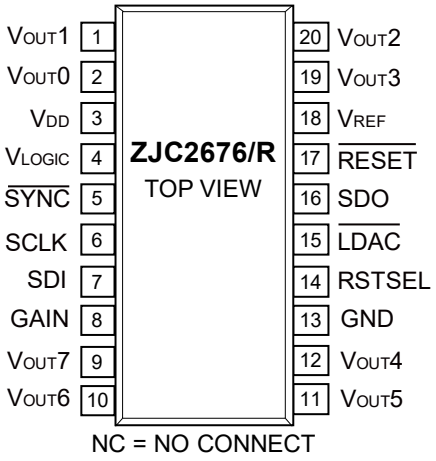

Figure 4. ZJC2676-16/12(R) in 20-Pin TSSOP

Mnemonic	Pin No.	Pin Type	Description
$V_{OUT}1$	1	Analog Output	DAC channel 1 analog output voltage.
$V_{OUT}0$	2	Analog Output	DAC channel 0 analog output voltage.
V_{DD}	3	Power Supply	Supply voltage input.
V_{LOGIC}	4	Power Supply	Digital interface supply voltage. This pin sets the I/O operating voltage.
$\overline{SYNC}$	5	Digital Input	Active low chip selection. When the signal goes low, it enables the serial interface input shift register. In asynchronous mode, a write to the DAC data register results in an immediate update of the DAC active register and DAC output on $\overline{SYNC}$ rising edge.
SCLK	6	Digital Input	Serial interface clock.
SDI	7	Digital Input	Serial data input. Data bits are clocked into the input shift register on each falling edge of the SCLK while $\overline{SYNC}$ is low.
GAIN	8	Digital Input	Output amplifier gain set pin. When it is tied to low or GND, all eight DAC outputs have a range from 0 V to V_{REF}. If it is tied to high or V_{LOGIC}, all eight DACs output have a range of 0 V to 2 × V_{REF}. After power-up, It changes the output gain option dynamically. Gain setup by register bit is invalid.
$V_{OUT}7$	9	Analog Output	DAC channel 7 analog output voltage.
$V_{OUT}6$	10	Analog Output	DAC channel 6 analog output voltage.
$V_{OUT}5$	11	Analog Output	DAC channel 5 analog output voltage.
$V_{OUT}4$	12	Analog Output	DAC channel 4 analog output voltage.
GND	13	Ground	Ground.
RSTSEL	14	Digital Input	Power-On V_{OUT} Reset Select Pin. Tie it to low or GND to power up all eight DAC outputs to zero scale. Tie this pin to high or V_{LOGIC} to power up all eight DACs to midscale.
$\overline{LDAC}$	15	Digital Input	Load DAC. $\overline{LDAC}$ operates in two modes, asynchronously and synchronously. For asynchronous mode, $\overline{LDAC}$ should be tied permanently low, and DAC outputs update on $\overline{SYNC}$ rising edge; For asynchronous mode, Putting this pin low allows any or all DAC registers to be updated which allows all DAC outputs to update simultaneously.
SDO	16	Digital Output	Serial data output. The SDO pin is in high impedance when $\overline{SYNC}$ pin is high. Data are clocked out of the input shift register on rising edges of the SCLK.
$\overline{RESET}$	17	Digital Input	Asynchronous Input. The $\overline{RESET}$ input is falling edge sensitive. When $\overline{RESET}$ is low, all $\overline{LDAC}$ pulses are ignored. When $\overline{RESET}$ is activated, the input register and the DAC register are updated with zero scale.
VREF	18	Analog Input or Output	When using the internal reference, this is the reference output voltage pin (default); When using an external reference, this is the reference input pin.
$V_{OUT}3$	19	Analog Output	DAC channel 3 analog output voltage.
$V_{OUT}2$	20	Analog Output	DAC channel 2 analog output voltage.

Absolute Maximum Ratings [1]

Parameter	Rating
V_{DD}, V_{LOGIC} to GND	-0.3 V ~ +6 V
V_{REF} to GND	-0.3 V ~ V_{DD} + 0.3 V
Digital Input to GND	-0.3 V ~ V_{LOGIC} + 0.3 V
Input current to pins except V_{DD}	±10 mA
Storage Temperature Range	-65 °C ~ +150 °C
Junction Temperature Range	150 °C
Lead Temperature (Soldering, 10 seconds)	300 °C
Maximum Reflow Temperature [2]	260 °C
Electrostatic Discharge (ESD) [3]	
Human Body Model (HBM) [4]	3 kV
Charged Device Model (CDM) [5]	1 kV

Thermal Resistance [6]

Package Type	θ_{JA}	θ_{JC}	Unit
QFN-20	51	27	°C/W
TSSOP-20	99	18	°C/W

[1] These ratings apply at 25 °C, unless otherwise noted. Stresses above these ratings may cause permanent damage. Exposure to absolute maximum conditions for extended periods may degrade device reliability. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those specified is not implied.

[2] IPC/JEDEC J–STD-020 Compliant.

[3] Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

[4] ANSI/ESDA/JEDEC JS-001 Compliant.

[5] ANSI/ESDA/JEDEC JS-002 Compliant.

[6] θ_{JA} addresses the conditions for soldering devices onto circuit boards to achieve surface mount packaging.

Specifications

The ● denotes the full temperature range for specified performance. Unless otherwise noted. V_{DD} = 2.7 V ~ 5.5 V, R_{LOAD} = 2 kΩ to GND, C_{LOAD} = 200 pF to GND, T_A = 25 °C, GND = 0 V.

Parameter	Symbol	Conditions			Min	Typ.	Max	Unit
Resolution								
16-bit							16	bits
12-bit							12	
Accuracy								
Integral Nonlinear Error	INL	16 bits		●	-4	±1.5	+4	LSB
		12 bits		●	-1	±0.5	+1	
Differential Nonlinear Error	DNL	16 bits		●	-1	±0.8	+1	LSB
		12 bits		●	-0.25	±0.2	+0.25	
Total Unadjusted Error	TUE	Gain = 1		●		±0.05	±0.15	%FSR
		Gain = 2		●		±0.04	±0.12	
Gain Error	GE	16 bits	Gain = 1	●		±0.04	±0.12	%
			Gain = 2	●		±0.02	±0.06	
Gain Error Temperature Drift						±3		ppm/°C
Offset Error		16 bits		●		±0.5		mV
Offset Error Temperature Coefficient						±5		μV/°C
Zero-code Error	ZCE	16/12-bit		●		1.0		mV
Zero-code Error Drift						±8		ppm/°C
Full-scale Error		16-bit	Gain = 1	●		±0.04	±0.15	%
			Gain = 2	●		±0.02	±0.1	
Full-scale Error Drift						±3		ppm/°C
DC PSRR		DAC Code = Midscale, V_{DD} = 5 V ± 10%				0.1		mV/V
DC Crosstalk		Due to Single Channel, Full-scale Output Change				±2.5		μV
		Due to Load Current Change				±3		μV/mA
		Due to Powering Down (per channel)				±3		μV
Output Characteristics								
Output Voltage Range		Gain = 2		●	0		2 * V_{REF}	V
		Gain = 1		●	0		V_{REF}	
Capacitive Load Stability		R_L = ∞				2		nF
		R_L = 1 kΩ				10		
Short Current		DAC Code = Full Scale. Output Shorted to GND				40		mA
		DAC Code = Zero Scale. Output Shorted to V_{DD}				40		
Load regulation		DAC Code = Midscale, -30 mA ≤ I_{OUT} ≤ 30 mA, V_{DD} = 5 V ± 10%				150		μV/mA
		DAC Code = Midscale, -20 mA ≤ I_{OUT} ≤ 20 mA, V_{DD} = 3 V ± 10%				150		
DC Output Impedance		DAC Code = Midscale				0.08		Ω
		DAC Output at GND or V_{DD}				18		
Power-up Time		Exiting Power-down Mode, V_{DD} = 5 V				12		μs
Output Characteristics								
Output Settling Time		¼ to ¾ scale and ¾ to ¼ scale settling time to ±2 LSB, V_{DD} = 5.5 V, V_{REF} = 2.5 V, Gain = 2				5		μs
Slew Rate	SR	V_{REFIN} = 2.5 V, Gain = 2				1		V/μs
Digital to Analog Glitch Impulse		(Internal Reference, Gain = 1)				2		nV-s
Output Noise		0.1 Hz to 10 Hz, DAC Code = Midscale, Gain = 1				6		μV_{P-P}
Output Noise Density		DAC Code = Midscale, 10 kHz, Gain = 2, External Reference				75		$nV/\sqrt{Hz}$
		DAC Code = Midscale, 10 kHz, Gain = 2, Internal Reference, C_L = 10 nF				250		

Parameter	Symbol	Conditions		Min	Typ.	Max	Unit
Total Harmonic Distortion	THD	At T_A, Bandwidth = 20 kHz, V_{DD} = 5 V, f_{OUT} = 1 kHz			-72		dB
Signal to Noise Ratio	SNR	At T_A = 25 °C, Bandwidth = 20 kHz, V_{DD} = 5 V, f_{OUT} = 1 kHz			70		dB
Spurious Free Dynamic Range	SFDR	At T_A = 25 °C, bandwidth = 20 kHz, V_{DD} = 5 V, f_{OUT} = 1 kHz			-73		dB
Signal to Noise and Distortion Ratio	SINAD	At T_A = 25 °C, Bandwidth = 20 kHz, V_{DD} = 5 V, f_{OUT} = 1 kHz			69.5		dB
AC Crosstalk		Digital, Internal Reference, Gain = 2			0.1		nV-s
		Analog, Internal Reference, Gain = 2			-0.3		nV-s
		DAC to DAC, Internal Reference, Gain = 2			1		nV-s
Digital Feedthrough		DAC Code = Midscale. f_{SCLK} = 1 MHz, SDO Disabled			0.15		nV-s
External Reference Input							
V_{REF}				1		V_{DD}	V
Reference Input Current		V_{REF} = 2.5 V, Gain = 1 / Gain = 2			150/300		µA
Reference Input Impedance		Gain = 1 / Gain = 2			16.7/8.3		kΩ
Reference Input Capacitance					5		pF
Internal Reference							
Reference Output Voltage		T_A = 25 °C		2.495	2.5	2.505	V
Reference Output Drift					5		ppm/°C
Output Impedance					0.03		Ω
Output Noise		0.1 Hz to 10 Hz			12		μV_{P-P}
Output Noise Density		10 kHz, $V_{REFLOAD}$ = 10 nF			280		$nV/\sqrt{Hz}$
Load Current					±20		mA
Load Regulation		Source and Sink			30		µV/mA
Line Regulation					50		µV/V
Digital Input							
Input High Voltage	V_{IH}		•	0.7 * V_{LOGIC} /2.4			V
Input Low Voltage	V_{IL}		•			0.3 * V_{LOGIC} /0.8	V
Input Current			•		±1		µA
Input Capacitance					3		pF
Digital Output							
Output High Voltage	V_{OH}	I_{LOAD} = +0.2 mA	•	V_{LOGIC} - 0.4			V
Output Low Voltage	V_{OL}	I_{LOAD} = -0.2 mA	•			0.4	V
Output Pin Capacitance					3		pF
Power Supply							
Analog Supply Voltage	V_{DD}		•	2.7		5.5	V
IO Supply Voltage	V_{LOGIC}		•	1.62		5.5	V
I_{DD} Supply Current	I_{DD}	Active mode. Internal Reference Enabled. Gain = 1. DAC Code = Full Scale. Outputs Unloaded. SPI Static			2.6		mA
		Active Mode. Internal Reference Disabled. Gain = 1. DAC Code = Full Scale. Outputs Unloaded. SPI Static			1.5		
		Power Down			20		µA
I_{LOGIC} Supply Current	I_{IO}				1		µA
Temperature Range							
Rated Performance		T_{MIN} to T_{MAX}		-40		+125	°C

Timing Index

The ●denotes the full temperature range for specified performance. Unless otherwise specified. T_A = 25 °C, V_{DD} = 2.7 V to 5.5 V.

Write Operation Timing Characteristics:

Parameters	Symbol		1.62 V ≤ V_{LOGIC} < 2.7 V		2.7 V ≤ V_{LOGIC} ≤ 5.5 V		Unit
			Min	Max	Min	Max	
SCLK Cycle Time	t_1	●	20		20		ns
SCLK High Level Time	t_2	●	8		8		ns
SCLK Low Level Time	t_3	●	8		8		ns
$\overline{SYNC}$ to SCLK Falling Edge Setup	t_4	●	15		12		ns
SDI Setup	t_5	●	4		4		ns
SDI Hold	t_6	●	3		3		ns
SCLK Falling Edge to $\overline{SYNC}$ Rising Edge	t_7	●	5		5		ns
$\overline{SYNC}$ High Time	t_8	●	15		15		ns
$\overline{SYNC}$ Rising Edge to $\overline{SYNC}$ Rising Edge (DAC Register Updates)	t_9	●	500		500		ns
$\overline{SYNC}$ Falling Edge to SCLK Falling Ignore	t_{10}	●	5		5		ns
$\overline{LDAC}$ Pulse Width Low	t_{11}	●	10		10		ns
$\overline{SYNC}$ Rising Edge to $\overline{LDAC}$ Rising Edge	t_{12}	●	25		25		ns
$\overline{SYNC}$ Rising Edge to $\overline{LDAC}$ Falling Edge	t_{13}	●	25		25		ns
$\overline{LDAC}$ Falling Edge to $\overline{SYNC}$ Rising Edge	t_{14}	●	500		500		ns
Minimum Pulse Width Low	t_{15}	●	10		10		ns
$\overline{RESET}$ Activation Time	t_{16}	●	100		100		ns

Note: DB15 to DB4 is used for DAC Code of ZJC2676-12(R).

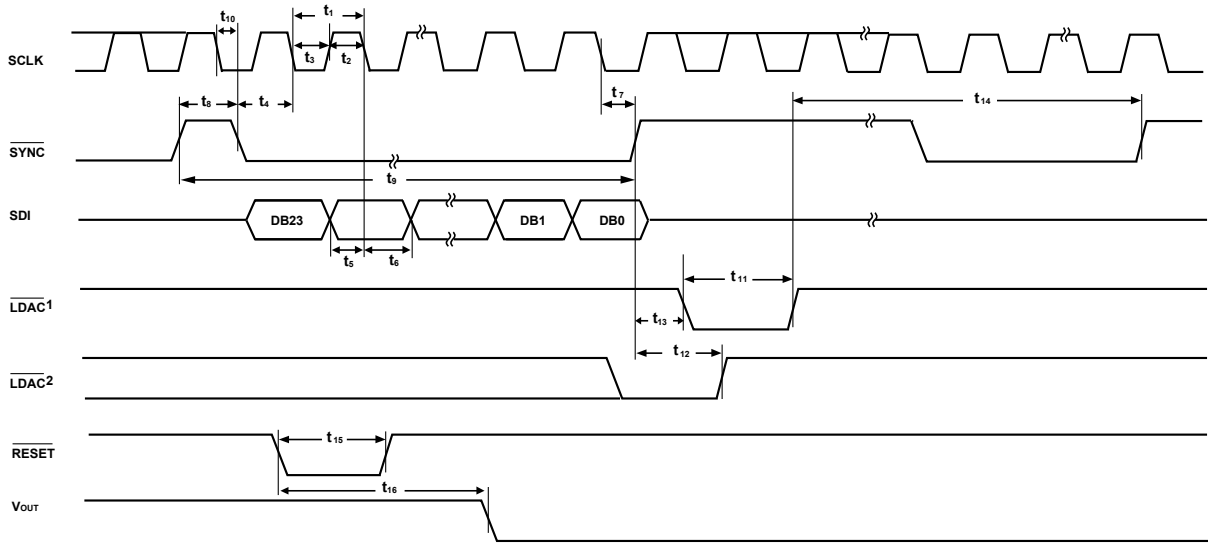

Figure 5. ZJC2676-16(R) Write Timing Diagram

1 $\overline{LDAC}^1$: Asynchronous update mode.

2 $\overline{LDAC}^2$: Synchronous update mode.

Daisy-chain and Readback Timing Characteristics:

Parameters	Symbol		1.62 V ≤ V_{LOGIC} < 2.7 V		2.7 V ≤ V_{LOGIC} ≤ 5.5 V		Unit
			Min	Max	Min	Max	
SCLK Cycle Time	t_1	●	130		120		ns
SCLK High Time	t_2	●	35		25		ns
SCLK Low Time	t_3	●	35		25		ns
$\overline{SYNC}$ to SCLK Falling Edge Setup	t_4	●	30		20		ns
SDI Setup	t_5	●	5		5		ns
SDI Hold	t_6	●	4		4		ns
SCLK Falling Edge to $\overline{SYNC}$ Rising Edge	t_7	●	10		10		ns
$\overline{SYNC}$ High Time	t_8	●	15		15		ns
SDO Data Valid from SCLK Rising Edge	t_9	●	5		5		ns
$\overline{SYNC}$ Rising Edge to SCLK Falling Edge	t_{10}	●	3		6		ns
$\overline{SYNC}$ Rising Edge to SDO Disable	t_{11}	●	5		4		ns

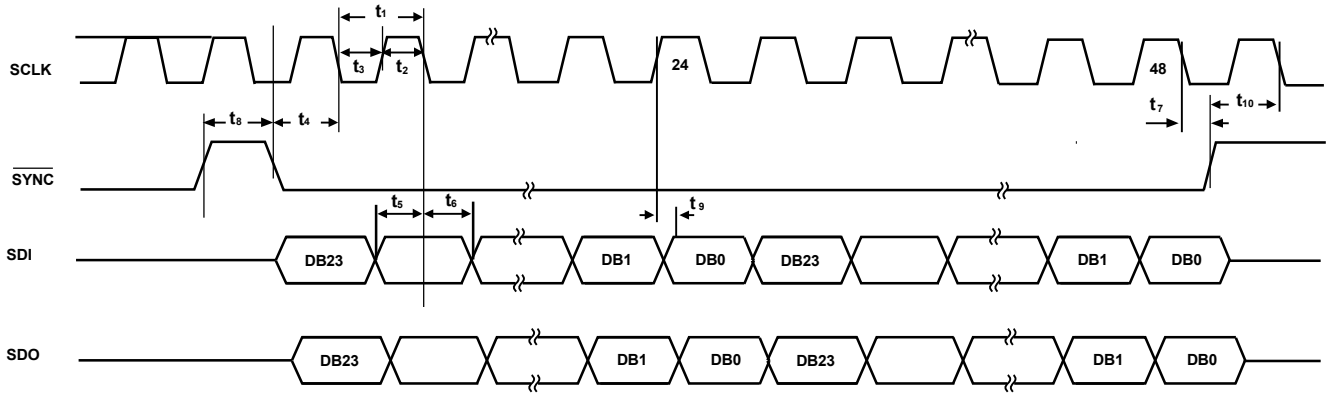

Figure 6. ZJC2676-16(R) Daisy Chain Timing Diagram

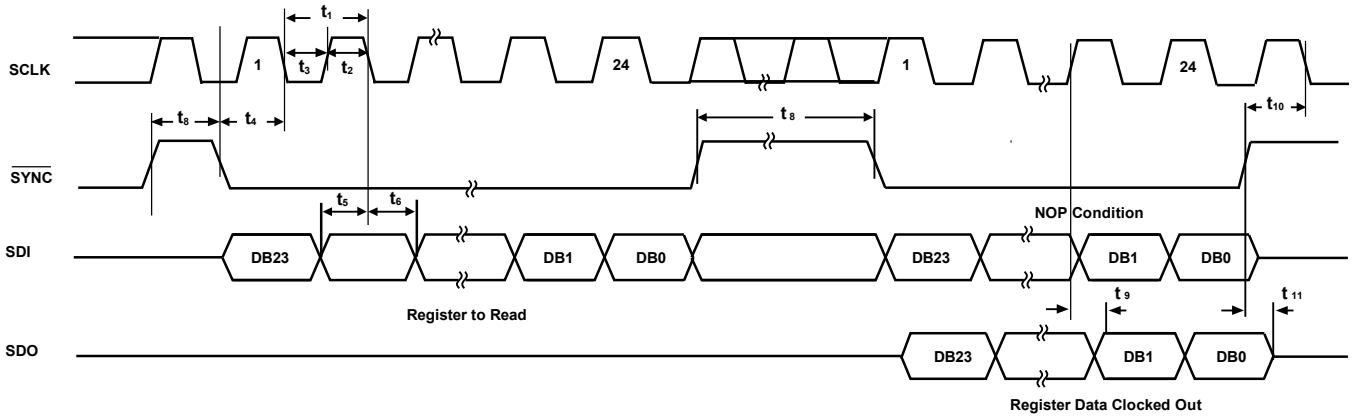

Figure 7. ZJC2676-16(R) Read Timing Diagram

Typical Performance Characteristics

Unless otherwise noted, V_{DD} = 5.0 V, V_{REF} = 2.5 V, T_A = 25 °C.

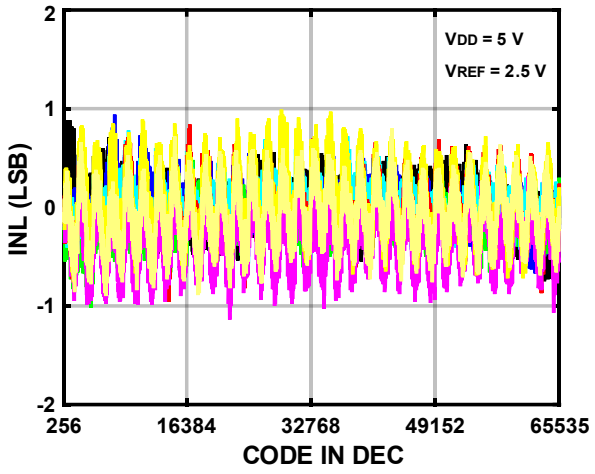

Figure 8. Integral Nonlinearity vs. Code-16 bits

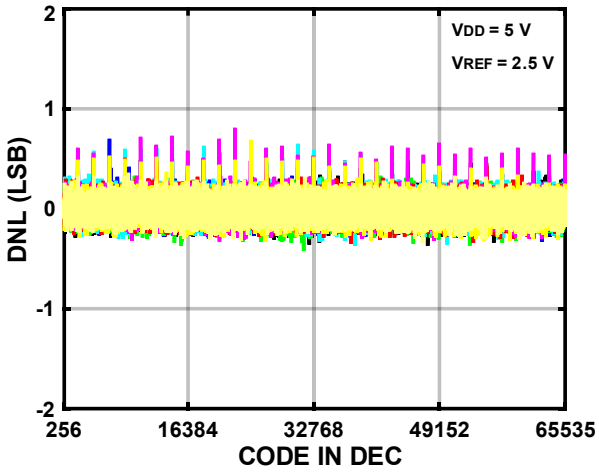

Figure 9. Differential Nonlinearity vs Code-16 bit

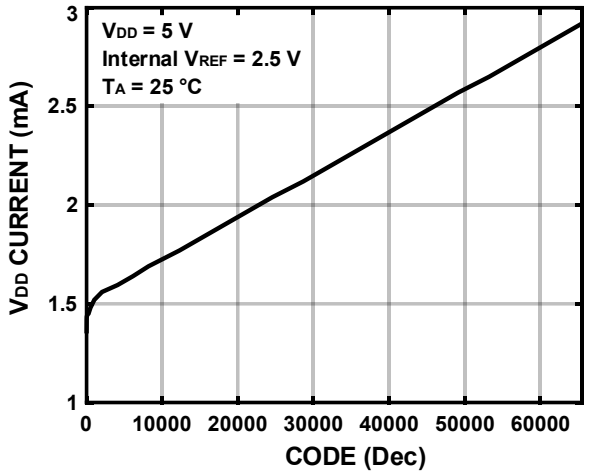

Figure 10. I_{DD} vs. Code

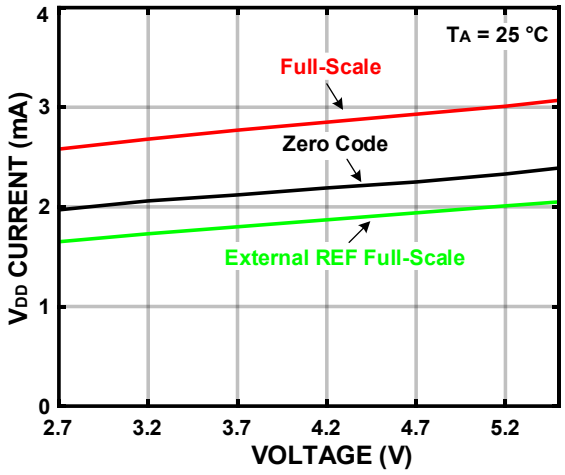

Figure 11. I_{DD} vs. V_{DD} Supply Voltage

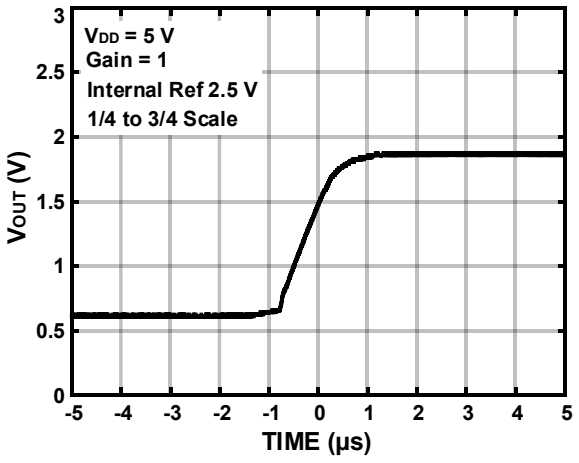

Figure 12. V_{OUT} Step Settling Time

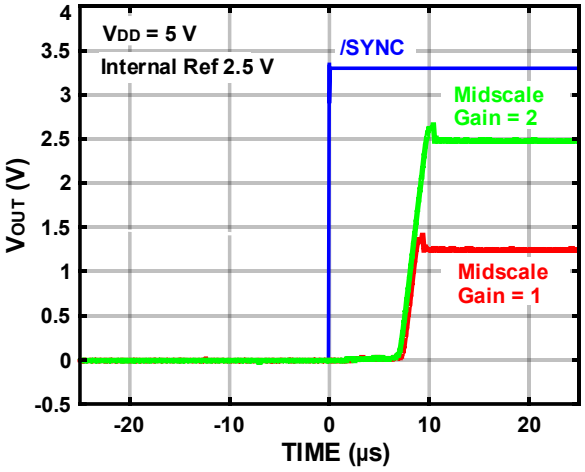

Figure 13. Exiting Power-down to Midscale

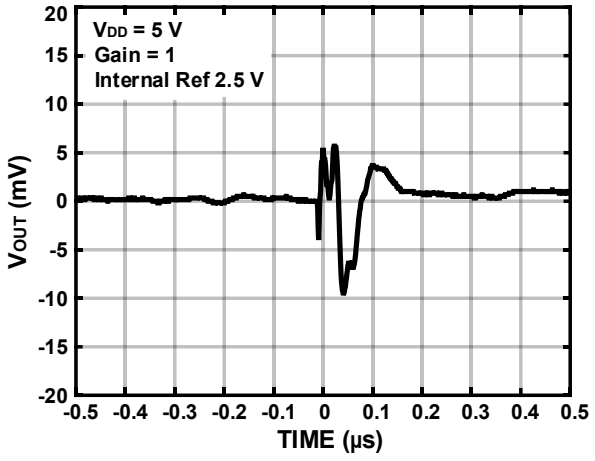

Figure 14. V_{OUT} Glitch

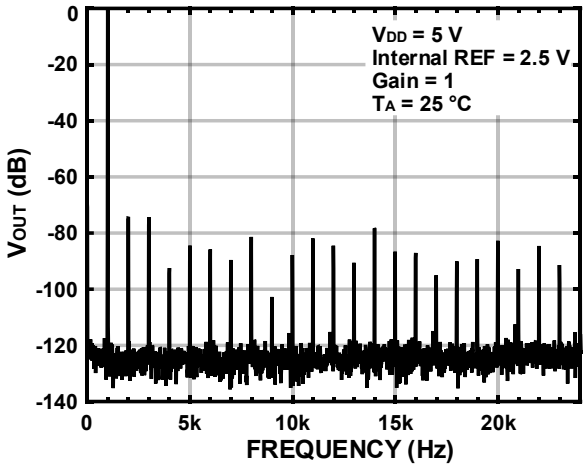

Figure 15. Harmonic Distortion vs Frequency

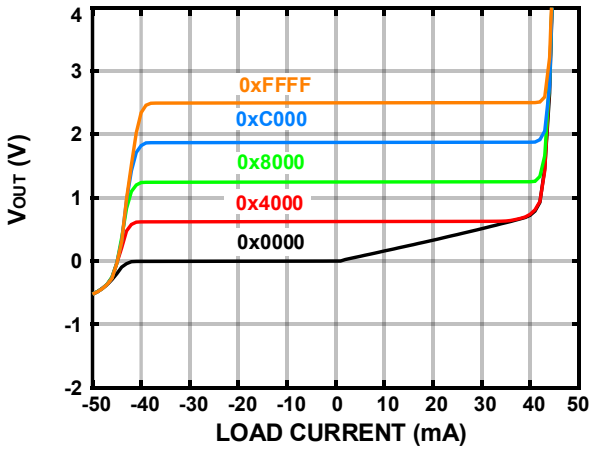

Figure 16. Source and Sink Capability With Gain = 1

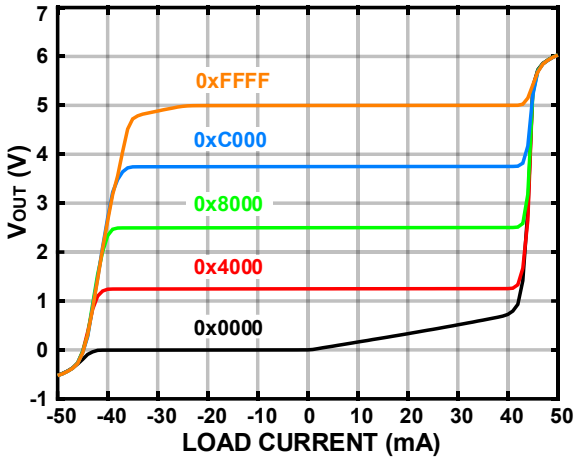

Figure 17. Source and Sink Capability With Gain = 2

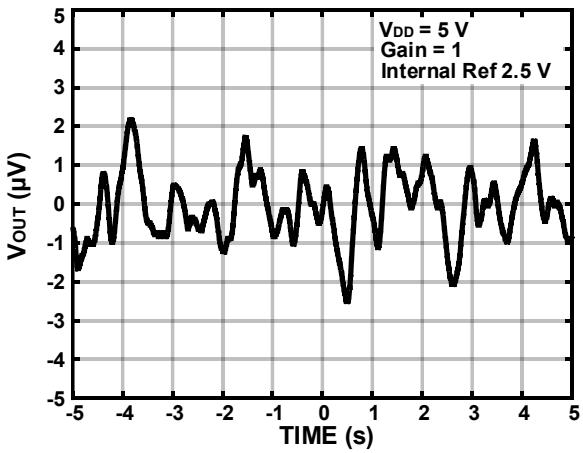

Figure 18. Output 0.1 to 10 Hz Noise

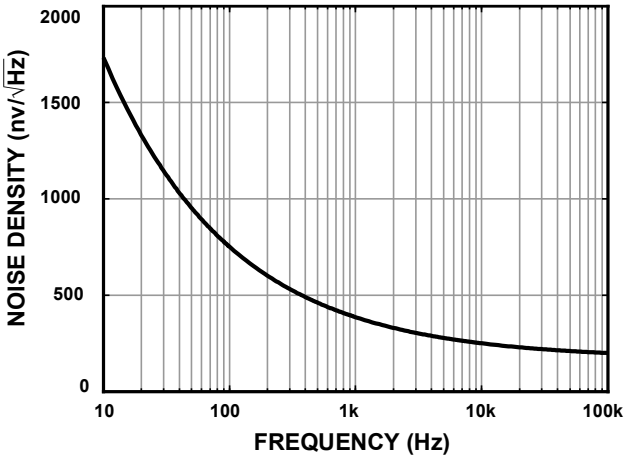

Figure 19. Output NSD (Internal Ref, Gain = 2, Midscale)

Theory of Operation

ZJC2676-16/12(R) is a pin-compatible family of eight-channel, buffered voltage-output digital-to-analog converters (DACs) with 16 or 12-bit resolution. It includes a 2.5 V internal reference and user selectable gain configuration output voltage 2.5 V (Gain = 1) or 5 V (Gain = 2). The device operates from a single 2.7 V to 5.5 V V_{DD} supply.

The ZJC2676-16/12(R) incorporates a power-on-reset circuit that powers up and maintains the DAC outputs at either zero scale or midscale.

Digital-to-analog Conversion

Each output channel in the ZJC2676-16/12(R) consists of a string resistor architecture followed by an output buffer amplifier.

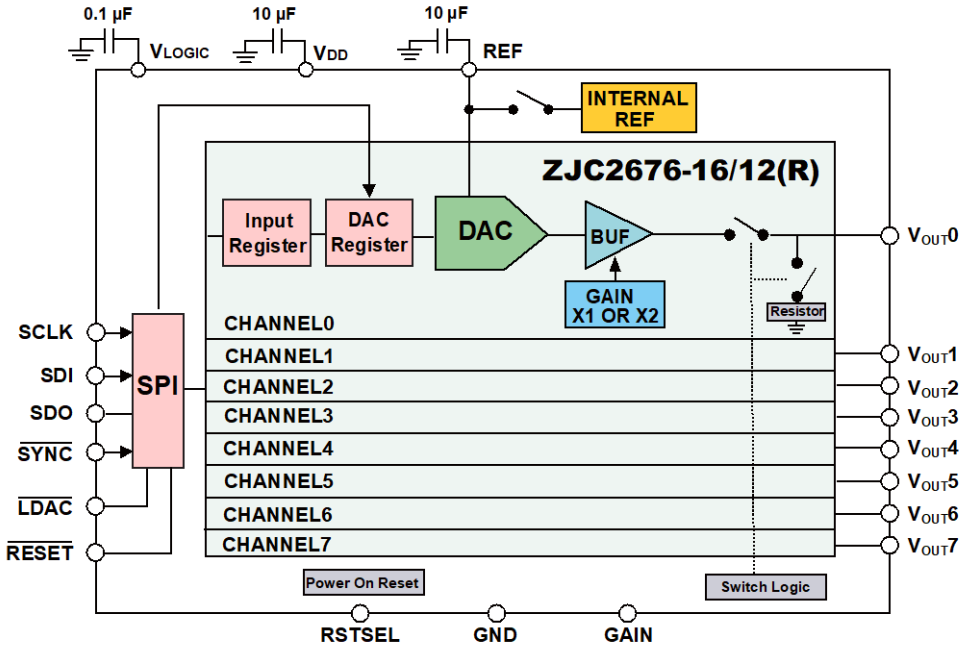

Figure 20. ZJC2676-16/12(R) Block Diagram

DAC Transfer Function

The output voltage is related to the reference level as shown in the following equation:

$$V_{\mathrm{OUT}} = \frac{CODE}{2^N} * V_{REF} * GAIN$$

Where:

CODE is the decimal data word loaded into the DAC register.

N is the resolution of the DAC.

V_{REF} is the DAC selected external or internal reference voltage.

GAIN = 1 (Amplifier gain setting DB2 = 0 or GAIN pin = low of TSSOP-20) or 2 (Amplifier gain setting DB2 = 1 or GAIN pin = high of TSSOP-20).

ZJC2676-16(R) digital code value and ideal output voltage: Amplifier gain setting DB2 = 1

DAC Latch Data	Analog Output (Reference Input V_{REF})
1111 1111 1111 1111	V_{REF} × (65535 / 65536) *2
1000 0000 0000 0000	V_{REF} × (32768 / 65536) * 2 = V_{REF}
0000 0000 0000 0001	V_{REF} × (1 / 65536) * 2
0000 0000 0000 0000	0 V

ZJC2676-16/12(R) digital code value and ideal output voltage: Amplifier gain setting DB2 = 0

DAC Latch Data	Analog Output (Reference Input V_{REF})
1111 1111 1111 1111	V_{REF}× (65535 / 65536)
1000 0000 0000 0000	V_{REF} × (32768/65536) = 1/2 * V_{REF}
0000 0000 0000 0001	V_{REF} × (1/65536)
0000 0000 0000 0000	0V

Internal Reference

The ZJC2676-16/12R includes a 2.5 V precision bandgap reference enabled by default. Operation from an external reference is supported by disabling the internal reference in the control register. The internal reference is externally available at the REF pin. A minimum 470 nF capacitor is recommended for decoupling and noise filtering.

Output Amplifiers

The ZJC2676-16/12(R) output buffer amplifier is capable of driving a load of 1 kΩ in parallel with 10 nF to GND. The full-scale output voltage for each channel is determined by the reference voltage and the output buffer gain for that channel.

Input Shift Register

The input shift register of ZJC2676-16/12(R) is 24 bits wide. Data is loaded MSB first (DB23), and the first four bits are the command bits, C3 to C0, followed by the 4-bit DAC address bits, A3 to A0, and finally, the 16-bit DAC code.

The DAC code comprises 16 or 12-bit input code, followed by 0 or four don't care bits (ZJC2676-12(R)). These data bits are transferred to the input register on the 24 falling edges of SCLK and are sampled on the rising edge of $\overline{\text{SYNC}}$.

Command Definitions:

Command				Description
C3	C2	C1	C0	
0	0	0	0	No operation
0	0	0	1	Write to DAC Input Register x where x = 1 to 8, depending on the DAC channel selected from the address bits in the table below.
0	0	1	0	Update DAC Register x (DB7 to DB0) and output ($\overline{\text{LDAC}}$ activated) with data of Input Register x.
0	0	1	1	Write to and update DAC Channel x output.
0	1	0	0	Power down/power up the DAC channel.
0	1	0	1	Hardware $\overline{\text{LDAC}}$ mask register.
0	1	1	0	Software reset (power-on reset).
0	1	1	1	Internal reference enable and gain register.
1	0	0	0	Set up the DCEN register (daisy-chain enable).
1	0	0	1	Set up the readback register (readback enable).

Command				Description
C3	C2	C1	C0	
1	0	1	0	Update all channels of the input register simultaneously with the input SDI data.
1	0	1	1	Update all channels of the DAC register and input register simultaneously with the input SDI data.
1	1	0	0	Reserved.
…	…	…	…	
1	1	1	1	No operation, for daisy-chain mode.

Address Commands:

Channel Address [3:0]				Selected Channel
A3	A2	A1	A0	
0	0	0	0	DAC0
0	0	0	1	DAC1
0	0	1	0	DAC2
0	0	1	1	DAC3
0	1	0	0	DAC4
0	1	0	1	DAC5
0	1	1	0	DAC6
0	1	1	1	DAC7

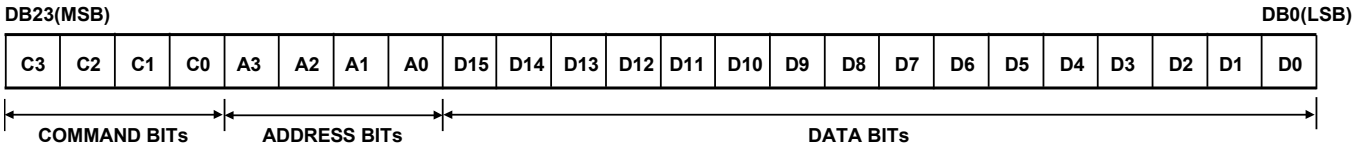

Figure 21. ZJC2676-16(R) Input Shift Register Content

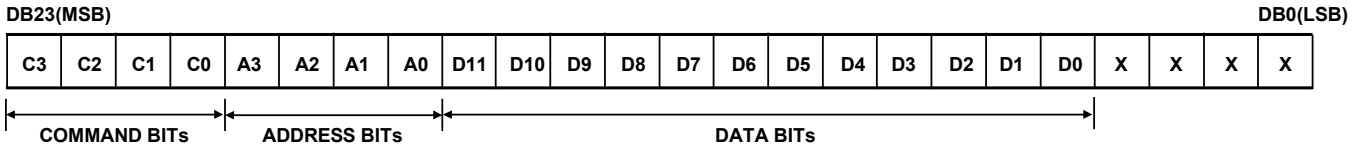

Figure 22. ZJC2676-12(R) Input Shift Register Content

Functions

Stand-alone Operation

A serial interface write or read frame can be started by asserting the $\overline{SYNC}$ pin low and ended by de-asserting the $\overline{SYNC}$ pin high. SDI data bits are clocked into a register on SCLK falling edges with 24 bits long. If $\overline{SYNC}$ is taken high at a clock before the 24th clock (less than 24 SCLK cycles), it is considered a invalid frame. If the access cycle contains more than the minimum clock edges, only the last 24 bits are used. When $\overline{SYNC}$ is high, the SCLK and SDI signals are blocked and the SDO pin is in a Hi-Z state.

Write to Input Register x (Dependent on $\overline{LDAC}$)

Command 0001 is used to write the target input register (not the DAC register) of each DAC individually. When $\overline{LDAC}$ is low, the input register is transparent to the DAC register and output updates, if not controlled by the $\overline{LDAC}$ mask register.

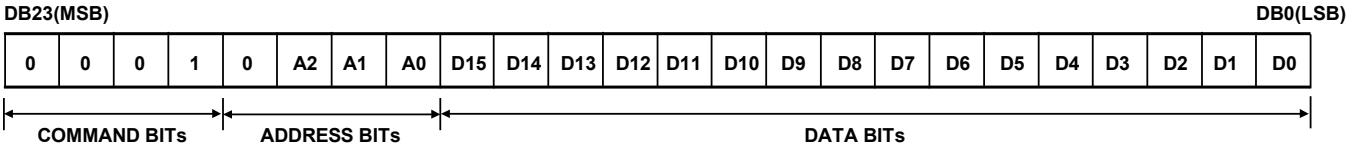

Figure 23. ZJC2676-16(R) Write Input Register

Update DAC Register x with Data of Input Register x

Command 0010 loads the DAC registers and outputs with the data of the input registers selected, and updates the DAC channel outputs directly. Data Bit D7 to D0 determine which DACs have data from the input register transferred to the DAC register. Setting a bit to 1 transfers data from the input register to the appropriate DAC register.

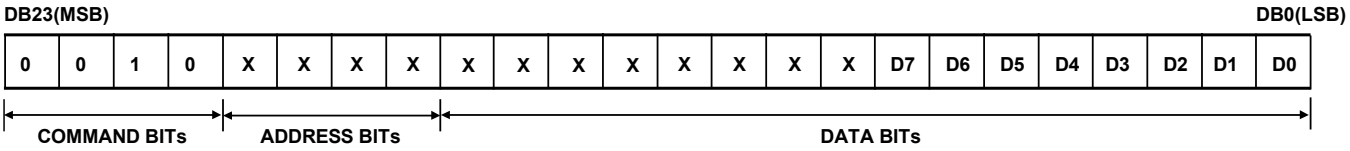

Figure 24. ZJC2676-16/12(R) Update DAC Register

Write to and Update DAC Channel x (Independent of $\overline{LDAC}$)

Command 0011 is used to write to the input registers and updates the DAC outputs directly. The address bits are used to select the DAC channel.

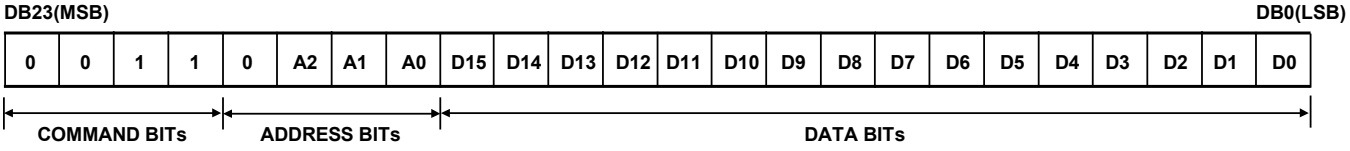

Figure 25. ZJC2676-16(R) Write Input Register and Update DAC Register Output

Daisy-chain Operation

The SDO pin can daisy-chain several DAC parts together and is enabled through a daisy-chain enable (DCEN) command. Command 1000 is reserved for this DCEN function. The daisy-chain mode is enabled by setting Bit DB0 in the DCEN register. The POR default setting is standalone mode, where DB0 = 0.

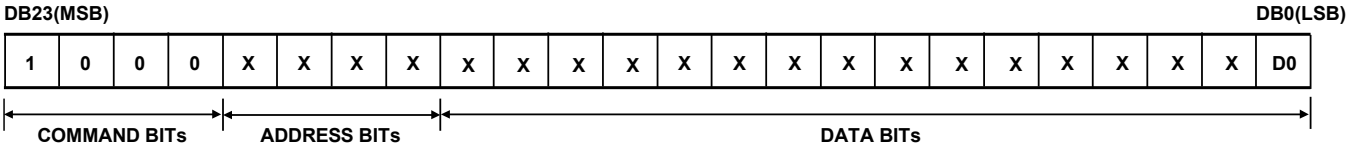

Figure 26. ZJC2676-16/12(R) Write DCEN Register

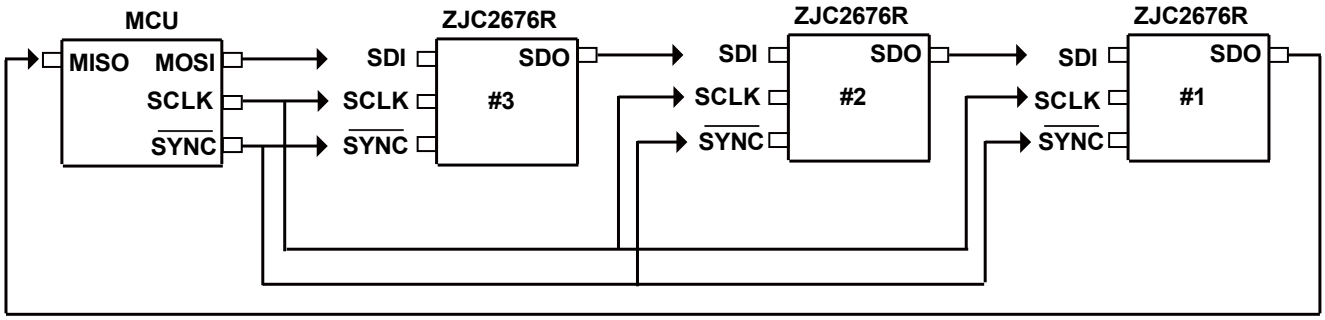

Figure 27. ZJC2676-16/12(R) Daisy-chain Connection

When $\overline{\text{SYNC}}$ is low, if more than 24 clock pulses are applied, the data outputs from the shift register on the SDO line. This data is clocked out on the rising edge of SCLK. Connect this SDO line to the SDI input on the next DAC to make a daisy-chain interface. Each DAC part in the chain requires 24 clock pulses. Therefore, the total number of clock cycles must equal to 24×N, where N is the total parts updated. If $\overline{\text{SYNC}}$ is taken high at a clock that is not a multiple of 24, it is considered a valid frame, and invalid data may be loaded to the DAC. When the data transfer to all parts is complete, $\overline{\text{SYNC}}$ goes high, which latches the input data in each part.

Readback Operation

Command 1001 is reserved for the readback function. With the address bits A3 to A0, users can select the DAC input register to read. During readback, only one input register can be selected. The following data bits are don't care bits. During the next SPI operation, the data of the addressed register appearing on the SDO output.

For example, to read back the DAC register for Channel 1:

1. Write 0 x 910000 to the ZJC2676-16/12(R) input register. This configures the device into read mode with the DAC register Channel 1 selected. All data bits, DB15 to DB0, are don't care bits.

2. Follow this with a second SPI operation, a no operation (NOP) condition, 0 x 000000 or 0 x F00000 when in daisy-chain mode. During this operation, the target data is clocked out on the SDO line. DB19 to DB16 contain register address, and the last 16 bits contain the DB15 to DB0 DAC register contents.

Power-down Operation

The ZJC2676-16/12(R) contains two power-down modes. Command 0100 is used for the power-down function. Any or all DACs (DAC 0 to DAC 7) can be powered down to the selected mode by the corresponding bits.

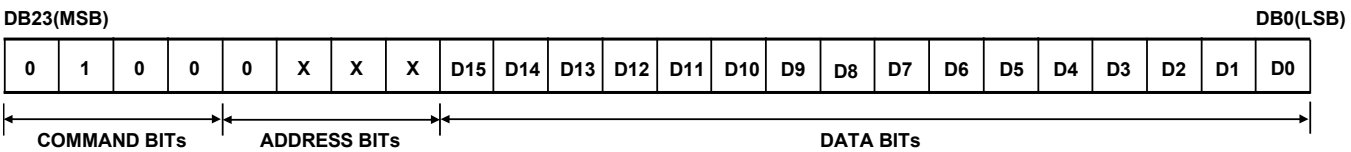

Figure 28. ZJC2676-16/12(R) Write Power down/Power up Register

Operating Mode	PD1	PD0
Normal Operation	0	0
Power-Down Modes		
1 kΩ to GND	0	1
Tristate	1	1

When both Bit PD1 and Bit PD0 in the input shift register are set to 0, the device works normally with a typical power consumption of 1.5 mA at 5 V. However, for the two power-down modes, the supply current typically falls to 20 μA. There are two different power-down options. The output is either connected internally to GND through a 1 kΩ resistor or it is left open circuited (tristate).

The bias generator, output amplifier, resistor string, and other associated linear circuitry shut down when power-down mode is activated. However, the contents of the DAC register are unaffected when in power-down. The DAC register updates while the device is in power-down mode. The time required to exit power-down is typically 12 μs for V_{DD} = 5 V.

24-Bit Input Shift Register of Power-Down/Power-Up Operation:

			DAC7	DAC6	DAC5	DAC4	DAC3	DAC2	DAC1	DAC0
[D23:D20]	[D19]	[D18:D16]	[D15:D14]	[D13:D12]	[D11:D10]	[D9:D8]	[D7:D6]	[D5:D4]	[D3:D2]	[D1:D0]
0100	0	XXX	[PD1:PD0]	[PD1:PD0]	[PD1:PD0]	[PD1:PD0]	[PD1:PD0]	[PD1:PD0]	[PD1:PD0]	[PD1:PD0]

Load DAC (Hardware $\overline{\text{LDAC}}$ Pin)

The ZJC2676-16/12(R) has double buffered interface consisting of two groups of registers: input registers and DAC registers. The user can write to any combination of the input registers. Updates to the DAC register are controlled by the $\overline{\text{LDAC}}$ pin.

For instantaneous DAC updating, $\overline{\text{LDAC}}$ should be held low while data is clocked into the input register using Command 0001. Both the addressed input register and the DAC register are updated on the rising edge of $\overline{\text{LDAC}}$ and the output changes.

For deferred DAC updating, $\overline{\text{LDAC}}$ is held high while data is clocked into the input register using Command 0001. All DAC outputs can be asynchronously updated by taking $\overline{\text{LDAC}}$ low after $\overline{\text{SYNC}}$ is taken high. The output updates on the falling edge of $\overline{\text{LDAC}}$.

$\overline{\text{LDAC}}$ Mask Register

Writing to the DAC using Command 0101, address bits are ignored, loads the 8-bit $\overline{\text{LDAC}}$ register (DB7 to DB0). The default bit for each channel is 0, and the $\overline{\text{LDAC}}$ pin works normally. Setting the bits to 1 forces the DAC channels to ignore the state of the $\overline{\text{LDAC}}$ pin. Clearing the $\overline{\text{LDAC}}$ bits (DB7to DB0) to 0 for a DAC channel means that this channel update is controlled by the $\overline{\text{LDAC}}$ pin.

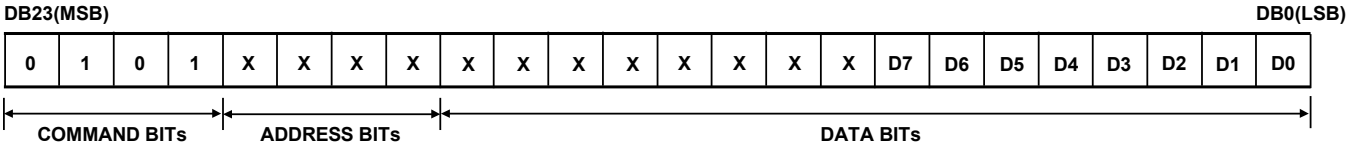

Figure 29. ZJC2676-16/12(R) Write $\overline{\text{LDAC}}$ Mask Register

$\overline{\text{LDAC}}$ Register Definition:

Load $\overline{\text{LDAC}}$ Register		
$\overline{\text{LDAC}}$ Register [DB7:DB0]	$\overline{\text{LDAC}}$ pin	$\overline{\text{LDAC}}$ Register
00000000	0 or 1	Determined by the $\overline{\text{LDAC}}$ pin.
11111111	Don't care	DAC channels update and ignore the $\overline{\text{LDAC}}$ pin (for Command 0001 to update DAC output directly).

$\overline{\text{LDAC}}$ Register Definition:

Command	Description	$\overline{\text{LDAC}}$ Pin State	Input Register Contents	DAC Register Contents
0001	Write to Input Register x (dependent on $\overline{\text{LDAC}}$)	V_{LOGIC}	Data update	No update
		GND	Data update	Data update
0010	Update DAC Register x with contents of Input Register x	V_{LOGIC}	No update	Updated with input register contents
		GND	No update	Updated with input register contents
0011	Write to and update DAC Channel x	V_{LOGIC}	Data update	Data update
		GND	Data update	Data update

Hardware Reset ($\overline{\text{RESET}}$)

The $\overline{\text{RESET}}$ pin is an active low reset, and can make the outputs cleared to either zero scale or midscale. The clear code value is user selectable via the RSTSEL pin. After power supply established, it is necessary to keep the $\overline{\text{RESET}}$ pin for a minimum low time to complete the operation. If the $\overline{\text{RESET}}$ pin is pulled low at power-up, the device does not initialize correctly until the pin is released. When the $\overline{\text{RESET}}$ signal is returned high, the output remains the cleared value until a new value is programmed. While the $\overline{\text{RESET}}$ pin is low, the outputs cannot be updated with a new value.

Reset Select Pin (RSTSEL)

The ZJC2676-16/12(R) contains a power-on reset circuit. By connecting the RSTSEL pin low, the output powers up to zero scale; By connecting the RSTSEL pin high, $V_{OUT}x$ power up to midscale. The output remains at this level until a valid write sequence is made to the DAC. The RSTSEL pin is only available on the TSSOP-20. The ZJC2676-16/12(R) in QFN-20 outputs to 0 V after power up.

Software Reset

Command 0110 is designated for a software reset function. The DAC address bits must be set to 0 x 0 and the data bits set to 0 x 1234 for the software reset command to execute.

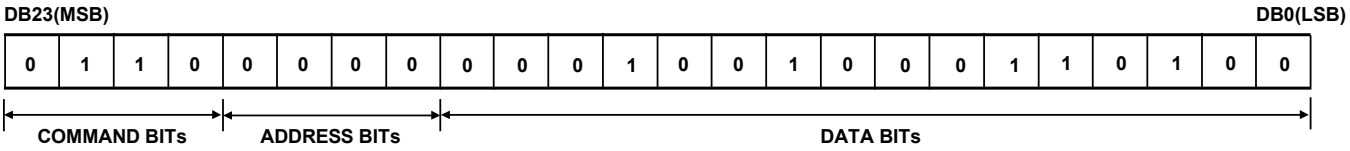

Figure 30. ZJC2676-16/12(R) Write Input Register and Update DAC Register Output

Amplifier Gain Selection

The output amplifier gain setting for the QFN-20 is determined by the state of the DB2 bit in the internal reference and gain setup register, while that for the TSSOP-20 is determined by the GAIN pin.

Internal Reference Setup

The on-chip reference is on by default. Command 0111 is reserved for setting up the internal reference and the gain setting (QFN-20 only).

Internal Reference and Gain Setup Register:

Bit	Description
DB2	Amplifier Gain Setting DB2 = 0: Amplifier Gain = 1 (default) DB2 = 1: Amplifier Gain = 2
DB0	Reference Disable DB0 = 0: Internal Reference Enabled (default) DB0 = 1: Internal Reference Disabled

Outline Dimensions

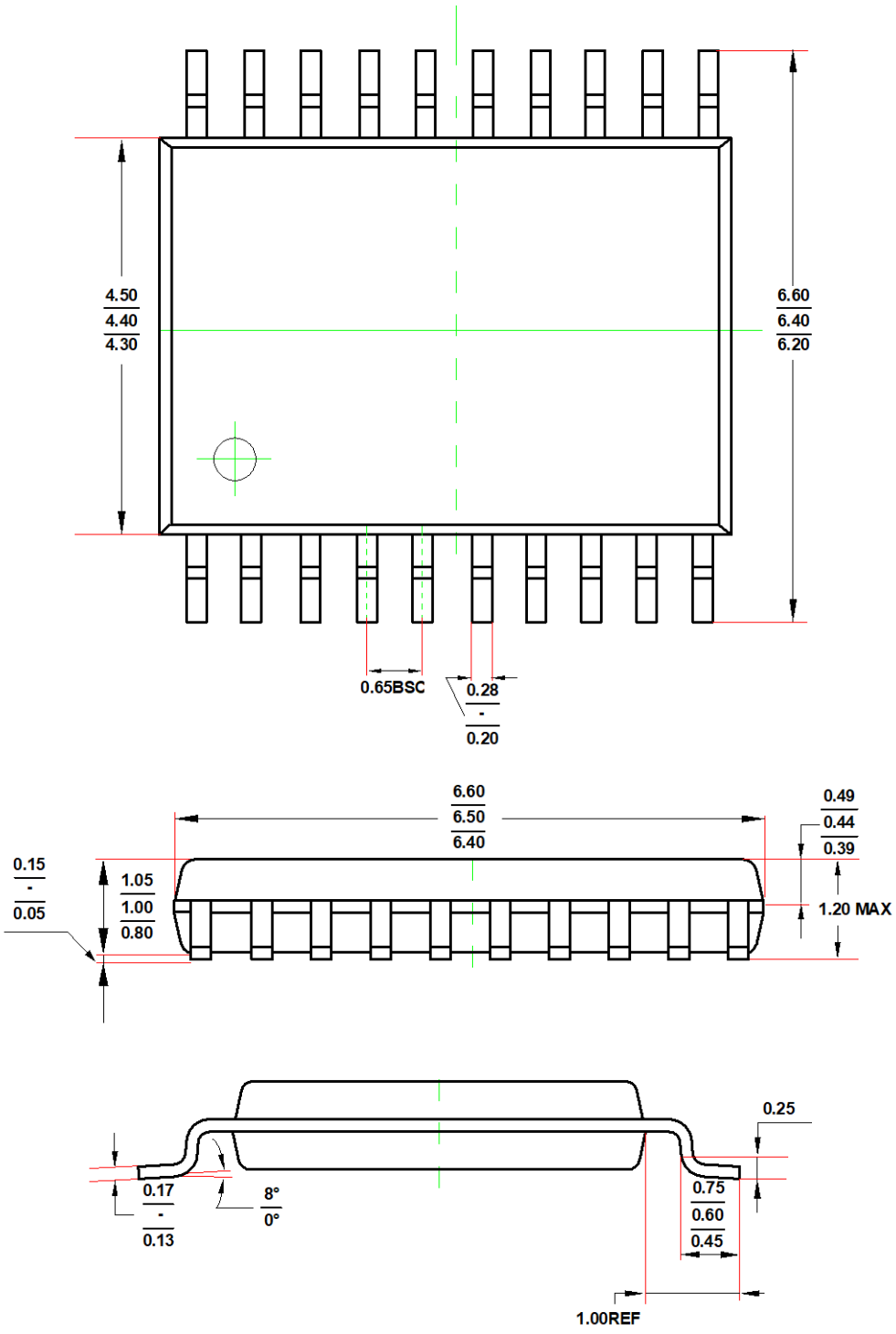

Figure 31. 20-Lead TSSOP Package Dimensions shown in millimeter

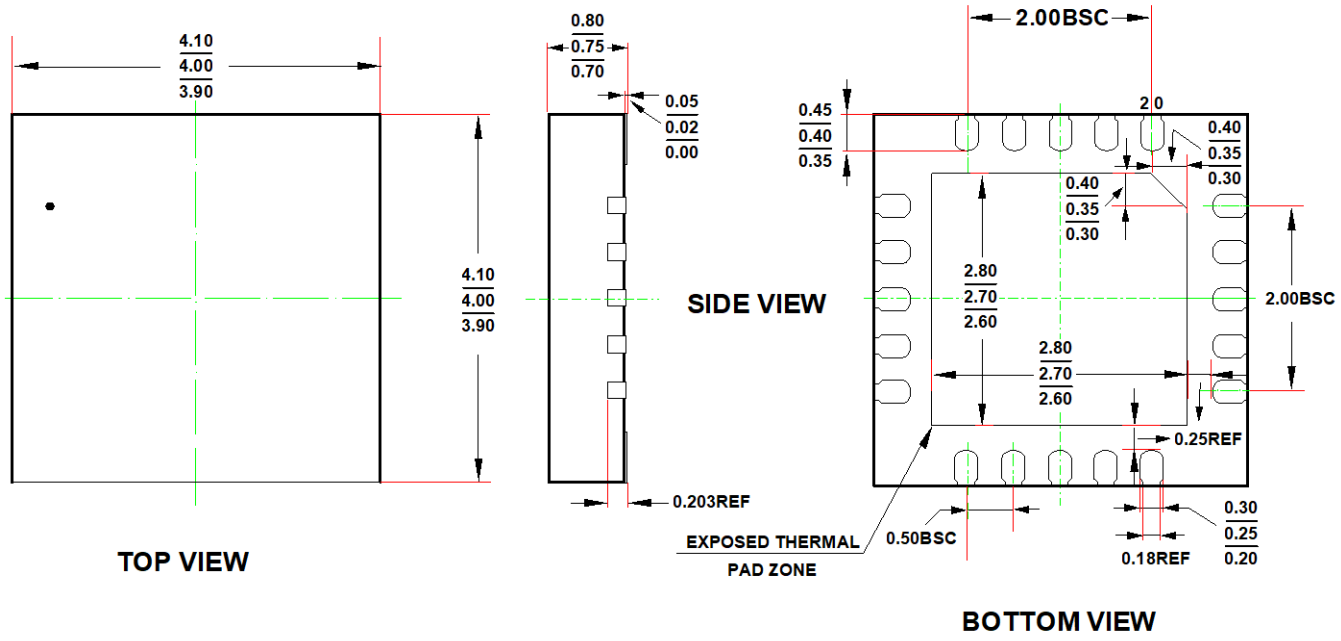

Figure 32. 20-Lead QFN (4x4 mm) Package Dimensions shown in millimeter

Ordering Guide

Model	Orderable Device	Resolution(bit)	Package	Silk Screen	Temperature Range(°C)	External Package
ZJC2676R	ZJC2676-16RATPBR	16	QFN-20	2676RP	-40 to +125	13” Reel
	ZJC2676-16RAUPBT		TSSOP-20			Tube
	ZJC2676-16RAUPBR					13” Reel
	ZJC2676-12RATPBR	12	QFN-20	2676RL		13” Reel
	ZJC2676-12RAUPBT		TSSOP-20			Tube
	ZJC2676-12RAUPBR					13” Reel
ZJC2676	ZJC2676-16ATPBR	16	QFN-20	2676-P		13” Reel
	ZJC2676-16AUPBT		TSSOP-20			Tube
	ZJC2676-16AUPBR					13” Reel

Product Order Model

ZJXXXXX X X X X X Q1

- Q1: Automotive Grade
- External Package: T = Tube; R = Reel
- Temperature Range: A = -40 °C to 125 °C Automotive Grade 1, B = -40 °C to 125 °C; E = -40 °C to 85 °C
- Number of Pins: R = 3; K =5; T = 6, A = 8; B = 10; D = 14; E = 16; P = 20
- Package Type: S = SOIC; U = MSOP, TSSOP, SOT; T = DFN, QFN; X = SC70; W = WLCSP; Z = TSOT23; L = LS
- Grade: B grade is better than A grade
- Base: R = Voltage reference; A = Amplifier; C = Data Converter; G = Switches and Multiplexers; M = Others

Related Parts

Part Number	Description	Comments
ADC		
ZJC2020	20-bit 350 kSPS SAR ADC	Fully differential input, SINAD 101.4 dB, THD -118 dB
ZJC2000/2010	18-bit 400 kSPS/200 kSPS SAR ADC	Fully differential input, SINAD 99.3 dB, THD -113 dB
ZJC2001/2011	16-bit 500 kSPS/250 kSPS SAR ADC	Fully differential input, SINAD 95.3 dB, THD -113 dB
ZJC2002/2012 ZJC2003/2013	16-bit 500 kSPS/250 kSPS SAR ADC	Pseudo-differential unipolar input, SINAD 91.7 dB, THD -105 dB Pseudo-differential bipolar input, SINAD 91.7 dB, THD -105 dB
ZJC2004/2014 ZJC2005/2015	18-bit 400 kSPS/200 kSPS SAR ADC	Pseudo-differential unipolar input, SINAD 94.2 dB, THD -105 dB Pseudo-differential bipolar input, SINAD 94.2 dB, THD -105 dB
ZJC2007/2017 ZJC2008/2018	14-bit 600 kSPS/300 kSPS SAR ADC	Pseudo-differential unipolar input, SINAD 85 dB, THD -105 dB Pseudo-differential bipolar input, SINAD 85 dB, THD -105 dB
ZJC2100/1-18 ZJC2100/1-16	18-bit 400 kSPS/200 kSPS 4-ch differential SAR ADC, SINAD 99.3 dB, THD -113 dB 16-bit 500 kSPS/250 kSPS 4-ch differential SAR ADC, SINAD 95.3 dB, THD -113 dB	
ZJC2102/3-18 ZJC2102/3-16 ZJC2102/3-14	18-bit 400 kSPS/200 kSPS 8-ch pseudo-differential SAR ADC, SINAD 94.2 dB, THD -105 dB 16-bit 500 kSPS/250 kSPS 8-ch pseudo-differential SAR ADC, SINAD 91.7 dB, THD -105 dB 14-bit 600 kSPS/300 kSPS 8-ch pseudo-differential SAR ADC, SINAD 85 dB, THD -105 dB	
ZJC2104/5-18 ZJC2104/5-16	18-bit 400 kSPS/200 kSPS 4-ch pseudo-differential SAR ADC, SINAD 94.2 dB, THD -105 dB 16-bit 500 kSPS/250 kSPS 4-ch pseudo-differential SAR ADC, SINAD 91.7 dB, THD -105 dB	
DAC		
ZJC2541-18/16/14 ZJC2543-18/16/14	18/16/14-bit 1 MSPS single channel DAC with unipolar output	Power on reset to 0 V (ZJC2541) or V_{REF}/2 (ZJC2543), 1 nV-S glitch, SOIC-8, MSOP-10/8, DFN-10 packages
ZJC2542-18/16/14 ZJC2544-18/16/14	18/16/14-bit 1 MSPS single channel DAC with bipolar output	Power on reset to 0 V (ZJC2542) or V_{REF}/2 (ZJC2544), 1 nV-S glitch, SOIC-14, TSSOP-16, QFN-16 packages
Amplifier		
ZJA3000-1/2/4 ZJO2177-1/2/4	Single/Dual/Quad 36 V low bias current precision Op Amps	3 MHz, 35 µV max Vos, 0.5 µV/°C max TCVos, 25 pA max Ibias, 1 mA/ch, input to V- (ZJA3000 only), RRO, 4.5 V to 36 V
ZJA3018-2 ZJA3008-2	OVP ±75 V, 36 V, Low Power, High Precision Op Amp 36 V, Low Power, High Precision Op Amp	1.3 MHz, 10 µV max Vos, 0.5 µV/°C max TCVos, 25 pA max Ibias, 0.5 mA/ch, OVP ±75 V (ZJA3018 only), RRO, 4.5 V to 36 V
ZJA3512-2	Dual 36 V 7 MHz precision JFET Op Amps	7 MHz, 35 V/µS, 50 µV max Vos, 1 µV/°C max TCVos, 2 mA/ch, RRO, 9 V to 36 V
ZJA3216/06/02-1/2	Precision 20/10/5 MHz CMOS RRIO Op Amps	20/10/5 MHz, RRIO, 30 µV max Vos, 1 µV/°C max TCVos, 0.6 pA Ib, 2.7 V to 5.5 V
ZJA3600/1	36 V ultra-high precision in-amp	CMRR 105 dB min (G = 1), 25 pA max Ib, 25 µV max Vosi, ±2.4 V to ±18 V, -40 °C to 125 °C
ZJA3611, ZJA3609	36 V precision wider bandwidth precision in-amp (G ≥ 10)	CMRR 120 dB min (G = 10), 25 pA max Ibias, 25 µV max Vosi, 1.2 MHz BW (G = 10)
ZJA3676/7 ZJA3678/9	Low power, G=1 Single/Dual 36 V difference amplifier Low power, G=0.5/2 Single/Dual 36 V difference amplifier	Input protection to ±65 V, CMRR 104 dB min (G = 1), Vos 100 µV max, gain error 15 ppm max, 500 kHz BW (G = 1), 330 µA/channel, 2.7 V to 36 V
ZJA3669	High Common-Mode Voltage Difference Amplifier	±270 V CMV, 2.5 kV ESD, 96 dB min CMRR, 450 kHz BW, 4 V to 36 V, SOIC-8
ZJA3100	15 V precision fully differential amplifier	145 MHz, 447 V/µS, 50 nS to 16-bit, 50 µV max Vos, 4.6 mA Iq, SOIC/MSOP-8, QFN-16
ZJA3236/26/22-2	Low-cost 20/10/5 MHz CMOS RRIO Op Amps	20/10/5 MHz, RRIO, 2 mV max Vos, 6 µV/°C max TCVos, 0.6 pA Ib, 2.7 V to 5.5 V
ZJA3622/8	36 V low-cost precision in-amp	0.5 nA max Ibias, 125 µV max Vosi, 625 kHz BW (G = 10), 3.3 mA Iq, ±2.4 V to ±18 V
Voltage Reference		
ZJR1004	40 V supply precision voltage reference	V_{OUT} = 2.048/2.5/3/3.3/4.096/5/10 V, 5 ppm/°C max drift -40 °C to 125 °C
ZJR1001/2 ZJR1003	5.5 V low power voltage reference (ZJR1001 with noise filter option)	V_{OUT} = 1.2/1.25/1.8/2.048/2.5/3/3.3/4.096/5 V, 5 ppm/°C max drift -40 °C to 125 °C, ±0.05% initial error, 130 µA, ZJR1001/2 in SOT23-6, ZJR1003 in SOIC/MSOP-8
Switches and Multiplexers		
ZJG4438/4439	36 V fault protection 8:1/dual 4:1 multiplexer	Protection to ±50 V power on & off, latch-up immune, Ron 270 Ω, 14.8 pC, t_{ON} 166 nS
ZJG4428/4429	36 V 8:1/dual 4:1 multiplexer	Latch-up immune, Ron 270 Ω, 14.8 pC charge injection, t_{ON} 166 nS
ZJG4408/4409	44 V, 8:1/dual 4:1 multiplexer	Latch-up roof, Ron 10.2 Ω, 180 pC charge injection, t_{ON} 155 nS
Quad Matching Resistor		
ZJM5400	±75 V precision match resistors	Mismatch < 100 ppm, 10k:10k:10k:10k, 100k:100k:100k:100k, 100k:10k:10k:100k, 1k:1k:1k:1k 1M:1M:1M:1M, 5k:1k:1k:5k, 5k:1.25k:1.25k:5k, 9k:1k:1k:9k, ESD: 3.5 kV