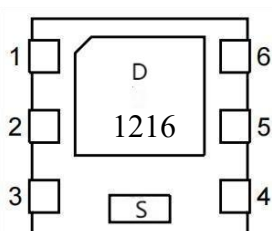


**Features**

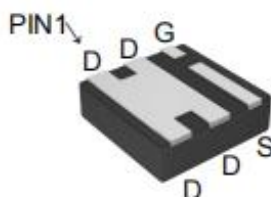
- Super Low Gate Charge
- Green Device Available
- Excellent Cdv/dt effect decline
- Advanced high cell density Trench technology

Bvdss**-19V****Rdson****12.4mΩ****ID****-16A****Application**

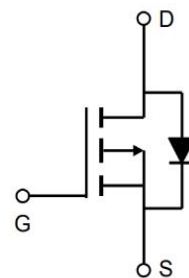
- PWM applications
- Load Switch
- Power management

RoHS**Package**

Marking and pin assignment



DFN2x2-6L top view



Schematic diagram

Package Marking and Ordering Information

Device Marking	Device	Device Package	Quantity
1216	HL1216M	DFN2X2-6L	3000

Absolute Maximum Ratings ($T_C=25^{\circ}\text{C}$ unless otherwise specified)

Parameter	Symbol	Rating	Unit
Drain-Source Voltage	V_{DS}	-19	V
Gate-Source Voltage	V_{GS}	± 12	V
Continuous Drain Current, $V_{GS} @ -4.5V^1$	$ID@T_C=25^{\circ}\text{C}$	-16	A
	$ID@T_C=70^{\circ}\text{C}$	-8.8	A
Pulsed Drain Current ²	I_{DM}	-40	A
Single Pulse Avalanche Energy	E_{AS}	-	mJ
Avalanche Current	I_{AS}	-	A
Total Power Dissipation ³	P_D	2.1	W
Storage Temperature Range	T_{STG}	-55 ~ 150	$^{\circ}\text{C}$
Operating Junction Temperature Range	T_J	-55 ~ 150	$^{\circ}\text{C}$



Thermal Resistance Ratings

Parameter	Symbol	Value	Unit
Thermal Resistance Junction-Ambient ¹	$R_{\theta JA}$	65	°C/W
Thermal Resistance Junction-Case ¹	$R_{\theta JC}$	80	°C/W

Ordering Information

Ordering Number	Package	Pin Assignment			Packing
Halogen Free		G	D	S	
HL1216M	DFN2X2-6L	3	1,2,5,6	4	Tape Reel

Electrical Characteristics ($T_J=25^{\circ}\text{C}$ unless otherwise noted)

Parameter	Symbol	Test Conditions	Min	Typ	Max	Units
Drain-Source Breakdown Voltage	$V_{(BR)DSS}$	$V_{GS}=0V, I_D=-250\mu A$	-19	-	-	V
Zero Gate Voltage Drain Current	I_{DSS}	$V_{DS}=-12V, V_{GS}=0V$	-	-	-1	μA
Gate-body Leakage Current	I_{GSS}	$V_{GS}=\pm 12V, V_{DS}=0V$	-	-	± 100	nA
Gate-Threshold Voltage	$V_{GS(th)}$	$V_{GS}=V_{DS}, I_D=-250\mu A$	-0.4	-0.7	-1	V
Static Drain-Source On-Resistance ²	$R_{DS(on)}$	$V_{GS}=-4.5V, I_D=-1A$	-	12.4	16	m Ω
		$V_{GS}=-2.5V, I_D=-1A$	-	16.4	21	
Input Capacitance	C_{iss}	$V_{DS}=-10V, V_{GS}=0V, f=1MHz$	-	1411	-	pF
Output Capacitance	C_{oss}		-	322	-	
Reverse Transfer Capacitance	C_{rss}		-	293	-	
Total Gate Charge	Q_g	$V_{DS}=-10V, I_D=-8A, V_{GS}=-4.5V$	-	20	-	nC
Gate Source Charge	Q_{gs}		-	6	-	
Gate Drain("Miller")Charge	Q_{gd}		-	8	-	
Turn-On Delay Time	$t_{d(on)}$	$V_{DD}=-10V, I_D=-8A, R_G=3.3\Omega, V_{GS}=-4.5V$	-	14	-	ns
Turn-On Rise Time	t_r		-	40	-	
Turn-Off Delay Time	$t_{d(off)}$		-	32	-	
Turn-Off Fall Time	t_f		-	10	-	
Drain to Source Diode Forward Voltage	V_{SD}	$V_{GS}=0V, I_S=-1A$	-	-	-1.2	V
Continuous Source Current ^{1,4}	I_S	$V_G=V_D=0V, \text{Force Current}$	-	-	-16	A
Pulsed Source Current ^{2,4}	I_{SM}		-	-	-40	A

Note : 1.The data tested by surface mounted on a 1 inch² FR-4 board with 2OZ copper.

2.The data tested by pulsed , pulse width $\leq 300\mu s$, duty cycle $\leq 2\%$.

3.The power dissipation is limited by 150°C junction temperature.

4.The data is theoretically the same as I_D and I_{DM} , in real applications , should be limited by total power dissipation.



Typical Performance Characteristics

Figure 1: Output Characteristics

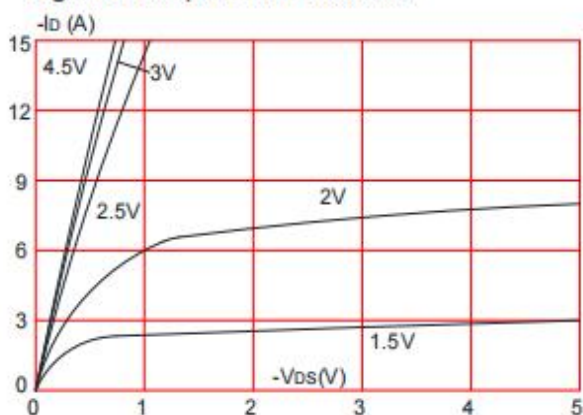


Figure 2: Typical Transfer Characteristics

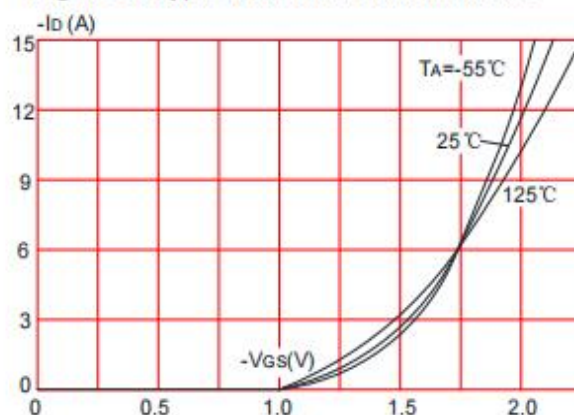


Figure 3: On-resistance vs. Drain Current

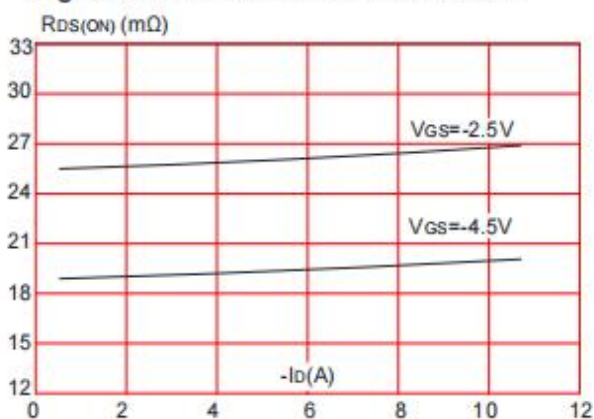


Figure 4: Body Diode Characteristics

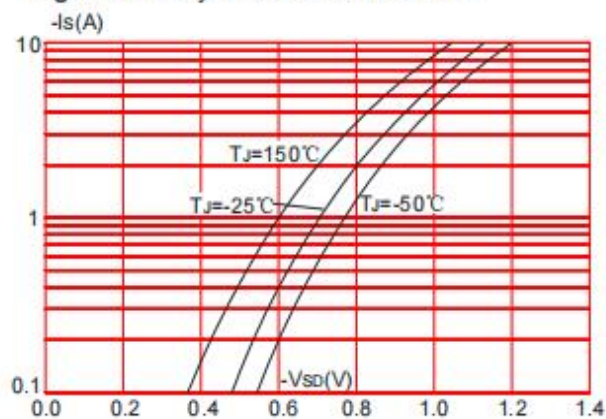


Figure 5: Gate Charge Characteristics

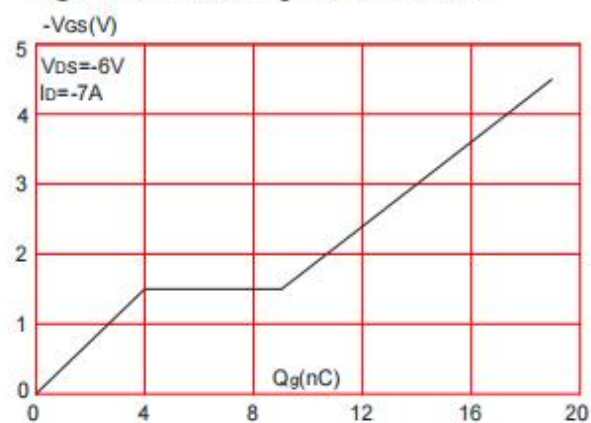
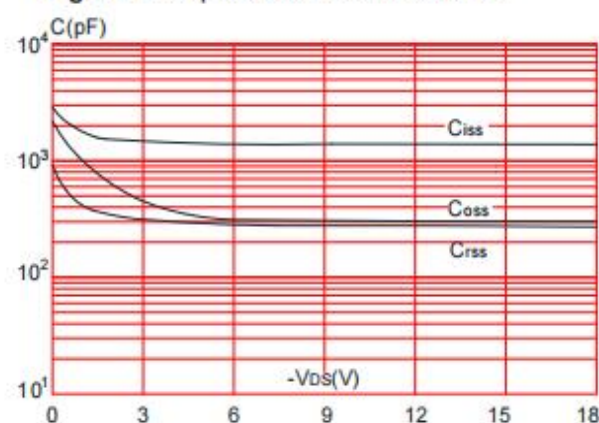
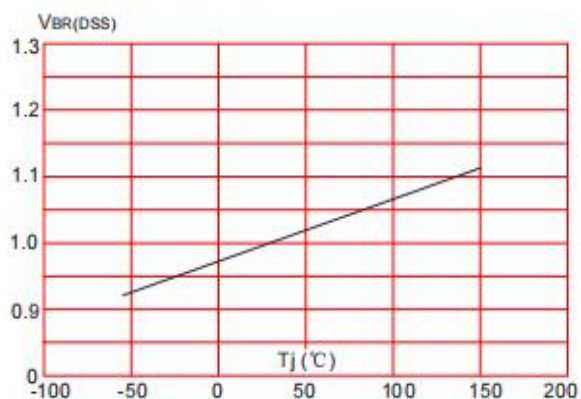
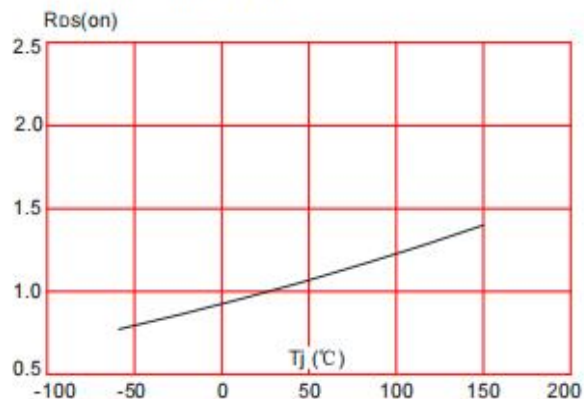
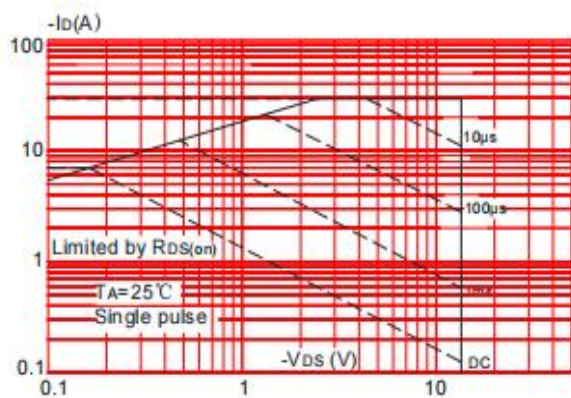
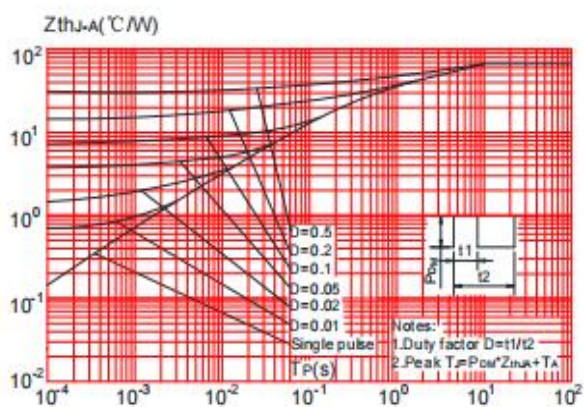
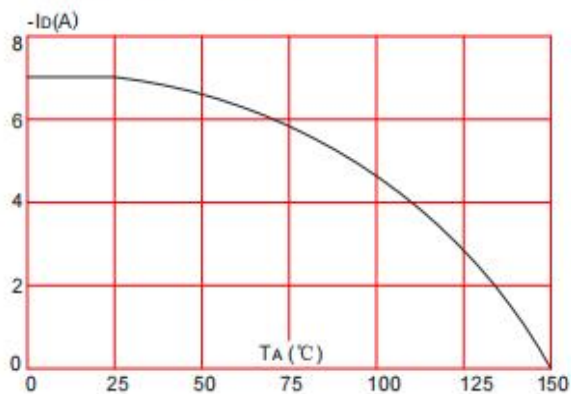


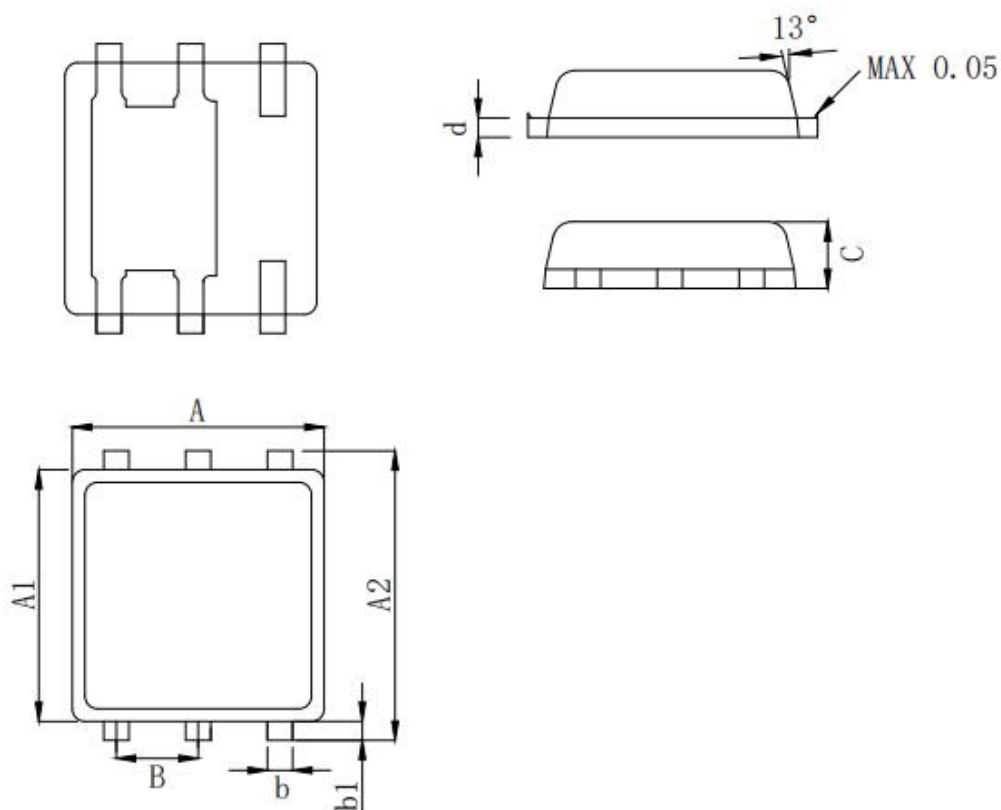
Figure 6: Capacitance Characteristics

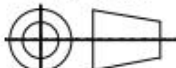


**Figure 7:** Normalized Breakdown Voltage vs. Junction Temperature**Figure 8:** Normalized on Resistance vs. Junction Temperature**Figure 9:** Maximum Safe Operating Area**Figure.11:** Maximum Effective Transient Thermal Impedance, Junction-to-Ambient**Figure 10:** Maximum Continuous Drain Current vs. Ambient Temperature



Package Dimensions DFN2x2-6L



PKG	COMMON DIMENSION (MM)		
	PDFN2X2		
SYMBOL	MIN	TYP	MAX
A	1.950	2.000	2.050
A1	1.950	2.000	2.050
A2	2.150	2.300	2.450
B	0.625	0.650	0.675
b	0.175	0.200	0.225
b1	0.100	0.150	0.200
C	0.510	0.540	0.570
d	0.144	0.152	0.160
TITLE	PDFN2X2 PACKAGE OUTLINE		
DESIGNED BY	YANG		X.X ±0.1
CHECKED BY	XIE		X.XX ±0.01
CHECKED BY	POD-PDFN2X2		X.XXX ±0.005



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