256-Tap, Low-Drift, Digital Potentiometer

Features

- ZJC2739-10: 10 kΩ Normal Resistance
- ZJC2739-100: 100 kΩ Normal Resistance
- 256 Tap Position Variable Resistance Device
- Low Ratiometric Temperature Coefficient: ±5 ppm/°C
- Low Resistor Temperature Coefficient: ±35 ppm/°C
- Single Supply Operation: 2.7 V ~ 5.5 V
- 3-Wire SPI™-Interface Compatible
- Power-on Reset: Wiper Goes to Midscale (Position 128)
- Package: MSOP-8, TSOT23-8, SOIC-8
- Temperature Range: -40 °C to +125 °C

Applications

- Mechanical Potentiometer Replacement
- Low-drift PGAs
- Adjustable Voltage References

General Description

The ZJC2739 provide a single-channel, 256-position, digitally controlled variable resistor (VR) device. These devices perform the same electronic adjustment function as a mechanical potentiometer or variable resistor. The ZJC2739 contains a single variable resistor device in 8-lead MSOP, TSOT23, or SOIC package. Each part contains a fixed resistor with a wiper contact that taps the fixed resistor value at a point determined by the digital code loaded into the controlling serial input register. The resistance between the wiper and either endpoint of the fixed resistor varies linearly with respect to the digital code transferred into the VR latch. Each variable resistor offers a completely programmable value of resistance between the A terminal and the wiper or the B terminal and the wiper.

Block Diagram

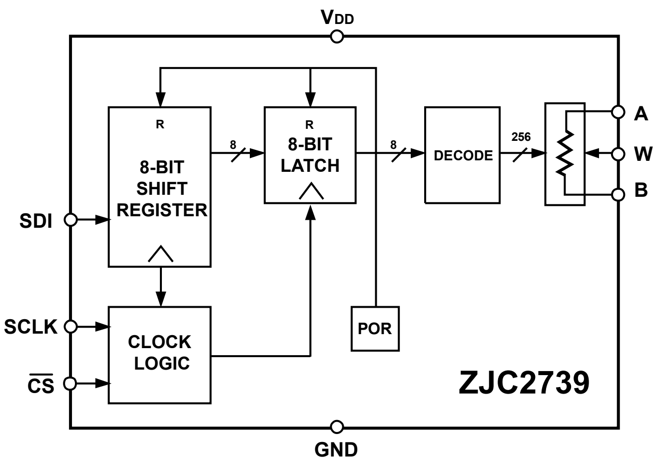

Figure 1. Block Diagram

Typical Characteristics

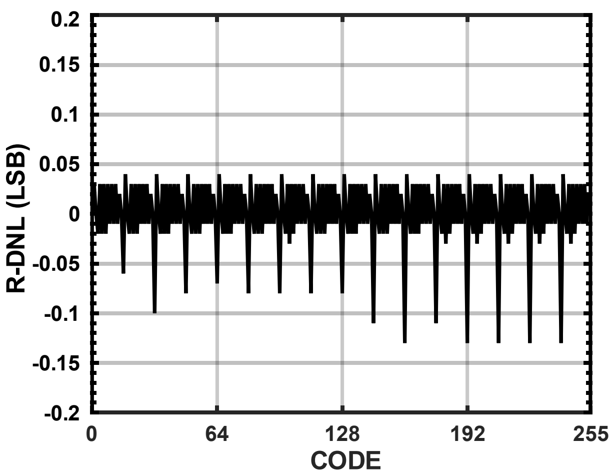

Figure 2. R-DNL vs. Code (10 kΩ)

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Version (Release A)[1]

Apr. 2026 — Release A

Update Specifications and Typical Performance Characteristics

Sep. 2025 — Initial

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Pin Configurations and Function Descriptions

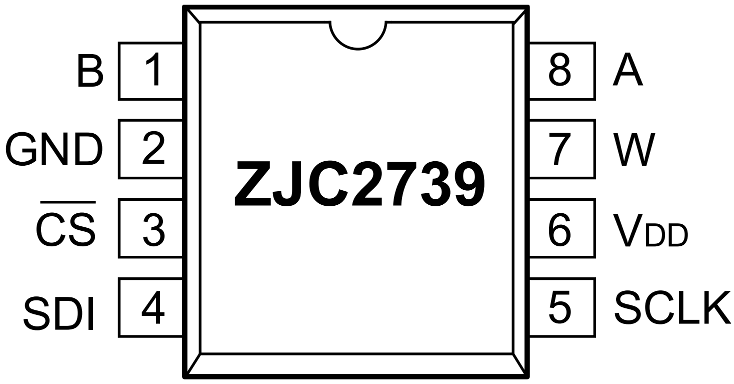

Figure 3. ZJC2739 Pin Configuration (8-lead MSOP, TSOT23 or SOIC)

Mnemonic	Pin No.	I/O[1]	Description
B	1	AI/O	Terminal B
GND	2	G	Ground
$\overline{CS}$	3	DI	Chip Select Input
SDI	4	DI	Serial Data Input.
SCLK	5	DI	Serial Clock Input, Positive Edge Triggered.
V_{DD}	6	P	Power Supply. Bypass with at least a 0.1 µF capacitor to GND
W	7	AI/O	Wiper
A	8	AI/O	Terminal A

[1] AI: Analog Input; AO: Analog Output; P: Power; G: Ground; DI: Digital Input; DO: Digital Output.

Absolute Maximum Ratings[1]

Parameter	Rating
V_{DD} to GND	-0.3 V to +6 V
SDI, SCLK, $\overline{CS}$ to GND	-0.3 V to (V_{DD} + 0.3 V)
V_A, V_B, V_W to GND	-0.3 V to (V_{DD} + 0.3 V)
Maximum Continuous Current into Pins A, B, and W	5 mA (10 kΩ) 1.5 mA (100 kΩ)
Operating Temperature Range	-40 °C to +125 °C
Storage Temperature Range	-60 °C to +150 °C
Junction Temperature Range	150 °C
Reflow Soldering	
Peak Temperature	260 °C
Electrostatic Discharge (ESD)[2]	
Human Body Model (HBM)[3]	3 kV
Charged Device Model (CDM)	2 kV

Thermal Resistance[4]

Package Type	θ_{JA}	θ_{JC}	Unit
8-lead MSOP	190	44	°C/W
8-lead TSOT-23	195	47	°C/W
8-lead SOIC	122.3	60.4	°C/W

[1] These ratings apply at 25 °C, unless otherwise noted. Stresses above these ratings may cause permanent damage. Exposure to absolute maximum conditions for extended periods may degrade device reliability. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those specified is not implied.

[2] Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

[3] ANSI/ESDA/JEDEC JS-001 Compliant.

[4] θ_{JA} addresses the conditions for soldering devices onto circuit boards to achieve surface mount packaging.

Specifications

Electrical Characteristics: R_{AB} = 10 kΩ

The ● denotes the full temperature range (-40 °C to +125 °C) for specified performance. Unless otherwise noted, V_{DD} = 2.7 V to 5.5 V; -40 °C < T_A< +125 °C, unless otherwise noted.

Parameter	Symbol	Conditions		Min	Typ.[1]	Max	Unit
DC Characteristics—Rheostat Mode							
Resolution	N	T_A = +25 °C		8			bits
Rheostat Integral Nonlinearity [2]	R-INL	V_{DD} ≥ 3.3 V	●	-0.6	±0.25	+0.6	LSB
		V_{DD} < 3.3 V	●	-0.8	±0.4	+0.8	LSB
Rheostat Differential Nonlinearity [2]	R-DNL		●	-0.5	±0.15	+0.5	LSB
Nominal Resistor Tolerance	$\Delta R_{AB}/R_{AB}$		●	-15		+15	%
Resistance Temperature Coefficient [3]	$(\Delta R_{AB}/R_{AB})/\Delta T \times 10^6$		●		±35		ppm/°C
Wiper Resistance	R_W		●		50	100	Ω
DC Characteristics—Potentiometer Divider Mode							
Integral Nonlinearity [4]	INL		●	-0.5	±0.25	+0.5	LSB
Differential Nonlinearity [4]	DNL		●	-0.3	±0.1	+0.3	LSB
Full Scale Error	V_{WFSE}		●	-2.0	-1.2		LSB
Zero Scale Error	V_{WZSE}		●		1.2	2.0	LSB
Voltage Divider Temperature Coefficient [3]	$(\Delta_{VW}/_{VW})/\Delta_T \times 10^6$	Code = Half Scale			±5		ppm/°C
Resistor Terminals							
Terminal Voltage Range [5]				GND		V_{DD}	V
Capacitance A/B [3]	C_A,C_B	f = 1 MHz, measured to GND, Code = Half Scale					
		R_{AB} = 10 kΩ			15		pF
Capacitance W [3]	C_W	f = 1 MHz, measured to GND, Code = Half Scale					
		R_{AB} = 10 kΩ			15		pF
Common-mode Leakage Current		V_A = V_W = V_B	●		±15		nA
Digital Input							
Input Logic [3]							
High	V_{INH}		●	0.7 × V_{DD}			V
Low	V_{INL}		●			0.3 × V_{DD}	V
Input Hysteresis [3]	V_{HYST}		●	0.1 × V_{DD}			V
Input Current [3]	I_{IN}		●			1	μA
Input Capacitance [3]	C_{IN}				3		pF
Power Supplies							
Power Supply Range	V_{DD}		●	2.7		5.5	V
Power Supply Current	I_{DD}	V_{IH} = V_{DD} or V_{IL} = GND					
		V_{DD} = 5.0 V			0.2		μA
Power Dissipation [6]	P_{DISS}	V_{IH} = V_{DD} or V_{IL} = GND			1.0		μW
Power Supply Rejection Ratio	PSRR	ΔV_{DD} = V_{DD} ± 10%, Code 80h			-60		dB

1 Typical values represent average readings at 25 °C, V_{DD} = 5 V.
2 Rheostat position non-linearity R-INL is the deviation from an ideal value measured between the maximum resistance and the minimum resistance wiper positions. R-DNL measures the relative step change from the ideal between successive tap positions. I_W = 50 μA for V_{DD} = 3 V and I_W = 400 μA for V_{DD} = 5 V for 10 kΩ version.
3 Guaranteed by design and characterization, not subject to production test.
4 INL and DNL are measured at VW with the device configured in the voltage divider or potentiometer mode. V_A = V_{DD} and V_B = 0 V.
5 Resistor Terminal A, Resistor Terminal B, and Resistor Terminal W have no limitations on polarity with respect to each other
6 P_{DISS} is calculated from (I_{DD} × V_{DD}).

Electrical Characteristics: R_{AB} = 100 kΩ

The ● denotes the full temperature range (-40 °C to +125 °C) for specified performance. Unless otherwise noted, V_{DD} = 2.7 V to 5.5 V; -40 °C < T_A < +125 °C, unless otherwise noted.

Parameter	Symbol	Conditions		Min	Typ.[1]	Max	Unit
DC Characteristics—Rheostat Mode							
Resolution	N	T_A = +25 °C		8			bits
Rheostat Integral Nonlinearity [2]	R-INL	V_{DD} ≥ 3.3 V	●	-0.5	±0.2	+0.5	LSB
		V_{DD} < 3.3 V	●	-0.6	±0.3	+0.6	LSB
Rheostat Differential Nonlinearity [2]	R-DNL		●	-0.5	±0.15	+0.5	LSB
Nominal Resistor Tolerance	$\Delta R_{AB}/R_{AB}$		●	-15		+15	%
Resistance Temperature Coefficient [3]	$(\Delta R_{AB}/R_{AB})/\Delta T \times 10^6$		●		±10		ppm/°C
Wiper Resistance [3]	R_W		●		50	100	Ω
DC Characteristics—Potentiometer Divider Mode							
Integral Nonlinearity [4]	INL		●	-0.5	±0.2	+0.5	LSB
Differential Nonlinearity [4]	DNL		●	-0.3	±0.1	+0.3	LSB
Full Scale Error	V_{WFSE}		●	-0.5	-0.2		LSB
Zero Scale Error	V_{WZSE}		●		0.15	+0.5	LSB
Voltage Divider Temperature Coefficient [3]	$(\Delta_{VW}/_{VW})/\Delta_T \times 10^6$	Code = Half Scale			±5		ppm/°C
Resistor Terminals							
Terminal Voltage Range [5]				GND		V_{DD}	V
Capacitance A/B [3]	C_A, C_B	f = 1 MHz, measured to GND, Code = Half Scale					
		R_{AB} = 100 kΩ			15		pF
Capacitance W [3]	C_W	f = 1 MHz, measured to GND, Code = Half Scale					
		R_{AB} = 100 kΩ			15		pF
Common-mode Leakage Current		$V_A = V_W = V_B$	●		±15		nA
Digital Input							
Input Logic [3]							
High	V_{INH}		●	0.7 × V_{DD}			V
Low	V_{INL}		●			0.3 × V_{DD}	V
Input Hysteresis [3]	V_{HYST}		●	0.1 × V_{DD}			V
Input Current [3]	I_{IN}		●			1	μA
Input Capacitance [3]	C_{IN}				3		pF
Power Supplies							
Power Supply Range	V_{DD}		●	2.7		5.5	V
Power Supply Current	I_{DD}	$V_{IH} = V_{DD}$ or V_{IL} = GND					
		V_{DD} = 5.0 V			0.2		μA
Power Dissipation [6]	P_{DISS}	$V_{IH} = V_{DD}$ or V_{IL} = GND			1.0		μW
Power Supply Rejection Ratio	PSRR	$\Delta V_{DD} = V_{DD}$ ± 10%, Code = Full Scale			-60		dB

1 Typical values represent average readings at 25 °C, V_{DD} = 5 V.
2 Rheostat position non-linearity R-INL is the deviation from an ideal value measured between the maximum resistance and the minimum resistance wiper positions. R-DNL measures the relative step change from the ideal between successive tap positions. I_W = 5 μA for V_{DD} = 3 V and I_W = 40 μA for V_{DD} = 5 V for 100 kΩ version.
3 Guaranteed by design and characterization, not subject to production test.
4 INL and DNL are measured at V_W with the device configured in the voltage divider or potentiometer mode. $V_A = V_{DD}$ and V_B = 0 V.
5 Resistor Terminal A, Resistor Terminal B, and Resistor Terminal W have no limitations on polarity with respect to each other.
6 P_{DISS} is calculated from ($I_{DD} \times V_{DD}$).

Interface Timing Specifications

The ●denotes the full temperature range (-40 °C to +125 °C) for specified performance. Unless otherwise noted, V_{DD} = 2.7 V to 5.5 V; -40 °C < T_A< +125 °C, unless otherwise noted.

Parameter	Symbol		Min	Typ.	Max	Unit
Clock Frequency (V_{DD} = 5 V)	F_{CLK}	●			25	MHz
Clock High Time	t_{HI}	●	18			ns
Clock Low Time	t_{LO}	●	18			ns
$\overline{CS}$ Fall to First Rising SCLK Edge	t_{CSSR}	●	15			ns
Data Input Setup Time	t_{SU}	●	5			ns
Data Input Hold Time	t_{HD}	●	5			ns
SCLK Rise to $\overline{CS}$ Rise Hold Time	t_{CHS}	●	30			ns
SCLK Rise to $\overline{CS}$ Fall Delay	t_{CS0}	●	10			ns
$\overline{CS}$ Rise to SCLK Rise Hold	t_{CS1}	●	100			ns
$\overline{CS}$ High Time	t_{CSH}	●	40			ns

For one frame ($\overline{CS}$ is low) of serial data write operation, if the number of SCLK cycles during the chip select low level is more than 8, the last 8-bit data is valid, and the redundant high bits are ignored.

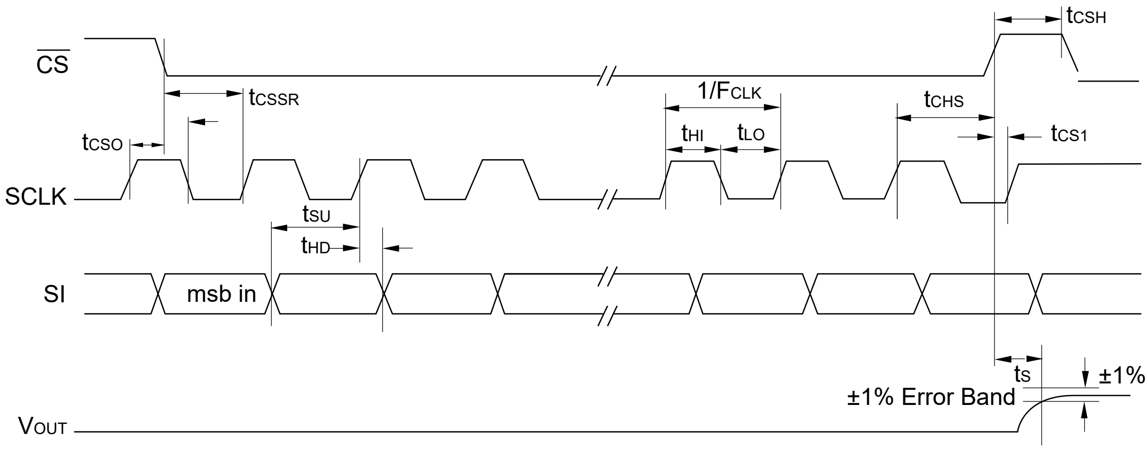

Figure 4. Detailed Serial Interface Timing

Typical Performance Characteristics

Unless otherwise stated, T_A = 25 °C, V_{DD} = 5.0 V.

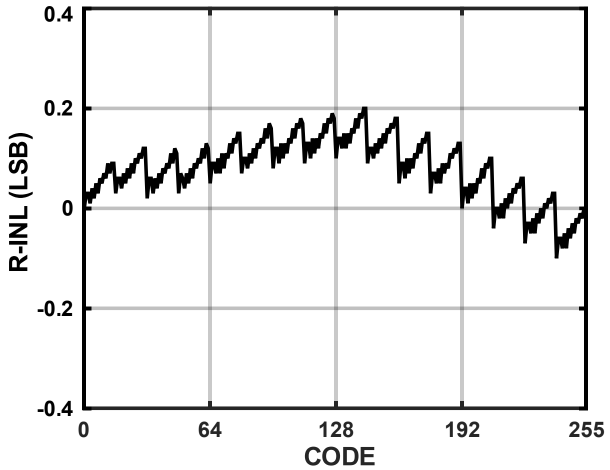

Figure 5. Rheostat-INL vs. Code (10 kΩ)

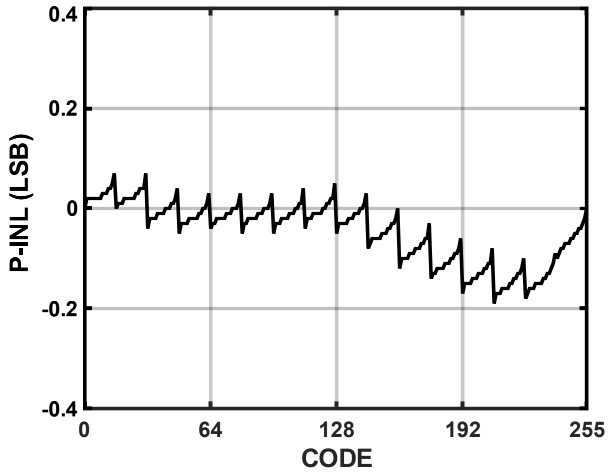

Figure 6. Potentio-INL vs. Code (10 kΩ)

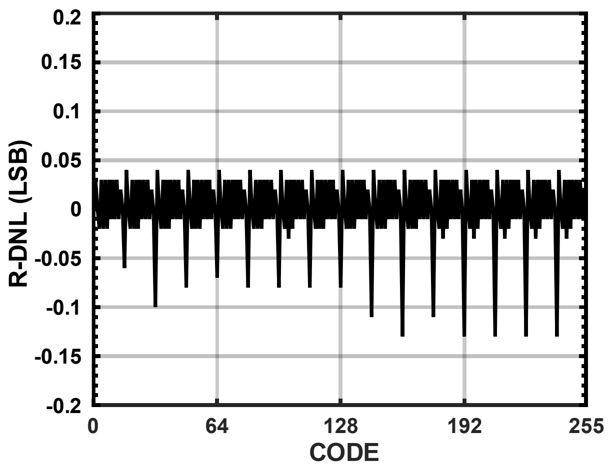

Figure 7. Rheostat-DNL vs. Code (10 kΩ)

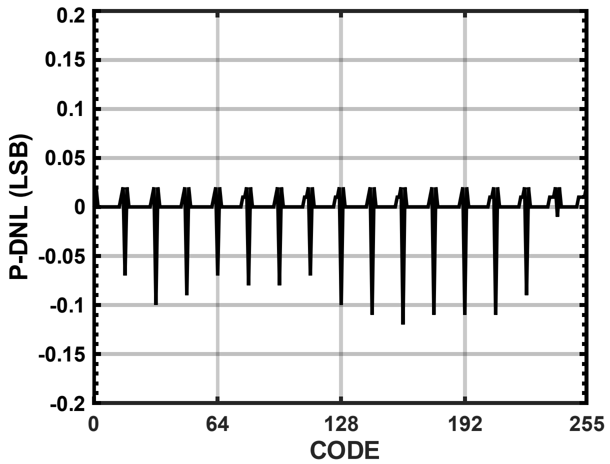

Figure 8. Potentio-DNL vs. Code (10 kΩ)

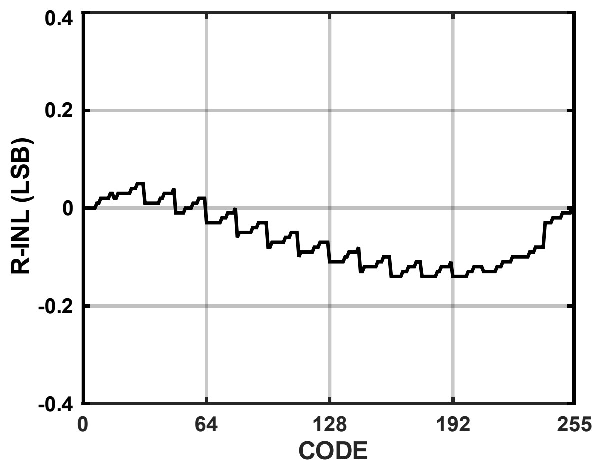

Figure 9. Rheostat-INL vs. Code (100 kΩ)

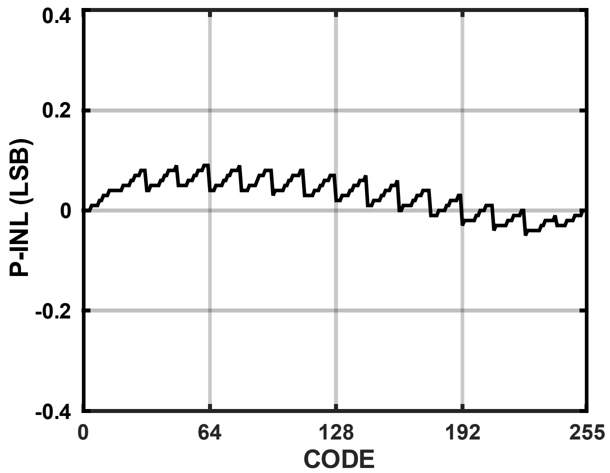

Figure 10. Potentio-INL vs. Code (100 kΩ)

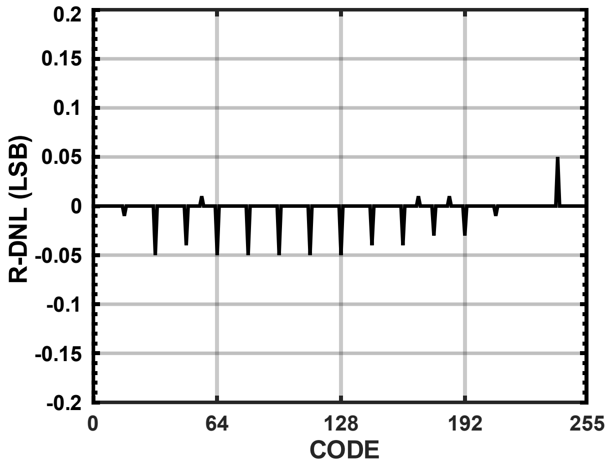

Figure 11. Rheostat-DNL vs. Code (100 kΩ)

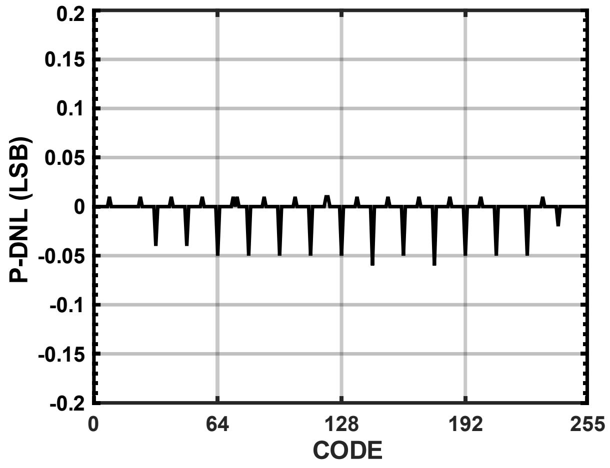

Figure 12. Potentio-DNL vs. Code (100 kΩ)

Serial Interface

Communications from the controller to the ZJC2739 digital potentiometers is by using the SPI serial interface.

Executing any command is accomplished by setting $\overline{CS}$ low and then clocking-in a code byte into the shift register. The code is executed when $\overline{CS}$ is raised. Data is clocked in on the rising edge of clock. The device will track the number of clocks (rising edges) while $\overline{CS}$ is low and will abort if the number of clocks is less than 8. For one frame ($\overline{CS}$ is low) of serial data write operation, if the number of SCLK cycles during the chip select low level is more than 8, the last 8-bit data is valid, and the redundant high bits are ignored.

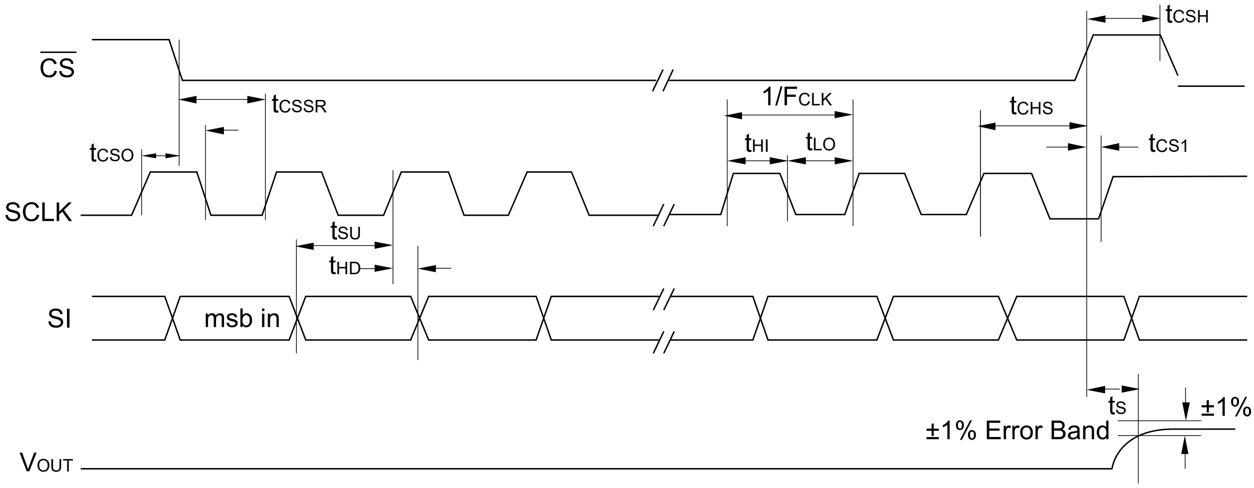

Figure 13. Detailed Serial Interface Timing

Programming the Variable Resistor

Rheostat Operation—±15% Resistor Tolerance

The ZJC2739 operates in rheostat mode when only two terminals are used as a variable resistor. The unused terminal can be floating, or it can be tied to Terminal W.

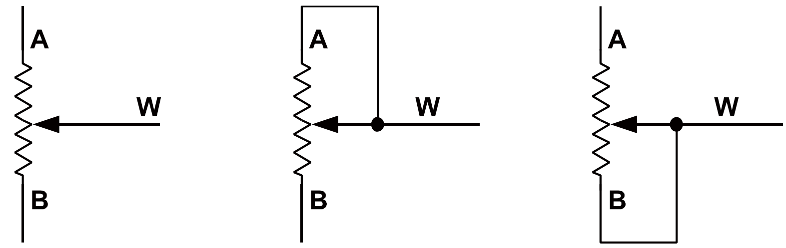

Figure 14. Rheostat Mode Configuration

The nominal resistance between Terminal A and Terminal B, R_{AB}, is 10 kΩ or 100 kΩ, and has 256 tap points accessed by the wiper terminal. The 8-bit data in the RDAC latch is decoded to select one of the 256 possible wiper settings. The general equations for determining the digitally programmed output resistance between Terminal W and Terminal B are

$$R_{WB}(D) = \frac{D}{256} \times R_{AB} + R_W \quad From\ 0x00\ to\ 0xFF$$

where:

- D is the decimal equivalent of the binary code in the 8-bit RDAC register.
- R_{AB} is the end to end resistance.
- R_W is the wiper resistance.

In potentiometer mode, similar to the mechanical potentiometer, the resistance between Terminal W and Terminal A also produces a digitally controlled complementary resistance, R_{WA}. R_{WA} also gives a maximum of 15% absolute. R_{WA} starts at the maximum resistance value and decreases as the data loaded into the latch increases. The general equations for this operation are

$$R_{AW}(D) = \frac{256 - D}{256} \times R_{AB} + R_W \;\; From\ 0x00\ to\ 0xFF$$

where:

- D is the decimal equivalent of the binary code in the 8-bit RDAC register.
- R_{AB} is the end to end resistance.
- R_W is the wiper resistance.

Programming The Potentiometer Divider

Voltage Output Operation

The digital potentiometer easily generates a voltage divider at wiper-to-B and wiper-to-A that is proportional to the input voltage at A to B.

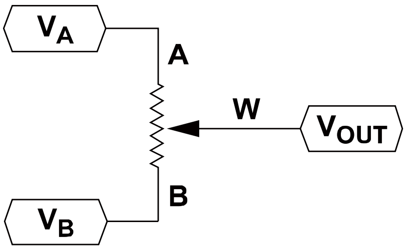

Figure 15. Potentiometer Mode Configuration

$$V_W(D) = \frac{R_{WB}(D)}{R_{AB}} \times V_A + \frac{R_{AW}(D)}{R_{AB}} \times V_B$$

Operation of the digital potentiometer in the divider mode results in a more accurate operation over temperature. The output voltage is dependent mainly on the ratio of the internal resistors, R_{AW} and R_{WB}, and not the absolute values.

Outline Dimensions

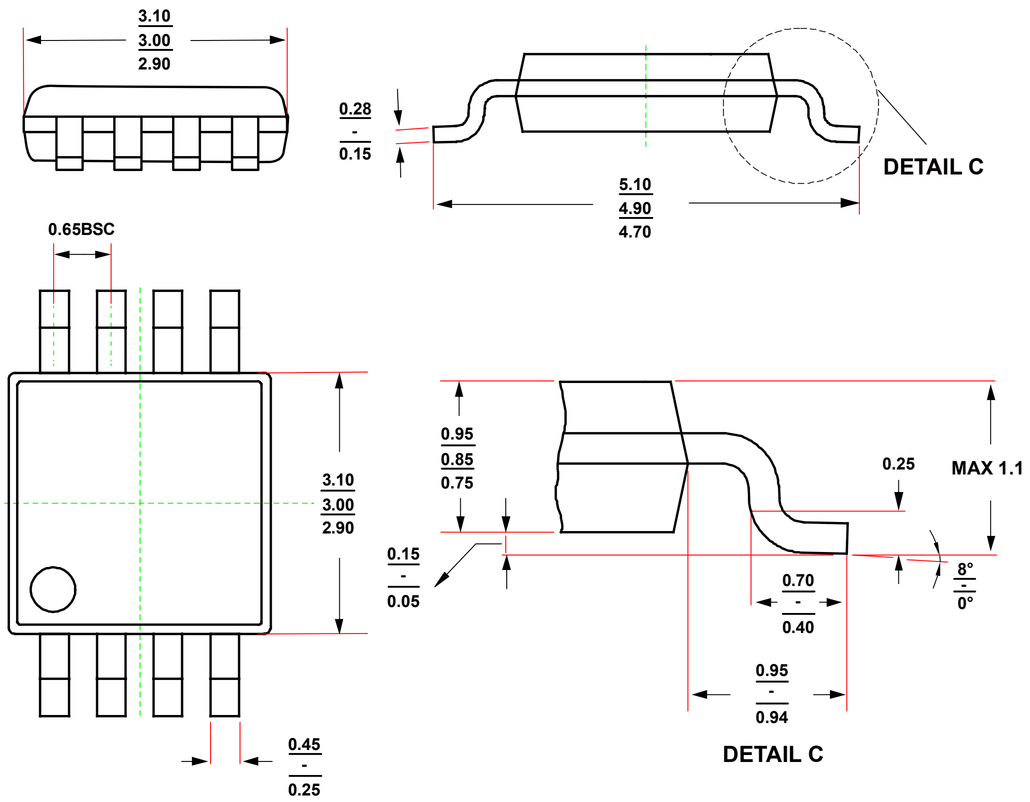

Figure 16. 8-Lead MSOP Package Dimensions shown in millimeters

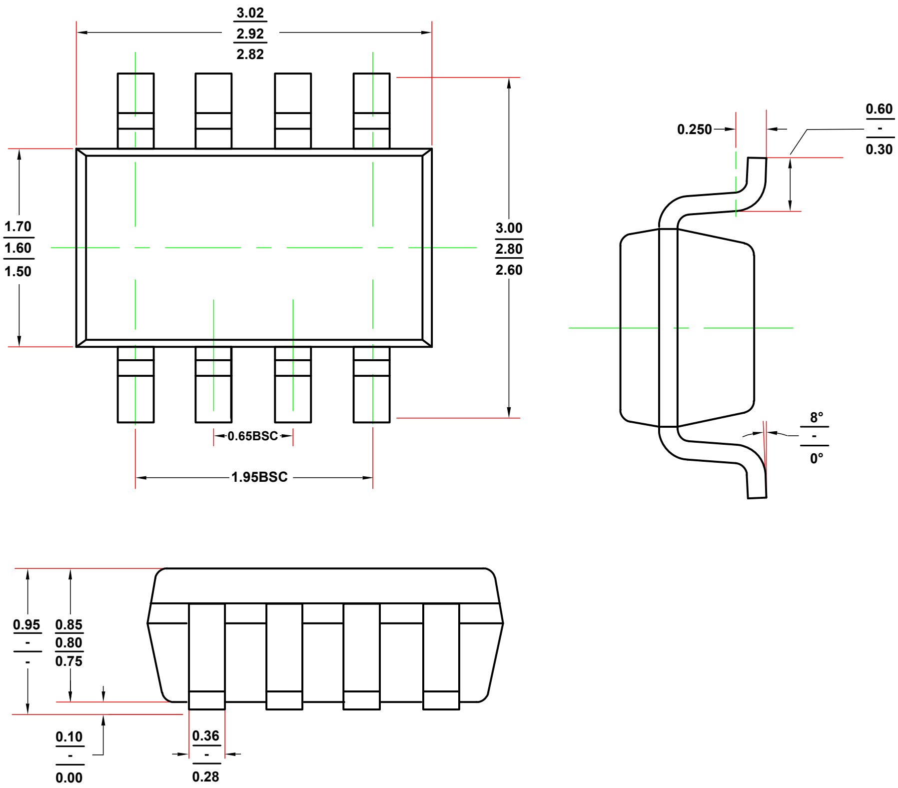

Figure 17. 8-Lead TSOT23 Package Dimensions shown in millimeters

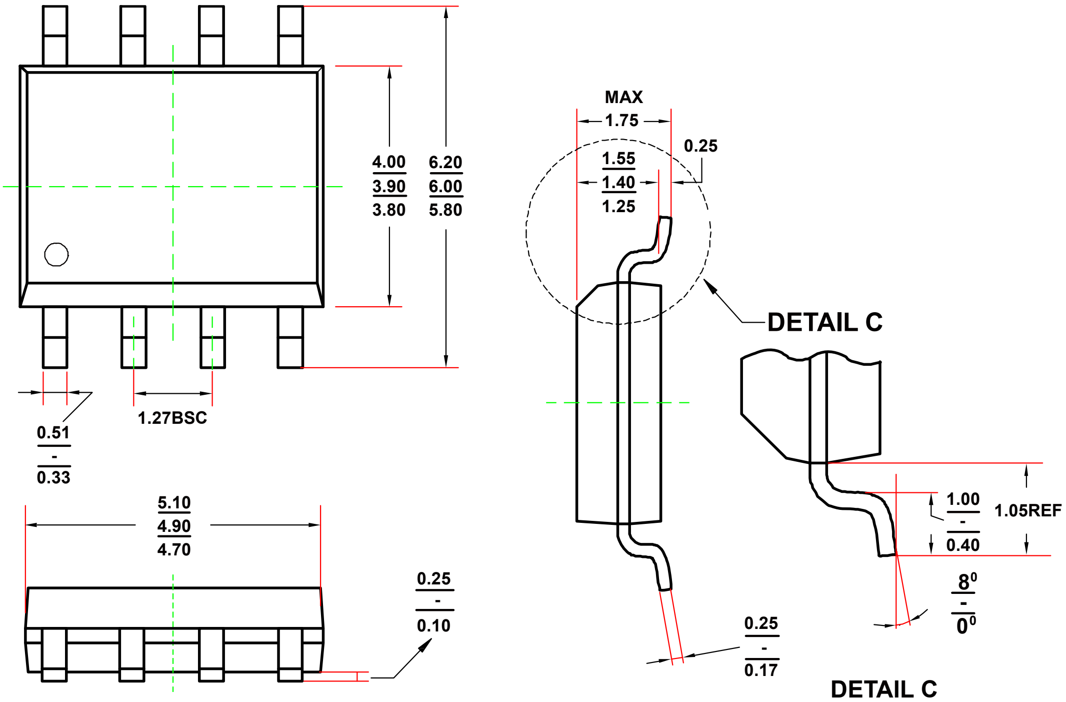

Figure 18. 8-Lead SOIC Package Dimensions shown in millimeters

Ordering Guide

Model	Orderable Device	Package	Marking	Supply Voltage (V)	Temperature Range(°C)	External Package
ZJC2739-10	ZJC2739-10AUABT	MSOP-8	273913	2.7 V to 5.5 V	-40 to +125	Tube
	ZJC2739-10AUABR					13” reel
	ZJC2739-10AZABR	TSOT23-8				7”reel
	ZJC2739-10ASABT	SOIC-8				Tube
	ZJC2739-10ASABR					13” reel
ZJC2739-100	ZJC2739-100AUABT	MSOP-8	273914	2.7 V to 5.5 V	-40 to +125	Tube
	ZJC2739-100AUABR					13” reel
	ZJC2739-100AZABR	TSOT23-8				7”reel
	ZJC2739-100ASABT	SOIC-8				Tube
	ZJC2739-100ASABR					13” reel

Product Order Model

ZJXXXXX X X X X X Q1

- Q1: Automotive Grade
- External Package: T = Tube; R = Reel
- Temperature Range: A = -40 °C to 125 °C Automotive Grade 1, B = -40 °C to 125 °C; E = -40 °C to 85 °C
- Number of Pins: R = 3; K =5; T = 6, A = 8; B = 10; D = 14; E = 16; P = 20
- Package Type: S = SOIC; U = MSOP, TSSOP, SOT; T = DFN, QFN; X = SC70; W = WLCSP; Z = TSOT23
- Grade: B grade is better than A grade
- Base: R = Voltage reference; A = Amplifier; C = Data Converter; G = Switches and Multiplexers; M = Others

Related Parts

Part Number	Description	Comments
ADC		
ZJC2020	20-bit 350 kSPS SAR ADC	Fully differential input, SINAD 101.4 dB, THD -118 dB
ZJC2000/2010	18-bit 400 kSPS/200 kSPS SAR ADC	Fully differential input, SINAD 99.3 dB, THD -113 dB
ZJC2001/2011	16-bit 500 kSPS/250 kSPS SAR ADC	Fully differential input, SINAD 95.3 dB, THD -113 dB
ZJC2002/2012 ZJC2003/2013	16-bit 500 kSPS/250 kSPS SAR ADC	Pseudo-differential unipolar input, SINAD 91.7 dB, THD -105 dB Pseudo-differential bipolar input, SINAD 91.7 dB, THD -105 dB
ZJC2004/2014 ZJC2005/2015	18-bit 400 kSPS/200 kSPS SAR ADC	Pseudo-differential unipolar input, SINAD 94.2 dB, THD -105 dB Pseudo-differential bipolar input, SINAD 94.2 dB, THD -105 dB
ZJC2007/2017 ZJC2008/2018	14-bit 600 kSPS/300 kSPS SAR ADC	Pseudo-differential unipolar input, SINAD 85 dB, THD -105 dB Pseudo-differential bipolar input, SINAD 85 dB, THD -105 dB
ZJC2100/1-18 ZJC2100/1-16	18-bit 400 kSPS/200 kSPS 4-ch differential SAR ADC, SINAD 99.3 dB, THD -113 dB 16-bit 500 kSPS/250 kSPS 4-ch differential SAR ADC, SINAD 95.3 dB, THD -113 dB	
ZJC2102/3-18 ZJC2102/3-16 ZJC2102/3-14	18-bit 400 kSPS/200 kSPS 8-ch pseudo-differential SAR ADC, SINAD 94.2 dB, THD -105 dB 16-bit 500 kSPS/250 kSPS 8-ch pseudo-differential SAR ADC, SINAD 91.7 dB, THD -105 dB 14-bit 600 kSPS/300 kSPS 8-ch pseudo-differential SAR ADC, SINAD 85 dB, THD -105 dB	
ZJC2104/5-18 ZJC2104/5-16	18-bit 400 kSPS/200 kSPS 4-ch pseudo-differential SAR ADC, SINAD 94.2 dB, THD -105 dB 16-bit 500 kSPS/250 kSPS 4-ch pseudo-differential SAR ADC, SINAD 91.7 dB, THD -105 dB	
DAC		
ZJC2541-18/16/14 ZJC2543-18/16/14	18/16/14-bit 1 MSPS single channel DAC with unipolar output	Power on reset to 0 V (ZJC2541) or $V_{REF}/2$ (ZJC2543), 1 nV-S glitch, SOIC-8, MSOP-10/8, DFN-10 packages
ZJC2542-18/16/14 ZJC2544-18/16/14	18/16/14-bit 1 MSPS single channel DAC with bipolar output	Power on reset to 0 V (ZJC2542) or $V_{REF}/2$ (ZJC2544), 1 nV-S glitch, SOIC-14, TSSOP-16, QFN-16 packages
Amplifier		
ZJA3000-1/2/4 ZJA3001-1/2/4	Single/Dual/Quad 36 V low bias current precision Op Amps	3 MHz, 35 µV max Vos, 0.5 µV/°C max TCVos, 25 pA max Ibias, 1 mA/ch, input to V- (ZJA3000 only), RRO, 4.5 V to 36 V
ZJA3018-2 ZJA3008-2	OVP ±75 V, 36 V, Low Power, High Precision Op Amp 36 V, Low Power, High Precision Op Amp	1.3 MHz, 10 µV max Vos, 0.5 µV/°C max TCVos, 25 pA max Ibias, 0.5 mA/ch, OVP ±75 V (ZJA3018 only), RRO, 4.5 V to 36 V
ZJA3512-2	Dual 36 V 7 MHz precision JFET Op Amps	7 MHz, 35 V/µS, 50 µV max Vos, 1 µV/°C max TCVos, 2 mA/ch, RRO, 9 V to 36 V
ZJA3216/06/02-1/2	Precision 20/10/5 MHz CMOS RRIO Op Amps	20/10/5 MHz, RRIO, 30 µV max Vos, 1 µV/°C max TCVos, 0.6 pA Ib, 2.7 V to 5.5 V
ZJA3600/1	36 V ultra-high precision in-amp	CMRR 105 dB min (G = 1), 25 pA max Ib, 25 µV max Vosi, ±2.4 V to ±18 V, -40 °C to 125 °C
ZJA3611, ZJA3609	36 V precision wider bandwidth precision in-amp (G ≥ 10)	CMRR 120 dB min (G = 10), 25 pA max Ibias, 25 µV max Vosi, 1.2 MHz BW (G = 10)
ZJA3676/7 ZJA3678/9	Low power, G=1 Single/Dual 36 V difference amplifier Low power, G=0.5/2 Single/Dual 36 V difference amplifier	Input protection to ±65 V, CMRR 104 dB min (G = 1), Vos 100 µV max, gain error 15 ppm max, 500 kHz BW (G = 1), 330 µA/channel, 2.7 V to 36 V
ZJA3669	High Common-Mode Voltage Difference Amplifier	±270 V CMV, 2.5 kV ESD, 96 dB min CMRR, 450 kHz BW, 4 V to 36 V, SOIC-8
ZJA3100	15 V precision fully differential amplifier	145 MHz, 447 V/µS, 50 nS to 16-bit, 50 µV max Vos, 4.6 mA Iq, SOIC/MSOP-8, QFN-16
ZJA3236/26/22-2	Low-cost 20/10/5 MHz CMOS RRIO Op Amps	20/10/5 MHz, RRIO, 2 mV max Vos, 6 µV/°C max TCVos, 0.6 pA Ib, 2.7 V to 5.5 V
ZJA3622/8	36 V low-cost precision in-amp	0.5 nA max Ibias, 125 µV max Vosi, 625 kHz BW (G = 10), 3.3 mA Iq, ±2.4 V to ±18 V
Voltage Reference		
ZJR1004	40 V supply precision voltage reference	V_{OUT} = 2.048/2.5/3/3.3/4.096/5/10 V, 5 ppm/°C max drift -40 °C to 125 °C
ZJR1001/2 ZJR1003	5.5 V low power voltage reference (ZJR1001 with noise filter option)	V_{OUT} = 2.048/2.5/3/3.3/4.096/5 V, 5 ppm/°C max drift -40 °C to 125 °C, ±0.05% initial error, 130 µA, ZJR1001/2 in SOT23-6, ZJR1003 in SOIC/MSOP-8
ZJR1302	5.5 V low power compact precision voltage reference	V_{OUT} = 2.048/2.5/3/3.3/4.096 V, 30 ppm/°C max drift -40 °C to 125 °C, 130 µA, SOT23-3
Switches and Multiplexers		
ZJG4438/4439	36 V fault protection 8:1/dual 4:1 multiplexer	Protection to ±50 V power on & off, latch-up immune, Ron 270 Ω, 14.8 pC, t_{ON} 166 nS
ZJG4428/4429	36 V 8:1/dual 4:1 multiplexer	Latch-up immune, Ron 270 Ω, 14.8 pC charge injection, t_{ON} 166 nS
Quad Matching Resistor		
ZJM5400	±75 V precision match resistors	Mismatch < 100 ppm, 10k:10k:10k:10k, 100k:100k:100k:100k, 100k:10k:10k:100k, 1k:1k:1k:1k, 1M:1M:1M:1M, 5k:1k:1k:5k, 5k:1.25k:1.25k:5k, 9k:1k:1k:9k, ESD: 3.5 kV