600-nA, 5-V Operational Amplifier

Features

- Supply Voltage: 1.8 V to 5.5 V
- Low Supply Current: 600 nA per Channel (Max)
- Offset Voltage: ±1.5 mV (Max)
- Offset Voltage Temperature Drift: 0.4 μV/℃
- Low Input Bias Current: 30 pA from −40℃ to 85℃
- Input Common-Mode Voltage Range Includes Ground
- Rail-to-Rail Input and Output
- Bandwidth: 10 kHz
- Operating Temperature Range: −40℃ to 125℃

Applications

- Current Sensing
- Threshold Detectors/Discriminators
- Low-Power Filters
- Handsets and Mobile Accessories
- Wireless Remote Sensors, Active RFID Readers
- Gas/Oxygen/Environment Sensors
- Battery or Solar-Powered Devices
- Sensor Network Powered by Energy Scavenging

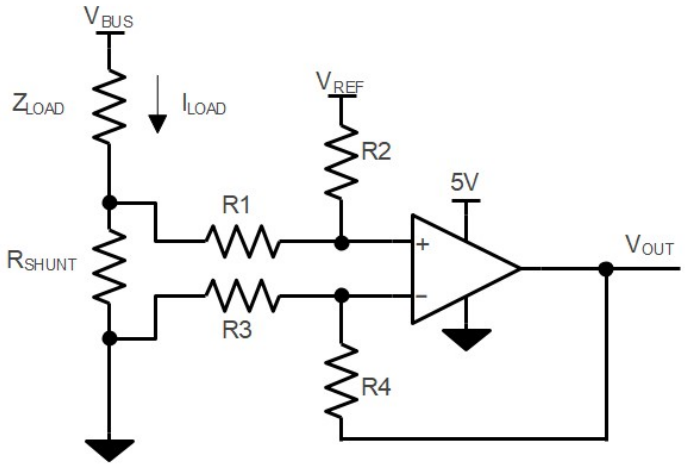
Description

The TP211x is a series of ultra-low power, precision CMOS operational amplifiers that provide a constant 10-kHz bandwidth and a 10-mV/μs slew rate with a maximum quiescent current of only 600 nA per amplifier. The ground-sensing input common-mode range, which guarantees a 1.5-mV V_{OS} and an ultra-low 0.4-μV/°C V_{OS} TC, enables accurate and stable measurement for both high-side and low-side current sensing.

The TP211x series has a carefully designed CMOS input stage that outperforms competitors with a typically 0.1-fA I_B. This ultra-low input current significantly reduces I_B and I_{OS} errors introduced in the giga-Ω resistance, high-impedance photodiode, and charge sense situations. The TP211x series is unity gain stable with a 1,000-nF capacitive load. It can operate from a single-supply voltage of +1.8 V to +5.5 V or a dual-supply voltage of ±0.9 V to ±2.75 V, and features ground-sensing inputs and the rail-to-rail output.

The combined features make the TP211x series ideally suited for a variety of 2-cell NiCd/Alkaline battery or single-Li+ battery-powered portable applications. Potential applications include low-frequency signal conditioning, mobile accessories, wireless remote sensing, vibration monitors, ECGs, pulse monitors, glucose meters, smoke and fire detectors, and backup battery sensors.

Typical Application Circuit



$V_{OUT} = (I_{LOAD} \times R_{SHUNT}) \times (R2 / R1) + V_{REF}$

When R3 = R1, R2 = R4, $R_{SHUNT} << R1$

Table of Contents

Revision History

Date	Revision	Notes
2014-01-01	Rev.A.0	Initial version.
2018-12-31	Rev.A.1	Updated the format. Updated Datasheet Limit. Corrected the Marking Information of TP2111-CR: from B1C to B1T.
2024-04-11	Rev.A.2	Added the maximum I_B at −40°C to 85°C. Added new P/N: TP2112-DFGR-S. Upgraded the format of the datasheet.
2024-11-14	Rev.A.3.Pre	Updated EC Table of I_B: • Added specification of 5°C to 45°C.
2024-12-18	Rev.A.3	Changed the status of the TP2112-DFGR-S to production in the Order Information. The following updates are all about the new datasheet formats or typos, and the actual product remains unchanged. • Updated the Package Outline Dimensions. • Updated the Tape and Reel Information. • Updated the Order Information.
2025-11-27	Rev.A.4	Added the thermal pad description in the Pin Configuration and Functions. The actual product remains unchanged.

Pin Configuration and Functions

TP2111
SOT23-5/SOT353 (SC70-5)
Top View

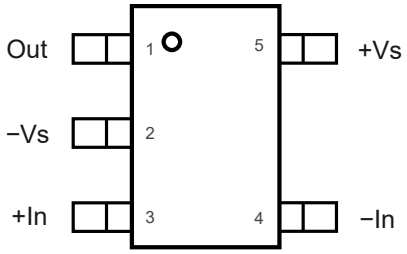
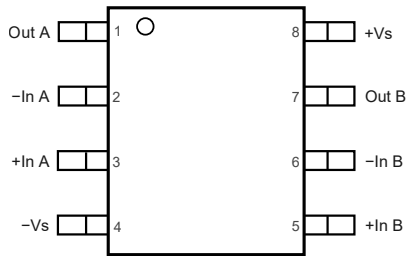


Table 1. Pin Functions: TP2111

Pin No.	Name	I/O	Description
1	Out	O	Output
2	$-V_S$	Power Supply	Negative power supply
3	+In	I	Non-inverting input
4	−In	I	Inverting input
5	$+V_S$	Power Supply	Positive power supply

TP2112
SOP8/TSSOP8/MSOP8
Top View



TP2112
DFN2X2-8
Top View

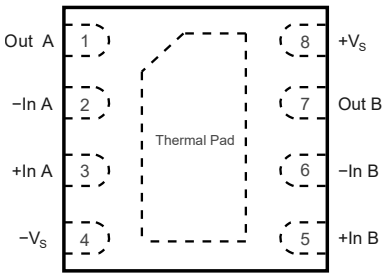


Table 2. Pin Functions: TP2112

Pin No.		Name	I/O	Description
1	1	Out A	O	Output
2	2	−In A	I	Inverting input
3	3	+In A	I	Non-inverting input
4	4	$-V_S$	Power Supply	Negative power supply
5	5	+In B	I	Non-inverting input
6	6	−In B	I	Inverting input
7	7	Out B	O	Output
8	8	$+V_S$	Power Supply	Positive power supply
		Thermal Pad		The thermal pad of the DFN2X2-8 is recommended to be left float or connected to $-V_S$.

TP2114
SOP14/TSSOP14
Top View

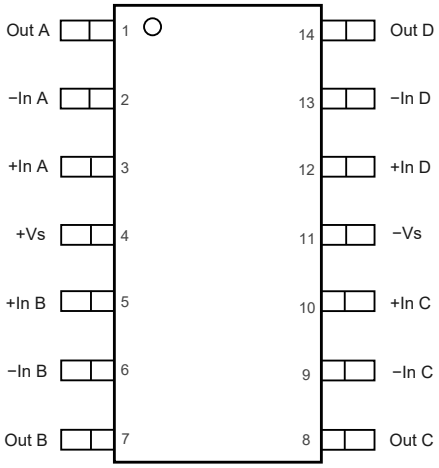


Table 3. Pin Functions: TP2114

Pin No.	Name	I/O	Description
1	Out A	O	Output
2	−In A	I	Inverting input
3	+In A	I	Non-inverting input
4	$+V_S$	Power Supply	Positive power supply
5	+In B	I	Non-inverting input
6	−In B	I	Inverting input
7	Out B	O	Output
8	Out C	O	Output
9	−In C	I	Inverting input
10	+In C	I	Non-inverting input
11	$-V_S$	Power Supply	Negative power supply
12	+In D	I	Non-inverting input
13	−In D	I	Inverting input
14	Out D	O	Output

Specifications

Absolute Maximum Ratings (1)

Parameter		Min	Max	Unit
	Supply Voltage: $(+V_S) – (-V_S)$		6	V
	Input Voltage	$(-V_S) – 0.3$	$(+V_S) + 0.3$	V
	Differential Input Voltage	−6	6	V
	Input Current: +IN, −IN (2)	−10	10	mA
	Output Short-Circuit Duration (3)		Infinite	
T_J	Maximum Junction Temperature		150	°C
T_A	Operating Temperature Range	−40	125	°C
T_{STG}	Storage Temperature Range	−65	150	°C
T_L	Lead Temperature (Soldering, 10 sec)		260	°C

(1) Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. Exposure to any Absolute Maximum Rating condition for extended periods may affect device reliability and lifetime.
(2) The inputs are protected by ESD-protection diodes to the negative power supply. If the input extends more than 300 mV beyond the negative power supply, the input current should be limited to less than 10 mA.
(3) A heat sink may be required to keep the junction temperature below the absolute maximum. This depends on the power supply voltage and how many amplifiers are shorted. The thermal resistance varies with the amount of PC board metal connected to the package. The specified values are for short traces connected to the leads.

ESD, Electrostatic Discharge Protection

Symbol	Parameter	Condition	Minimum Level	Unit
HBM	Human Body Model ESD	ANSI/ESDA/JEDEC JS-001 (1)	6	kV
CDM	Charged Device Model ESD	ANSI/ESDA/JEDEC JS-002 (2)	2	kV

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

Thermal Information

Package Type	θ_{JA}	θ_{JC}	Unit
SOT353 (SC70-5)	400		°C/W
SOT23-5	250	81	°C/W
SOP8	158	43	°C/W
MSOP8	210	45	°C/W
SOP14	120	36	°C/W
TSSOP14	180	35	°C/W

Electrical Characteristics

All test conditions: V_S = 5 V, T_A = 25°C, R_L = 100 kΩ to V_S / 2, unless otherwise noted.

Symbol	Parameter	Conditions	T_A	Min	Typ	Max	Unit
Power Supply							
V_S	Supply Voltage Range			1.8		5.5	V
I_Q	Quiescent Current per Amplifier	V_S = 5 V			500	600	nA
			−40°C to 125°C			900	nA
PSRR	Power Supply Rejection Ratio	V_S = 1.8 V to 5.5 V		70	90		dB
Input Characteristics							
V_{OS}	Input Offset Voltage	V_S = 5 V, V_{CM} = 2.5 V		−1.5	0.1	1.5	mV
			−40°C to 125°C	−2.5		2.5	mV
V_{OS} TC	Input Offset Voltage Drift		−40°C to 125°C		0.4		µV/°C
I_B	Input Bias Current				1		pA
			5°C to 45°C		4	20 (2)	pA
			−40°C to 85°C		4	30 (2)	pA
			−40°C to 125°C		10		pA
I_{OS}	Input Offset Current				1		pA
C_{IN}	Input Capacitance	Differential mode			3		pF
		Common mode			5		pF
A_V	Open-Loop Voltage Gain			80	120		dB
V_{CMR}	Common-Mode Input Voltage Range			(−V_S)		(+V_S)	V
CMRR	Common-Mode Rejection Ratio	V_{CM} = 0 V to 3.5 V		78	110		dB
		V_{CM} = 0 V to 5 V		60	80		dB
Output Characteristics							
V_{OH}	Output Voltage Swing from Positive Rail	R_{LOAD} = 100 kΩ to V_S / 2			10	30	mV
			−40°C to 125°C			50	mV
V_{OL}	Output Voltage Swing from Negative Rail	R_{LOAD} = 100 kΩ to V_S / 2			10	30	mV
			−40°C to 125°C			50	mV
I_{SC}	Output Short-Circuit Current				20		mA
AC Specifications							
GBW	Gain-Bandwidth Product				10		kHz
SR	Slew Rate	G = 1, 2-V step			6		mV/µs
t_S	Settling Time, 0.1%	G = 1, 2-V step			0.5		ms
	Settling Time, 0.01%				0.55		ms
PM	Phase Margin	R_L = 100 kΩ, C_L = 60 pF			65		°
GM	Gain Margin	R_L = 100 kΩ, C_L = 60 pF			10		dB

Symbol	Parameter	Conditions	T_A	Min	Typ	Max	Unit
Noise Performance							
E_N	Input Voltage Noise	f = 0.1 Hz to 10 Hz			10		μV_{PP}
e_N	Input Voltage Noise Density	f = 1 kHz			265		nV/√Hz

(1) The input offset voltage is the average of the input-referred trip points. The input hysteresis is the difference between the input-referred trip points.
(2) Provided by the bench tests and design simulation.
(3) The delay time is measured from the mid-point of the input to the mid-point of the output.

Typical Performance Characteristics

All test conditions: V_S = 5 V, V_{CM} = 2.5 V, R_L = Open, unless otherwise noted.

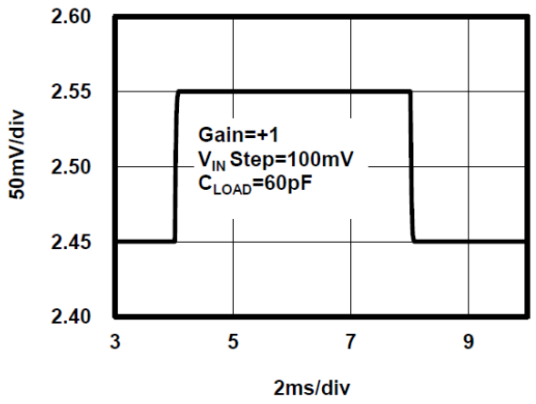


Figure 1. Small-Signal Step Response, 100-mV Step

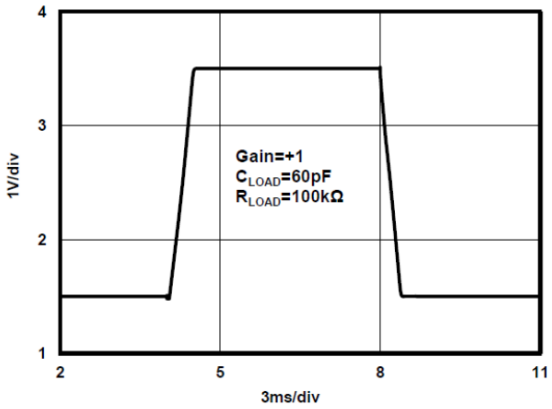


Figure 2. Large-Signal Step Response, 2-V Step

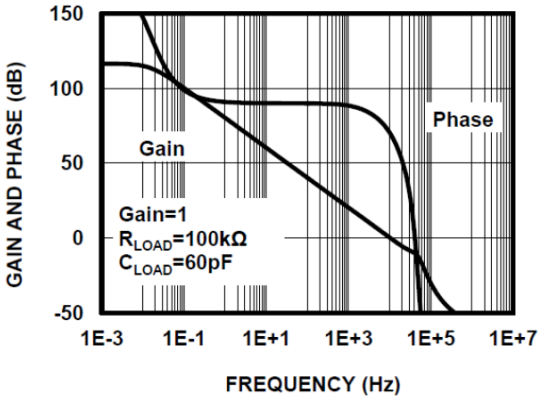


Figure 3. Open-Loop Gain and Phase

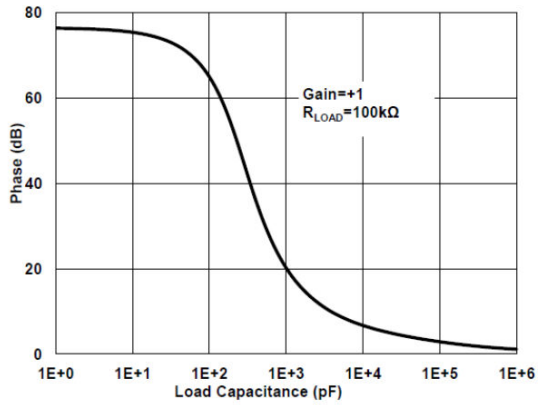


Figure 4. Phase Margin vs. C_{LOAD} (Stable for any C_{LOAD})

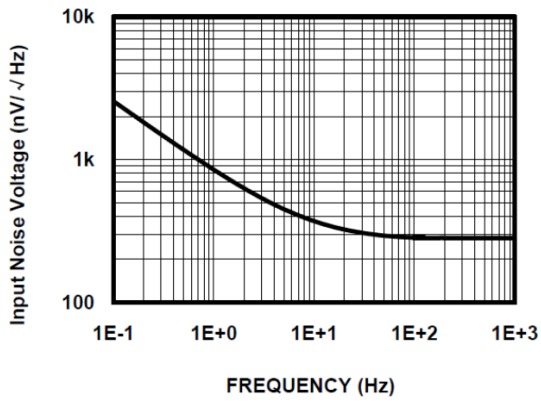


Figure 5. Input Voltage Noise Spectral Density

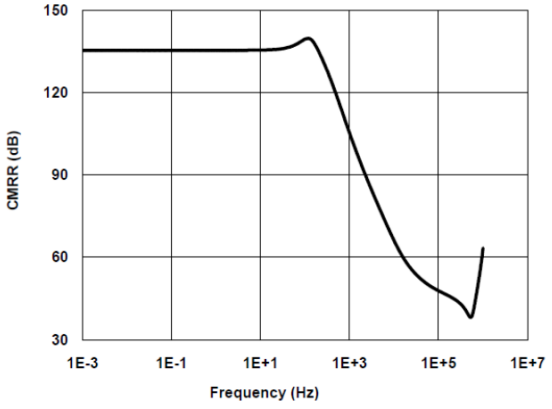


Figure 6. Common-Mode Rejection Ratio

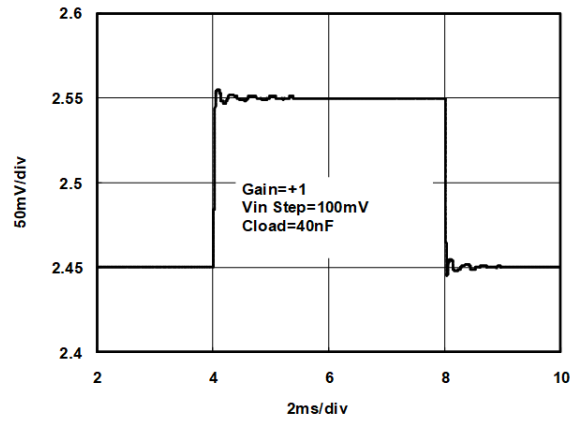


Figure 7. Over-Shoot Voltage, C_{LOAD} = 40 nF, Gain = +1, R_{FB} = 100 kΩ

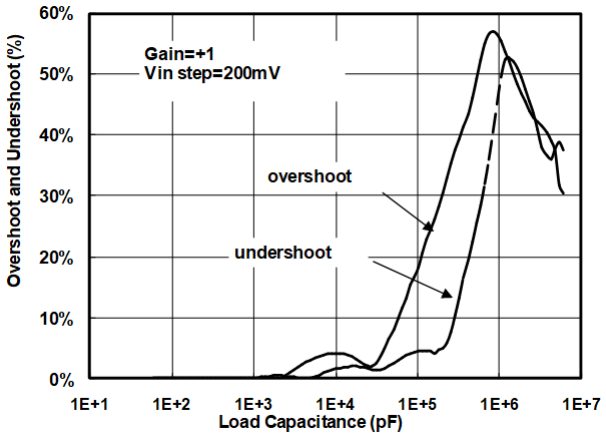


Figure 8. Over-Shoot % vs. C_{LOAD}, Gain = +1, R_{FB} = 1 MΩ

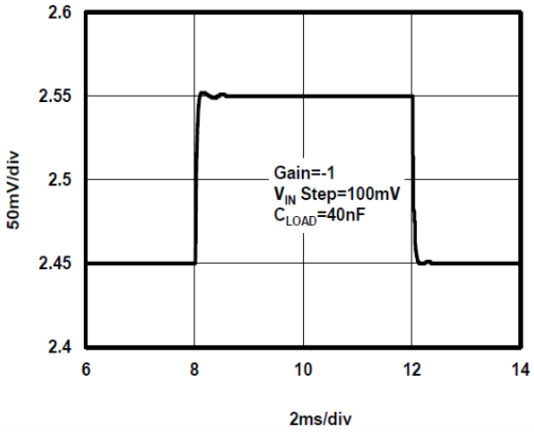


Figure 9. Over-Shoot Voltage, C_{LOAD} = 40 nF, Gain = −1, R_{FB} = 100 kΩ

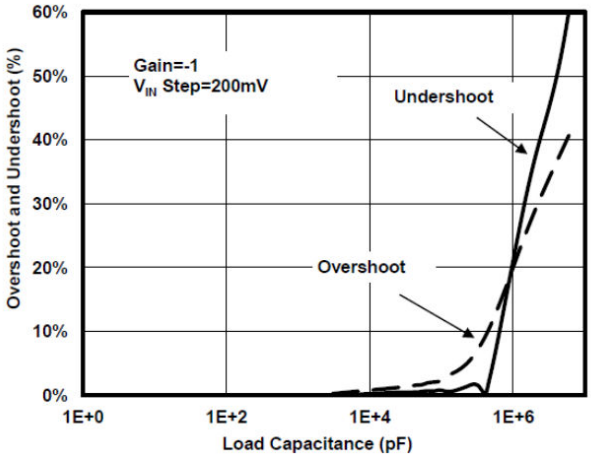


Figure 10. Over-Shoot % vs. C_{LOAD}, Gain = −1, R_{FB} = 1 MΩ

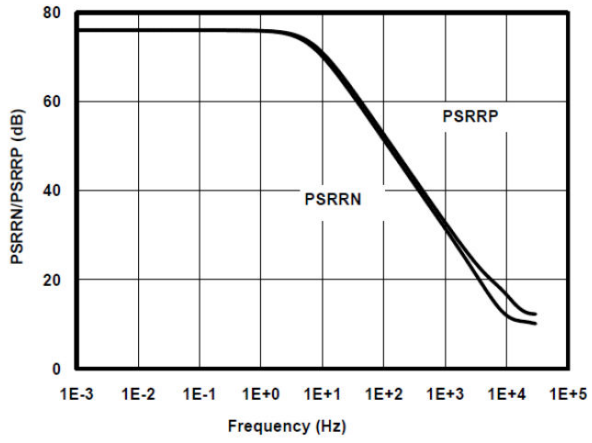


Figure 11. Power-Supply Rejection Ratio

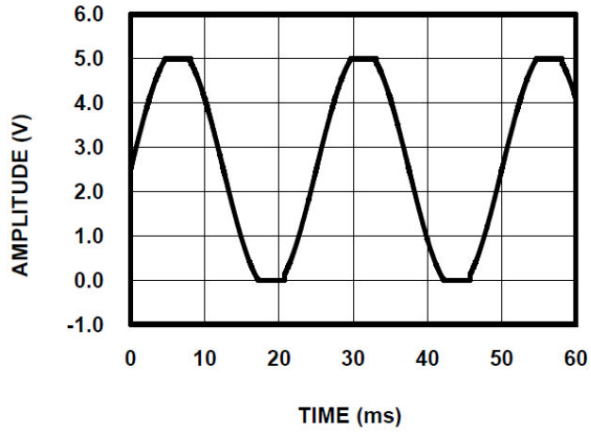


Figure 12. V_{IN} = −0.2 V to 5.2 V, No Phase Reversal

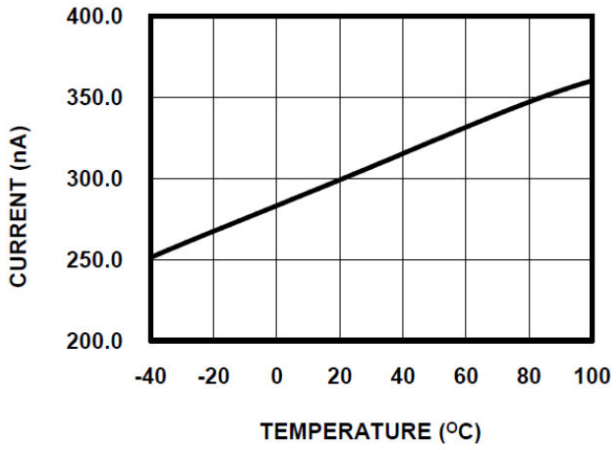


Figure 13. Quiescent Supply Current vs. Temperature

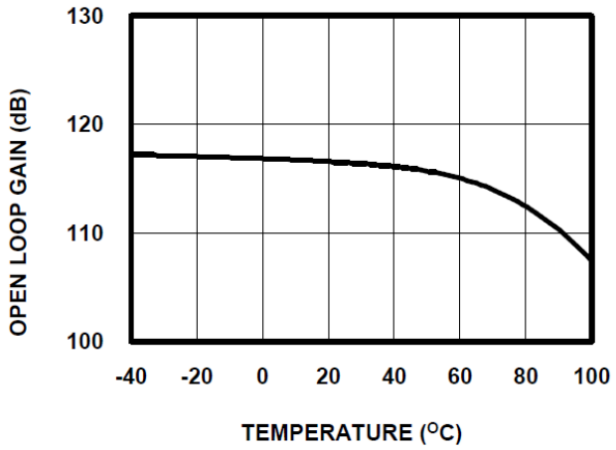


Figure 14. Open-Loop Gain vs. Temperature

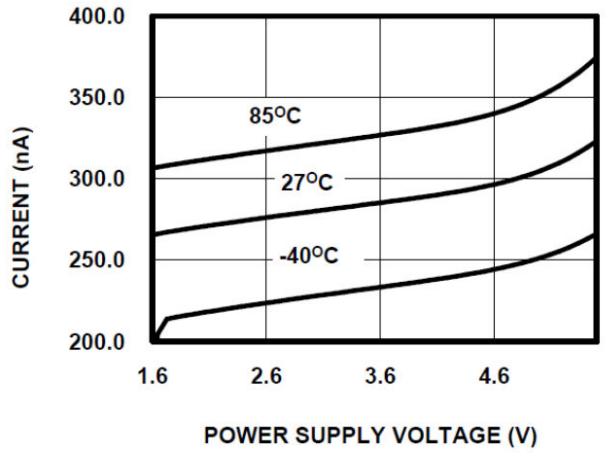


Figure 15. Quiescent Supply Current vs. Supply Voltage

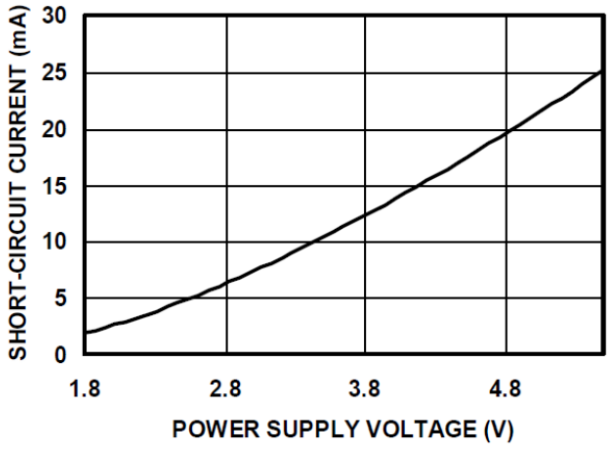


Figure 16. Short-Circuit Current vs. Supply Voltage

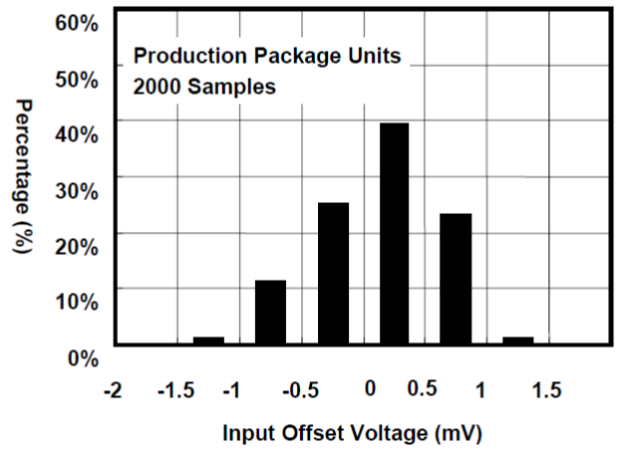


Figure 17. Input Offset Voltage Distribution

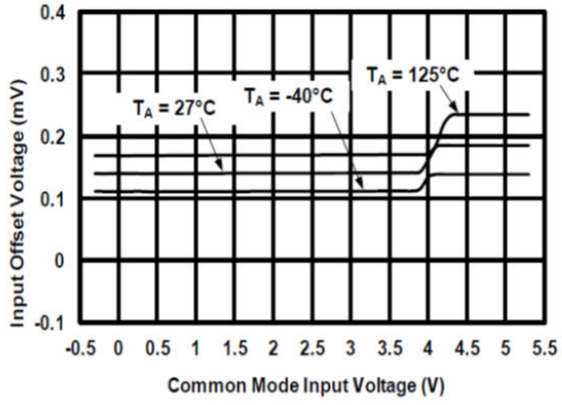


Figure 18. Input Offset Voltage vs. Common-Mode Input Voltage

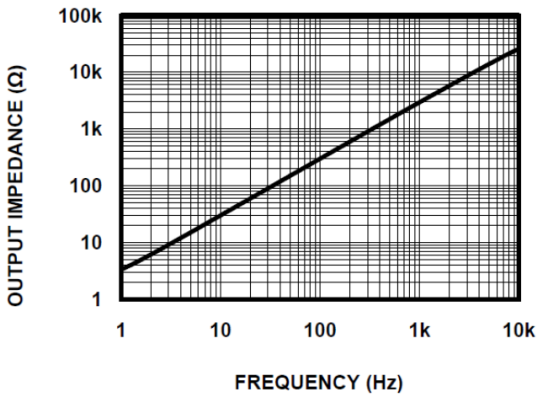


Figure 19. Closed-Loop Output Impedance vs. Frequency

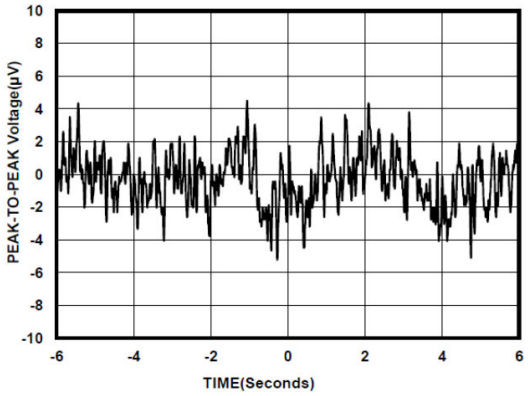


Figure 20. 0.1-Hz to 10-Hz Time Domain Output Voltage Noise

Detailed Description

Overview

The TP211x is a series of ultra-low power, precision CMOS operational amplifiers that provide a constant 10-kHz bandwidth and a 10-mV/μs slew rate with a maximum quiescent current of only 600 nA per amplifier. The ground-sensing input common-mode range, which guarantees a 1.5-mV V_{OS} and an ultra-low 0.4-μV/°C V_{OS} TC, enables accurate and stable measurement for both high-side and low-side current sensing.

Functional Block Diagram

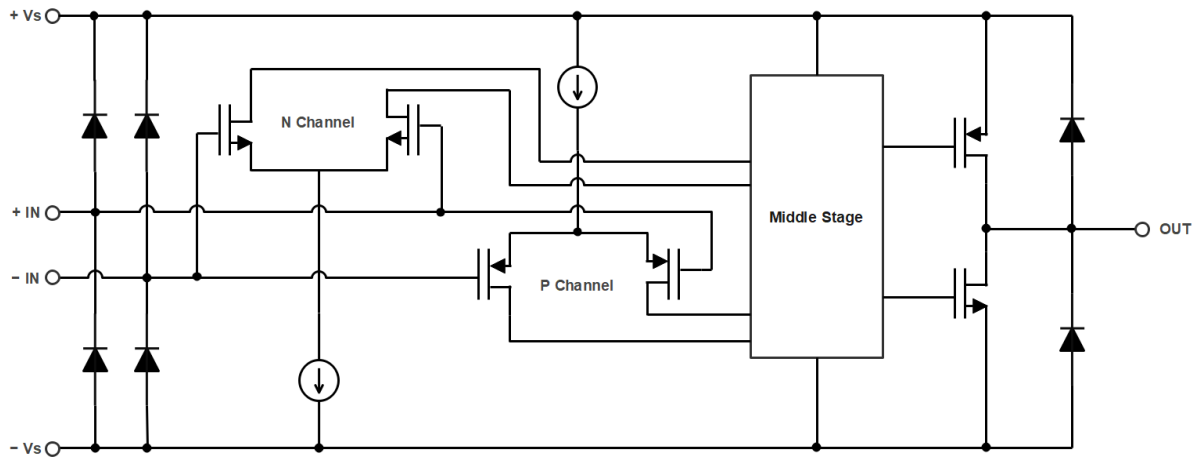


Figure 21. Functional Block Diagram

Application and Implementation

> Note
>
> Information in the following application sections is not part of the 3PEAK's component specification and 3PEAK does not warrant its accuracy or completeness. 3PEAK's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

Application Information

Low Supply Voltage and Low Power Consumption

The TP211x family of operational amplifiers can operate with power supply voltages from 2.1 V to 6.0 V. Each amplifier draws a quiescent current of only 300 nA. The low supply voltage capability and low supply current are ideal for portable applications that require high capacitive load driving capability and constant wide bandwidth. The TP211x family is optimized for wide-bandwidth low-power applications. It has an industry-leading high GBWP to power ratio and is unity gain stable for any capacitive load. When the load capacitance increases, the increased capacitance at the output pushes the non-dominant pole to lower the frequency in the open-loop frequency response, lowering the phase and gain margin. Higher gain configurations tend to have better capacitive drive capability than lower gain configurations due to lower closed-loop bandwidth and higher phase margin.

Low Input Referred Noise

The TP211x family provides a low input referred noise density of 296 nV/√Hz at 1 kHz. The voltage noise grows slowly with the frequency in the wideband range, and the input voltage noise is typically 12 μV_{PP} at the frequency of 0.1 Hz to 10 Hz.

Low Input Offset Voltage

The TP211x family has a low offset voltage of 1.5 mV maximum which is essential for precision applications. The offset voltage is trimmed with a proprietary trim algorithm to ensure low offset voltage for precision signal processing requirements.

Low Input Bias Current

The TP211x family is a CMOS OPA family and features a very low input bias current in the pA range. The low input bias current allows the amplifiers to be used in applications with high-resistance sources. Care must be taken to minimize the PCB surface leakage. See PCB Surface Leakage for more details.

PCB Surface Leakage

In applications where the low input bias current is critical, the Printed Circuit Board (PCB) surface leakage effects need to be considered. The surface leakage is caused by humidity, dust, or other contamination on the board. Under low humidity conditions, a typical resistance between nearby traces is 10^{12} Ω. A 5-V difference would cause a 5-pA current to flow, which is greater than the input bias current of the TP211x series at +27°C (±1 pA, typical). It is recommended to use the multi-layer PCB layout and route the −IN and +IN signal of the device under the PCB surface.

An effective way to reduce surface leakage is to use a guard ring around the sensitive pins (or traces). The guard ring is biased at the same voltage as the sensitive pin. An example of this type of layout is shown in xref not found for inverting gain applications.

1. For non-inverting gain and unity-gain buffers:
   a. Connect the non-inverting pin (V_{IN}+) to the input with a wire that does not touch the PCB surface.
   b. Connect the guard ring to the inverting input pin (V_{IN}–). This biases the guard ring to the common-mode input voltage.
2. For inverting gain and trans-impedance gain amplifiers (convert current to voltage, such as photo detectors):

a. Connect the guard ring to the non-inverting input pin (V_{IN}+). This biases the guard ring to the same reference voltage as the operational amplifier (e.g., V_{DD} / 2 or ground).
b. Connect the inverting pin (V_{IN}–) to the input with a wire that does not touch the PCB surface.

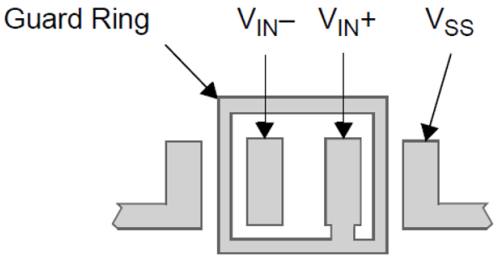


Figure 22. PCB Surface Leakage

Ground Sensing and Rail-to-Rail Output

The TP211x family has excellent output drive capability, delivering an output drive current of over 10 mA. The output stage is a rail-to-rail topology that is capable of swinging to within 10 mV of either rail. Since the inputs can go 300 mV beyond either rail, the operational amplifier can easily perform 'True Ground Sensing'.

The maximum output current is a function of the total supply voltage. As the supply voltage to the amplifier increases, the output current capability also increases. Attention must be paid to keeping the junction temperature of the IC below 150°C when the output is in continuous short-circuit. The output of the amplifier has reverse-biased ESD diodes connected to each supply. The output should not be forced more than 0.5 V beyond either supply, otherwise the current flows through these diodes.

ESD

The TP211x family has reverse-biased ESD protection diodes on all inputs and outputs. The input and output pins cannot be biased more than 300 mV beyond either supply rail.

Driving Large Capacitive Load

The TP211x family is designed to drive large capacitive loads. Refer to Typical Performance Characteristics for Figure 4. As always, a larger load capacitance decreases the overall phase margin in a feedback system where internal frequency compensation is utilized. As the load capacitance increases, the phase margin of the feedback loop decreases, and the closed-loop bandwidth is reduced. This produces the gain peaking in the frequency response, with overshoot and ringing in the output step response. The unity-gain buffer (G = +1 V/V) is the most sensitive to large capacitive loads.

When driving large capacitive loads with the TP211x family (e.g., > 200 pF when G = +1 V/V), a small series resistor at the output (R_{ISO} in Figure 23) improves the phase margin and stability of the feedback loop by making the output load resistive at higher frequencies.

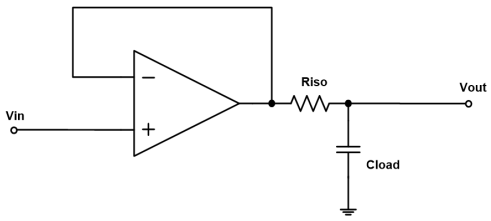


Figure 23. Driving Large Capacitive Load

Power Supply Layout and Bypass

The power supply pin (V_{DD} for single-supply) of the TP211x family should have a local bypass capacitor (i.e., 0.01 μF to 0.1 μF) within 2 mm for high-frequency performance. It can also use a bulk capacitor (i.e., 1 μF or larger) within 100 mm to provide large and slow currents. This bulk capacitor can be shared with other analog parts.

The ground layout improves performance by decreasing the amount of the stray capacitance and noise at the inputs and outputs of the operational amplifier. To decrease the stray capacitance, minimize the PC board lengths and resistor leads, and place external components to the pins as close as possible.

Proper Board Layout

To ensure optimum performance at the PCB level, care must be taken in the design of the board layout. To avoid leakage currents, the surface of the board should be kept clean and free of moisture. The coating of the surface creates a barrier to moisture accumulation and helps reduce the parasitic resistance on the board.

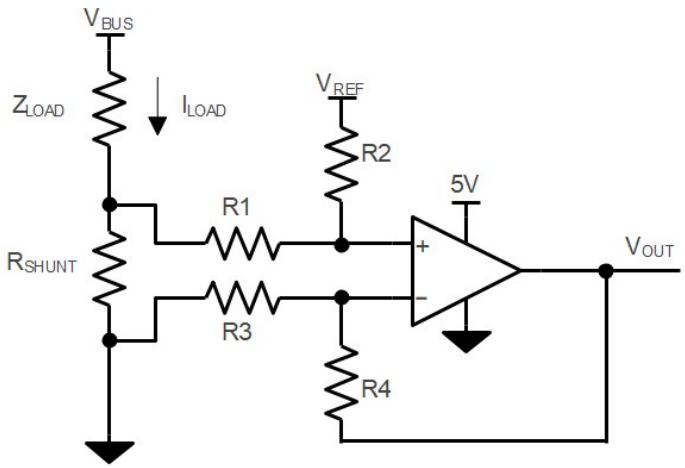
Keeping supply traces short and properly bypassing the power supplies can minimize power supply disturbances due to the output current variation, for example when driving an AC signal into a heavy load. Bypass capacitors should be connected as close as possible to the supply pins of the device. Stray capacitance is a concern for the inputs and outputs of the amplifier. It is recommended that signal traces should be kept at least 5 mm from supply lines to minimize the coupling.

A variation in temperature across the PCB can cause a mismatch in the Seebeck voltages at solder joints and other points where dissimilar metals are in contact, resulting in thermal voltage errors. To minimize these thermocouple effects, orient the resistors, so heat sources can warm both ends equally. Input signal paths should contain matching numbers and types of components, where possible to match the numbers and types of thermocouple junctions. For example, dummy components, such as zero-value resistors, can be used to match real resistors in the opposite input path. Matching components should be in close proximity and oriented in the same manner. Ensure that the leads are of equal length so that the thermal conduction is in equilibrium. Keep heat sources on the PCB as far away from amplifier input circuitry as is practical.

A ground plane is highly recommended. The ground plane reduces the EMI noise and helps maintain a constant temperature across the circuit board.

Typical Application

Figure 24 shows the typical application schematic.

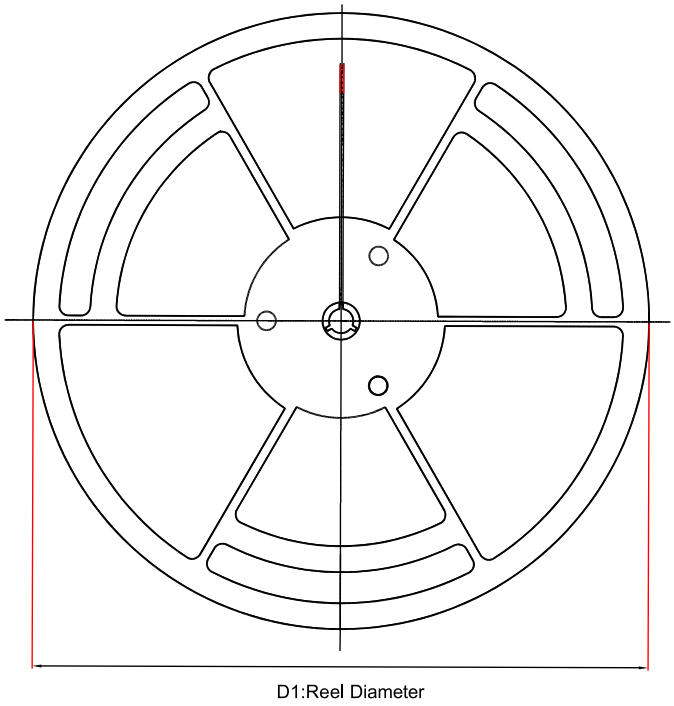


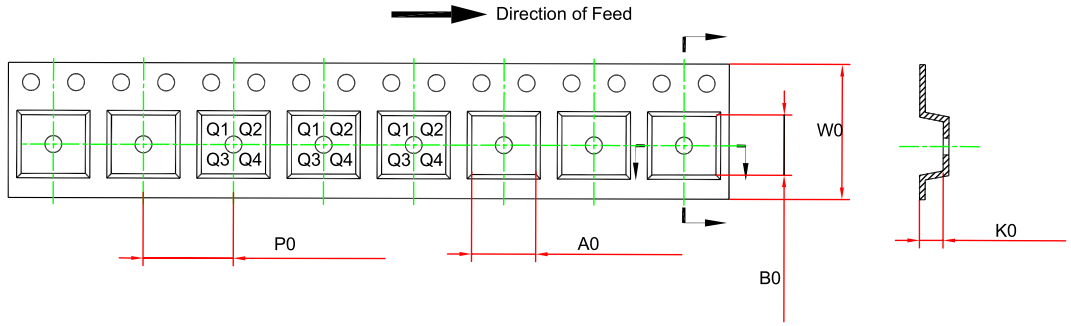
$V_{OUT} = (I_{LOAD} \times R_{SHUNT}) \times (R2 / R1) + V_{REF}$

When R3 = R1, R2 = R4, $R_{SHUNT} << R1$

Figure 24. Typical Application Circuit

Tape and Reel Information





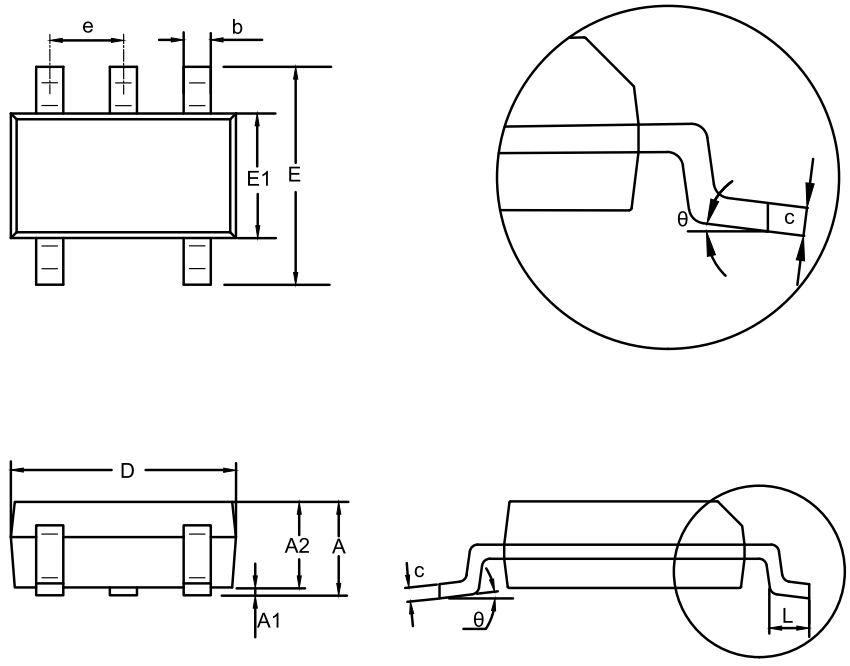
Order Number	Package	D1 (mm)	W1 (mm)	A0 (mm) (1)	B0 (mm) (1)	K0 (mm) (1)	P0 (mm)	W0 (mm)	Pin1 Quadrant
TP2111-CR	SOT353	178	12.1	2.4	2.5	1.2	4	8	Q3
TP2111-TR	SOT23-5	180	12	3.3	3.25	1.4	4	8	Q3
TP2112-SR	SOP8	330	17.6	6.5	5.4	2	8	12	Q1
TP2112-VR	MSOP8	330	17.6	5.3	3.4	1.3	8	12	Q1
TP2114-SR	SOP14	330	21.6	6.5	9.3	2.1	8	16	Q1
TP2114-TR	TSSOP14	330	17.6	6.8	5.5	1.5	8	12	Q1
TP2112-DFGR-S	DFN2X2-8	180.0	12.5	2.2	2.2	0.7	4.0	8.0	Q1

(1) The value is for reference only. Contact the 3PEAK factory for more information.

Package Outline Dimensions

SOT353 (SC70-5)

Package Outline Dimensions SC5(SOT353-5-A)



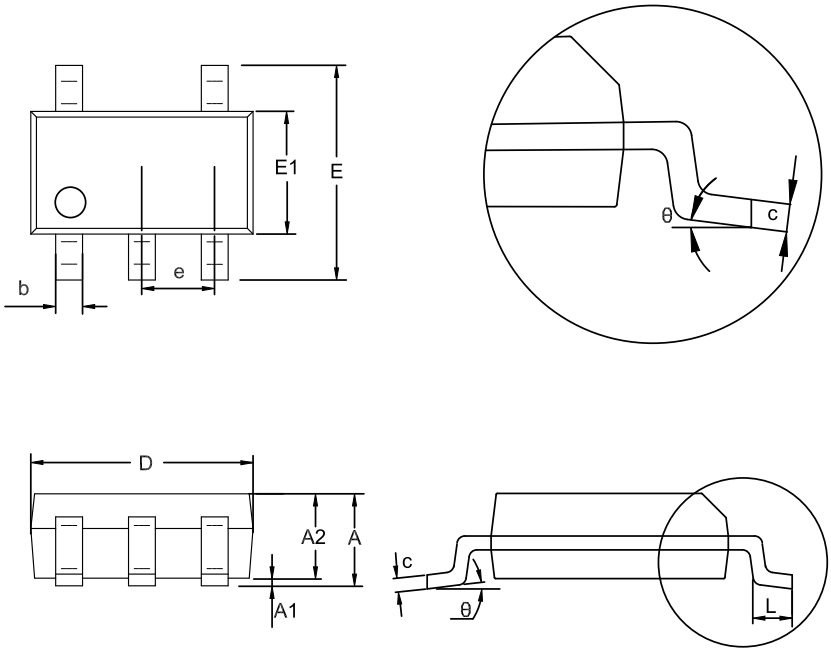
Symbol	Dimensions In Millimeters		Dimensions In Inches	
	MIN	MAX	MIN	MAX
A	0.850	1.100	0.033	0.043
A1	0.000	0.100	0.000	0.004
A2	0.800	1.000	0.031	0.039
b	0.150	0.350	0.006	0.014
c	0.110	0.230	0.004	0.009
D	2.000	2.200	0.079	0.087
E	2.150	2.450	0.085	0.096
E1	1.150	1.350	0.045	0.053
e	0.650 BSC		0.026 BSC	
L	0.260	0.460	0.010	0.018
θ	0	8°	0	8°

NOTES

1. Do not include mold flash or protrusion.
2. This drawing is subject to change without notice.

SOT23-5

Package Outline Dimensions S5T(SOT23-5-A)



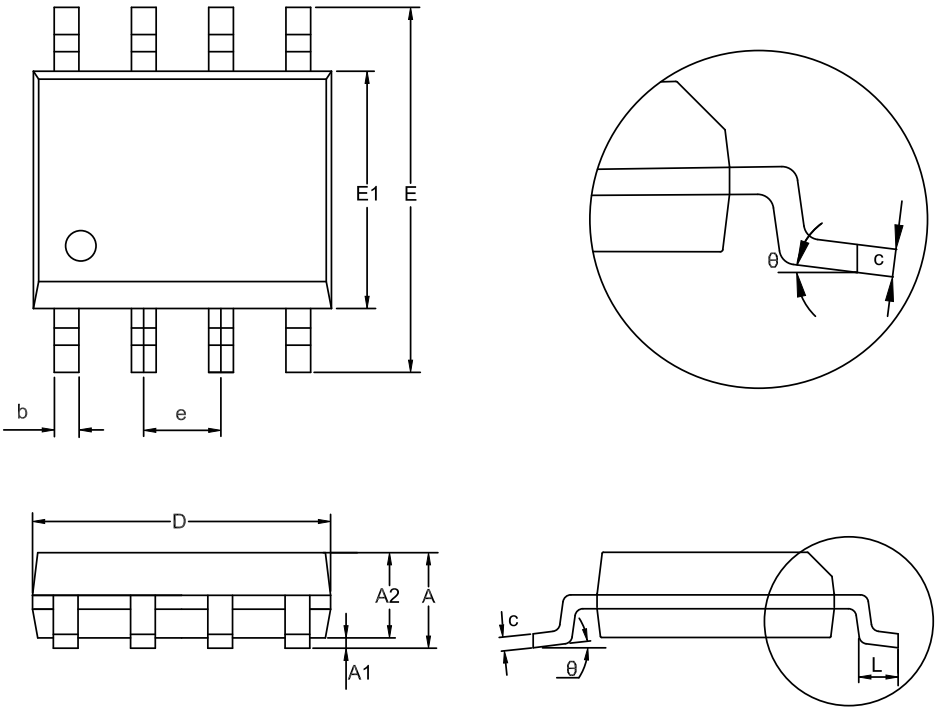
Symbol	Dimensions In Millimeters		Dimensions In Inches	
	MIN	MAX	MIN	MAX
A	1.050	1.250	0.041	0.049
A1	0.000	0.150	0.000	0.006
A2	1.000	1.200	0.039	0.047
b	0.280	0.500	0.011	0.020
c	0.100	0.230	0.004	0.009
D	2.820	3.020	0.111	0.119
E	2.600	3.000	0.102	0.118
E1	1.500	1.720	0.059	0.068
e	0.950 BSC		0.037 BSC	
L	0.300	0.600	0.012	0.024
θ	0	8°	0	8°

NOTES

1. Do not include mold flash or protrusion.
2. This drawing is subject to change without notice.

SOP8

Package Outline Dimensions SO1(SOP-8-A)



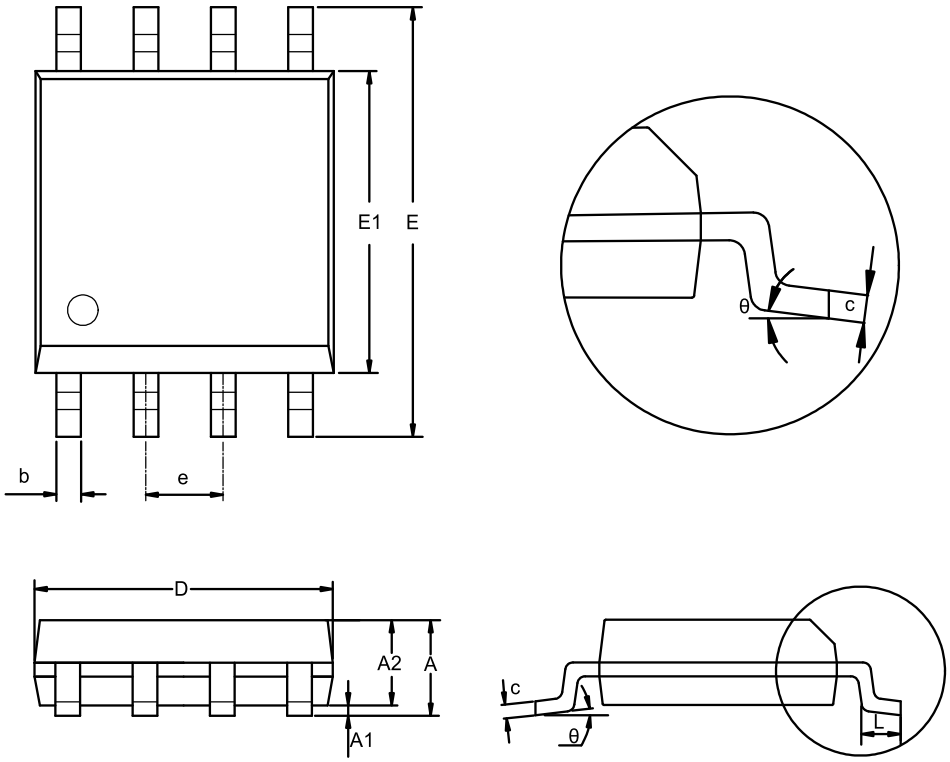
Symbol	Dimensions In Millimeters		Dimensions In Inches	
	MIN	MAX	MIN	MAX
A	1.350	1.750	0.053	0.069
A1	0.050	0.250	0.002	0.010
A2	1.250	1.550	0.049	0.061
b	0.330	0.510	0.013	0.020
c	0.170	0.250	0.007	0.010
D	4.700	5.100	0.185	0.201
E	5.800	6.200	0.228	0.244
E1	3.800	4.000	0.150	0.157
e	1.270 BSC		0.050 BSC	
L	0.400	1.000	0.016	0.039
θ	0	8°	0	8°

NOTES

1. Do not include mold flash or protrusion.
2. This drawing is subject to change without notice.

MSOP8

Package Outline Dimensions VS1(MSOP-8-A)



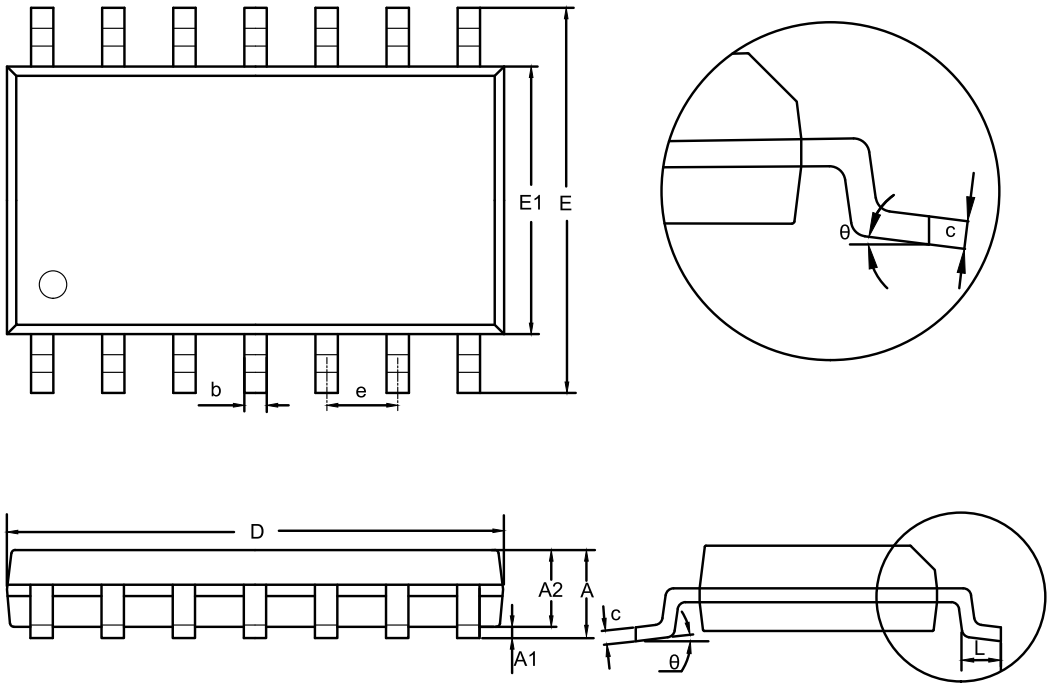
Symbol	Dimensions In Millimeters		Dimensions In Inches	
	MIN	MAX	MIN	MAX
A	0.800	1.100	0.031	0.043
A1	0.020	0.150	0.001	0.006
A2	0.750	0.950	0.030	0.037
b	0.250	0.380	0.010	0.015
c	0.090	0.230	0.004	0.009
D	2.900	3.100	0.114	0.122
E	4.700	5.100	0.185	0.201
E1	2.900	3.100	0.114	0.122
e	0.650 BSC		0.026 BSC	
L	0.400	0.800	0.016	0.031
θ	0	8°	0	8°

NOTES

1. Do not include mold flash or protrusion.
2. This drawing is subject to change without notice.

SOP14

Package Outline Dimensions SO2(SOP-14-A)



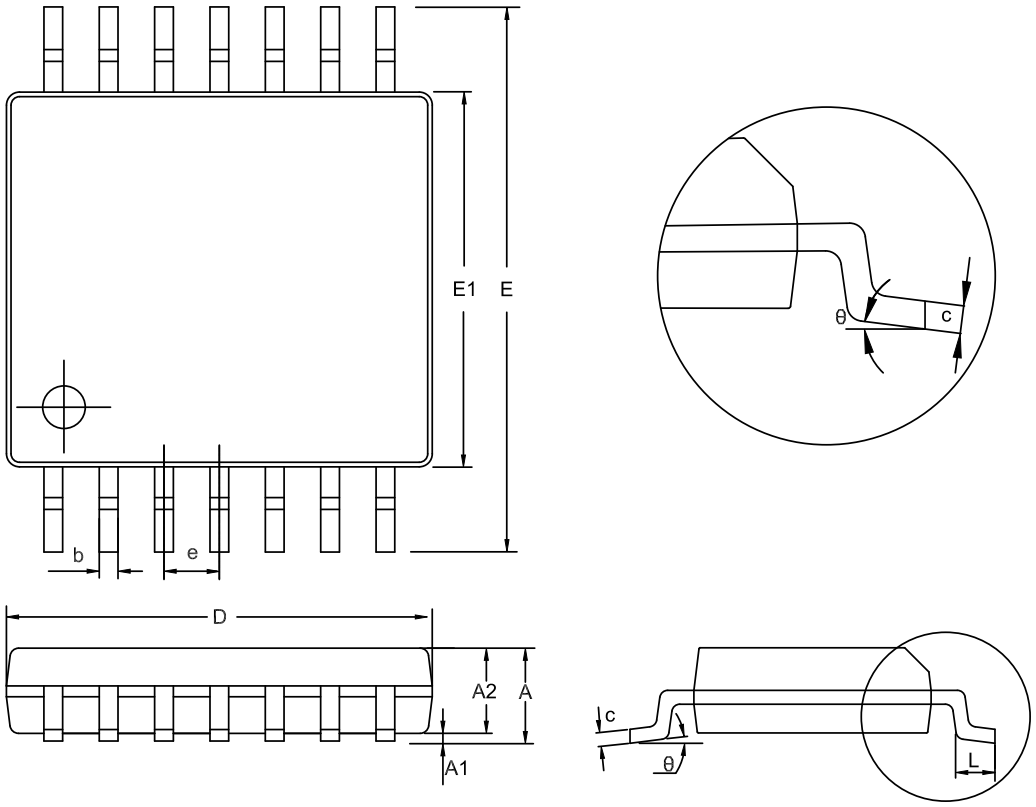
Symbol	Dimensions In Millimeters		Dimensions In Inches	
	MIN	MAX	MIN	MAX
A	1.350	1.750	0.053	0.069
A1	0.050	0.250	0.002	0.010
A2	1.250	1.650	0.049	0.065
b	0.310	0.510	0.012	0.020
c	0.100	0.250	0.004	0.010
D	8.450	8.850	0.333	0.348
E	5.800	6.200	0.228	0.244
E1	3.800	4.000	0.150	0.157
e	1.270 BSC		0.050 BSC	
L	0.400	1.270	0.016	0.050
θ	0	8°	0	8°

NOTES

1. Do not include mold flash or protrusion.
2. This drawing is subject to change without notice.

TSSOP14

Package Outline Dimensions TS2(TSSOP-14-A)



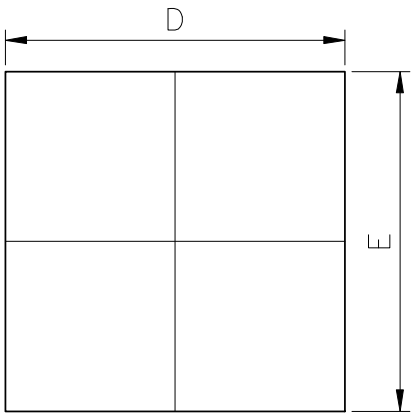
Symbol	Dimensions In Millimeters		Dimensions In Inches	
	MIN	MAX	MIN	MAX
A	0.900	1.200	0.035	0.047
A1	0.050	0.150	0.002	0.006
A2	0.800	1.050	0.031	0.041
b	0.190	0.300	0.007	0.012
c	0.090	0.200	0.004	0.008
D	4.900	5.100	0.193	0.201
E	6.200	6.600	0.244	0.260
E1	4.300	4.500	0.169	0.177
e	0.650 BSC		0.026 BSC	
L	0.450	0.750	0.018	0.030
θ	0	8°	0	8°

NOTES

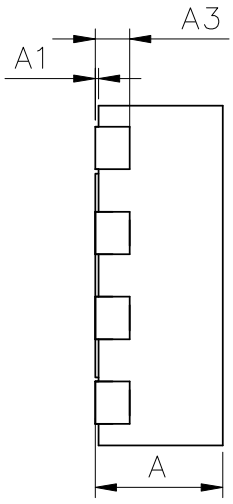
1. Do not include mold flash or protrusion.
2. This drawing is subject to change without notice.

DFN2X2-8

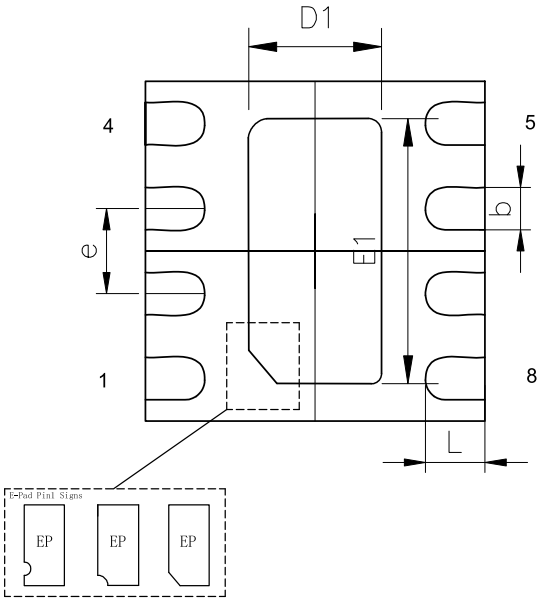
Package Outline Dimensions DFG(DFN2X2-8-E)



Top View



Side View



Bottom View

NOTES

1. Do not include mold flash or protrusion.
2. This drawing is subject to change without notice.
3. The many types of E-pad Pin1 signs may appear in the product.

Symbol	Dimensions In Millimeters		Dimensions In Inches	
	MIN	MAX	MIN	MAX
A	0.500	0.600	0.020	0.024
A1	0.000	0.050	0.000	0.002
b	0.150	0.300	0.006	0.012
A3	0.100	0.200	0.004	0.008
D	1.900	2.100	0.075	0.083
D1	0.800	1.000	0.031	0.039
E	1.900	2.100	0.075	0.083
E1	1.600	1.800	0.063	0.071
e	0.500 BSC		0.020BSC	
L	0.224	0.376	0.009	0.015

Order Information

Order Number	Operating Temperature Range	Package	Marking Information	MSL	Transport Media, Quantity	Eco Plan
TP2111-TR	−40 to 125°C	SOT23-5	B1TYW (1)	3	Tape and Reel, 3000	Green
TP2111-CR	−40 to 125°C	SOT353 (SC70-5)	B1TYW (1)	3	Tape and Reel, 3000	Green
TP2112-SR	−40 to 125°C	SOP8	B12S AAYW (1)	3	Tape and Reel, 4000	Green
TP2112-VR	−40 to 125°C	MSOP8	B12V AAYW (1)	3	Tape and Reel, 3000	Green
TP2114-SR (2)	−40 to 125°C	SOP14	2114 AAYW (1)	3	Tape and Reel, 2500	Green
TP2114-TR (2)	−40 to 125°C	TSSOP14	2114 AAYW (1)	3	Tape and Reel, 3000	Green
TP2112-DFGR-S	−40 to 125°C	DFN2X2-8	A58	3	Tape and Reel, 3000	Green

(1) "AA" identifies the manufacturing site. "YW" is the date code which means the manufacturing year and week as follows.
(2) For future products, contact the 3PEAK factory for more information and samples.

Green: 3PEAK defines "Green" to mean RoHS compatible and free of halogen substances.

The calendar year and the workweek coding scheme is as follows:

Year	Code	Year	Code
2010	A	2023	N
2011	B	2024	O
2012	C	2025	P
2013	D	2026	Q
2014	E	2027	R
2015	F	2028	S
2016	G	2029	T
2017	H	2030	U
2018	I	2031	V
2019	J	2032	W
2020	K	2033	X
2021	L	2034	Y
2022	M	2035	Z

Workweek	Code	Workweek	Code	Workweek	Code	Workweek	Code	Workweek	Code
1	1	14	E	27	R	40	e	53	r
2	2	15	F	28	S	41	f		
3	3	16	G	29	T	42	g		
4	4	17	H	30	U	43	h		
5	5	18	I	31	V	44	i		
6	6	19	J	32	W	45	j		
7	7	20	K	33	X	46	k		
8	8	21	L	34	Y	47	l		
9	9	22	M	35	Z	48	m		
10	A	23	N	36	a	49	n		
11	B	24	O	37	b	50	o		
12	C	25	P	38	c	51	p		
13	D	26	Q	39	d	52	q		

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