极景微半导体

12 Output Ultra-Low Additive Jitter LVDS Buffer

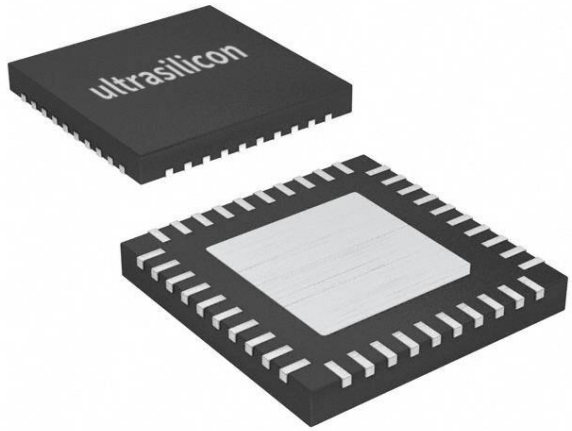
US5D1212D
Datasheet

Description

The US5D1212D is a 2-GHz,12-output differential high-performance clock fanout buffer.

The US5D1212D clock buffer distributes two selectable clock inputs (IN0 and IN1) to 12 pairs of differential LVDS clock outputs (Q0 through Q11) with minimum skew for clock distribution. The US5D1212D can accept two clock sources into an input multiplexer. The inputs can either be LVDS,LVPECL,HCSL or LVCMOS. It has a maximum clock frequency up to 2-GHz.

The device is designed for a signal fanout of high-frequency, low phase-noise clock and data signal. It is designed to operate from a 2.5V/3.3V core power supply, and either a 2.5V/3.3V output operating supply.



Features

- 2:12 Differential Buffer
- Universal Inputs can Accept LVPECL,LVDS，HCSL and LVCMOS
- Eight LVDS output
- Maximum Output Frequency LVDS: 2-GHz
- Maximum Propagation Delay: 0.5ns(typical)
- Output skew: 30 ps (Maximum)
- Additive RMS phase jitter 3.3V@ 156.25MHz: 63 fs RMS (12kHz - 20MHz)
- Supply voltage mode VDD: 2.5V±5%,3.3V±5%
- Industrial Temperature Range:-40°C to 85°C
- Available in QFN-40(6mm x 6mm) package

Applications

- Clock distribution and level translation for ADCs, DACs, Multi-Gigabit Elthernet, XAUI, Fibre channel, SATA/SAS, SONET/SDH,CPRI, High-Frequency Backplanes
- Switches, Routers, Line Cards, Timing Cards
- Servers, Computing, PCI Express(PCIe 3.0,4.0,5.0)
- Remote Radio Units and Baseband Units

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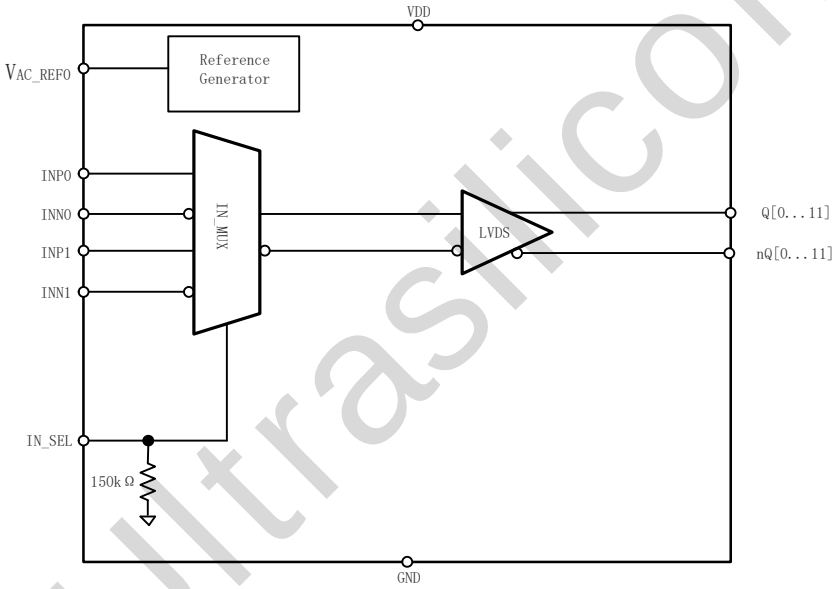
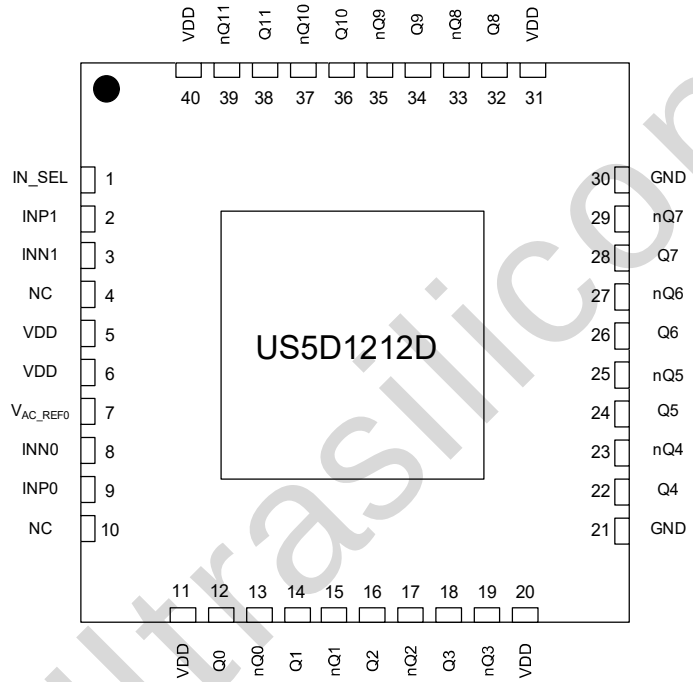
Block Diagram



Pin Assignment for QFN-40 Package



Pin Description and Pin Characteristic Tables

Table 1: Pin Descriptions

Number	Name	Type	Description
1	IN_SEL	Input	Input clock selection. Input with 150kΩ pulldown.
2	INP1	Input	Differential input pair or single ended input.
3	INN1	Input	Differential input pair .
4	NC	NC	No connect.
5	VDD	Power	Power supply for Core, 3.3V or 2.5V.
6	VDD	Power	Power supply for Core, 3.3V or 2.5V.
7	V_{AC_REF0}	Output	Bias voltage output for capacitive coupled inputs. If used, it is recommended to use VAC_REF0 Output a 0.1μF to GND on this pin.
8	INN0	Input	Differential input pair .
9	INP0	Input	Differential input pair or single ended input.
10	NC	NC	No connect.
11	VDD	Power	Power supply for Core, 3.3V or 2.5V.
12	Q0	Output	Differential LVDS output pair.
13	nQ0	Output	Differential LVDS output pair.
14	Q1	Output	Differential LVDS output pair.
15	nQ1	Output	Differential LVDS output pair.
16	Q2	Output	Differential LVDS output pair.
17	nQ2	Output	Differential LVDS output pair.
18	Q3	Output	Differential LVDS output pair.
19	nQ3	Output	Differential LVDS output pair.
20	VDD	Power	Power supply for Core, 3.3V or 2.5V.
21	GND	Power	Ground.
22	Q4	Output	Differential LVDS output pair.
23	nQ4	Output	Differential LVDS output pair.
24	Q5	Output	Differential LVDS output pair.
25	nQ5	Output	Differential LVDS output pair.
26	Q6	Output	Differential LVDS output pair.
27	nQ6	Output	Differential LVDS output pair.
28	Q7	Output	Differential LVDS output pair.
29	nQ7	Output	Differential LVDS output pair.
30	GND	Power	Ground.
31	VDD	Power	Power supply for Core, 3.3V or 2.5V.
32	Q8	Output	Differential LVDS output pair.
33	nQ8	Output	Differential LVDS output pair.
34	Q9	Output	Differential LVDS output pair.

35	nQ9	Output	Differential LVDS output pair.
36	Q10	Output	Differential LVDS output pair.
37	nQ10	Output	Differential LVDS output pair.
38	Q11	Output	Differential LVDS output pair.
39	nQ11	Output	Differential LVDS output pair.
40	VDD	Power	Power supply for Core, 3.3V or 2.5V.

Table 2: Input Selection Table

IN_SEL	ACTIVE CLOCK INPUT
0	INP0,INN0
1	INP1,INN1

Absolute Maximum Ratings

Exposure to absolute maximum rating conditions for extended periods may affect product reliability. Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These ratings are stress specifications only. Functional operation of the product at these conditions or any conditions beyond those listed in the *DC Characteristics or AC Characteristics* is not implied.

Item	Rating
V_{DD}	4.6V
V_{IN}	-0.5V to V_{DD} + 0.5V
T_J :Junction Temperature	125°C
T_{STG} :Storage Temperature	-65°C to 150°C

ESD Ratings

		Max	Unit
V(ESD) Electrostatic discharge	Human-body model (HBM), ANSI/ESDA/JEDEC JS-001-2017	±2500	V
	Machine model (MM), JEDEC Std. JESD22-A115-C	±250	
	Charged-device model (CDM), ANSI/ESDA/JEDEC JS-002-2018	±750	

Latch up

		Max	Unit
Latch up	I-test, JEDEC STD JESD78E	±200	mA
	V-test, JEDEC STD JESD78E	4.6	V

Recommended Operating Conditions

Symbol	Parameter	Min	Typ	Max	Unit
T_A	Ambient air temperature	-40		85	°C
T_J	Junction temperature			125	°C
V_{DD}	Power supply for Core and input Buffer blocks	2.5-5% 3.3-5%	2.5 3.3	2.5+5% 3.3+5%	V

Electrical Characteristics

VDD = 3.135 V to 3.6 V and TA = –40°C to 85°C (unless otherwise noted).

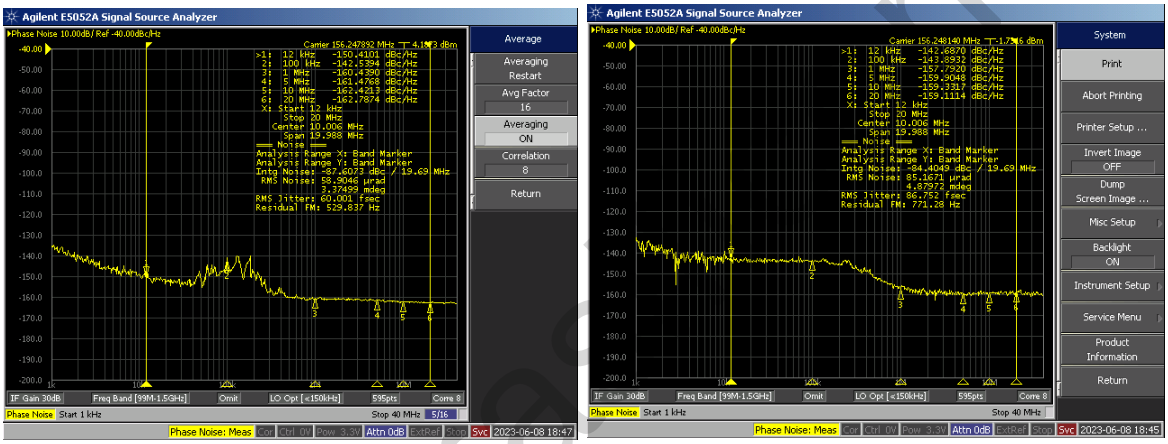
Parameter		Test Conditions	Min	Typ	Max	Unit
IDD	Power supply current	VDD=3.3V, F_{IN}=156.25MHz, All outputs active	-	210	-	mA
		VDD=2.5V, F_{IN}=156.25MHz, All outputs active	-	200	-	mA
R_{pull}(IN_SEL)	Input ulldown resistor			150		kΩ
LVCMOS INPUT						
F_{IN}	Input frequency	VDD=3.3V	0.1		250	MHz
Vth	input threshold voltage	External threshold voltage applied to complementary input	1.1		1.5	V
VIH	Input high voltage		0.7*VDD		VDD	V
VIL	Input low voltage		0		0.3*VDD	V
IIH	Input high current	VDD = 3.6V, VIH = 3.6 V			100	μA
IIL	Input low current	VDD = 3.6V, VIL = 0 V			-100	μA
C_{IN}	Input capacitance			2.5		pF

Electrical Characteristics(continued)

VDD = 3.135 V to 3.6 V and TA = –40°C to 85°C (unless otherwise noted).

Parameter		Test Conditions	Min	Typ	Max	Unit
DIFFERENTIAL INPUT						
F_{IN}	Input frequency	VDD=3.3V	0.1		2000	MHz
$V_{IN,DIFF}$	Differential input voltage Peak-to-peak	V_{ICM}=1.25V	0.3		1.6	VPP
V_{ICM}	Input common mode voltage	$V_{IN,DIFF,PP}$ > 0.4 V	1		VDD-0.3	V
IIH	Input high current	VDD = 3.6V, VIH = 3.6 V			100	μA
IIL	Input low current	VDD = 3.6V, VIL = 0 V			-100	μA
C_{IN}	Input capacitance			2.5		pF
LVDS OUTPUT						
VOD	Differential output voltage magnitude	$V_{IN,DIFF,PP}$ = 0.3 V,RL = 100 Ω	250		450	mV
ΔVOD	Change in differential output voltage magnitude	$V_{IN,DIFF,PP}$ = 0.3 V,RL = 100 Ω	-15		15	mV
VOC(ss)	Steady-state common mode output voltage	$V_{IN,DIFF,PP}$ = 0.3 V,RL = 100 Ω	1.1		1.375	V
ΔVOC(ss)	Steady-state common mode output voltage	$V_{IN,DIFF,PP}$ = 0.3 V,RL = 100 Ω	-15		15	mV
Vring	Output overshoot and undershoot	Percentage of output amplitude VOD			10%	
t_{PD}	Propagation delay	3.3V@156.25MHz		0.5	1.5	ns
$t_{SK,pp}$	Part-to-part skew				600	ps
$t_{SK,O}$	Output skew			10	30	ps
$t_{SK,P}$	Pulse skew	50% duty cycle input,crossingpoint-to-crossing-point distortion	-50		50	ps
t_{RJIT}	Random additive jitter	50% duty cycle input, 12 kHz to 20 MHz,VDD=3.3V@156.25MHz		64	100	fs
t_R/t_F	Output rise time,tR	20% to 80%		200	300	ps
	Output fall time,tF	20% to 80%		200	300	ps
VAC_REF CHARACTERISTICS						
V_{AC_REF}	Reference output voltage	VDD=2.5V	1.1	1.25	1.35	V

PHASE JITTER



(a)Jitter_Source (b)3V3_156M25_LVDS

Figure 1 .RMS_Jitter_3V3=Sqrt(87²-60²)=64fs

The additive phase jitter for this device was measured using the Low jitter SPXO(156.25MHz) as an input source with and Agilent E5052A phase noise analyzer. (VDD=3.3V)

Timing Diagrams

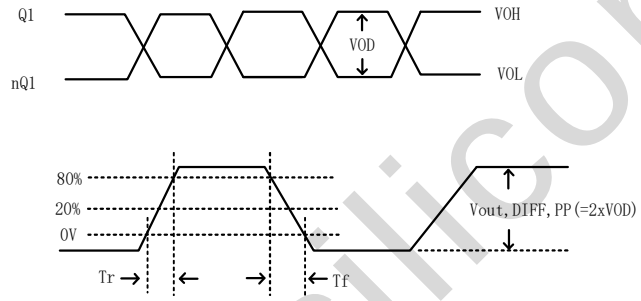
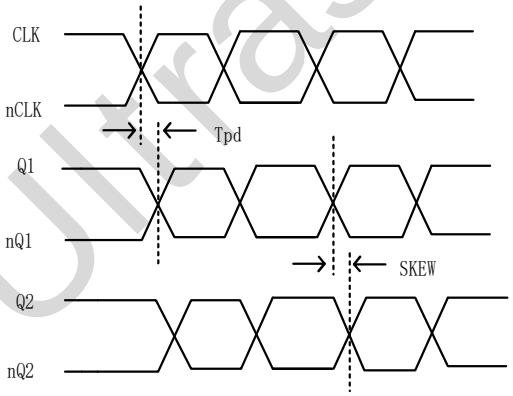


Figure 2.output voltage and rise/fall time



(1) Output skew is calculated as the greater of the following: As the difference between the fastest and the slowest tPLHn(n = 0, 1, 2....7), or as the difference between the fastest and the slowest tPHLn (n = 0, 1, 2....7).
(2) Part-to-part skew is calculated as the greater of the following: As the difference between the fastest and the slowest tPLHn (n = 0, 1, 2....7) across multiple devices, or the difference between the fastest and the slowest tPHLn (n = 0, 1,2....7) across multiple devices

Figure 3.output and skew

Applications Information

Wiring the Differential Input to Accept Single-Ended Levels

For the single-ended input LVCMOS signal, Rs and R0 in the driver form a 50Ω impedance match, and the direct-isolated capacitor C3 avoids the influence of the common-mode level between the input and output, and then drives the receiver through the voltage divider and the common-mode level to VDD/2.

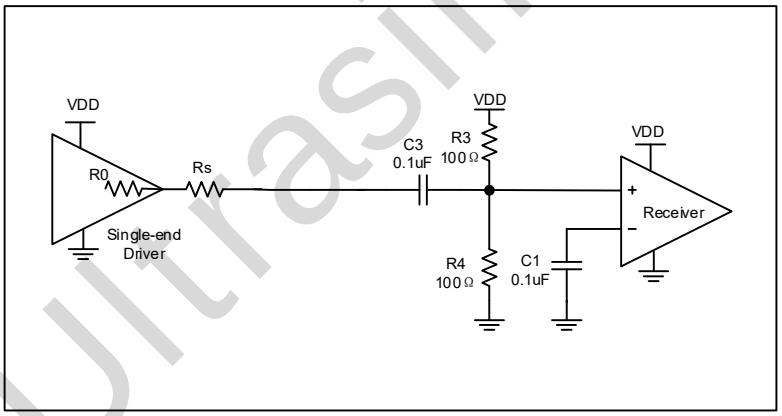
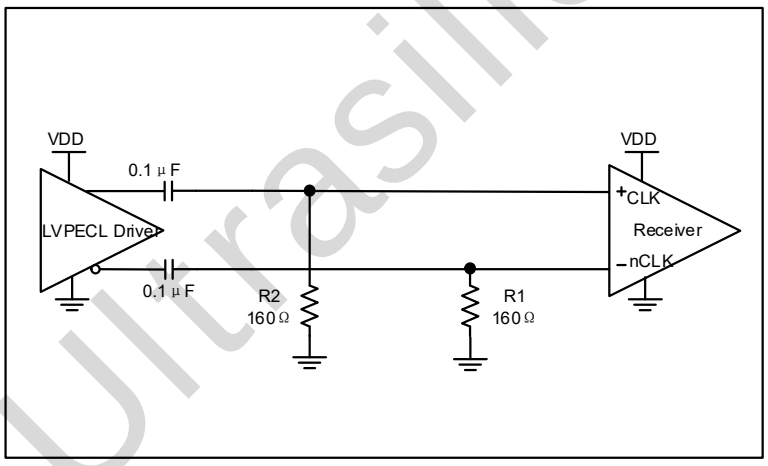
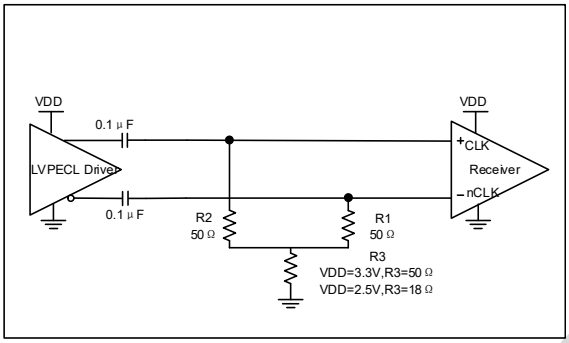


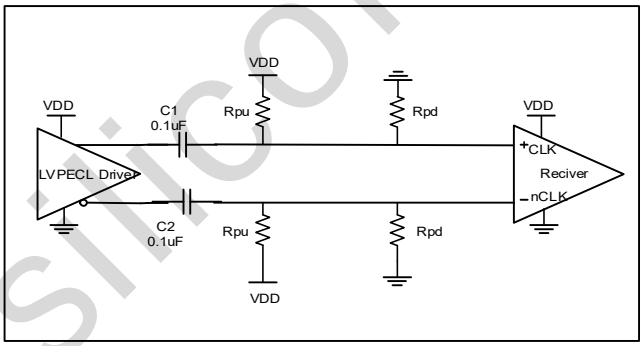
Figure4.Single-ended input

Input connection circuit

The CLK /nCLK accepts LVDS, LVPECL, HCSL and other differential signals. Both differential signals must meet the VPP and VCMR input requirements. Figure5 to Figure8 show interface examples for the CLK/nCLK input driven by the most common driver types. The input interfaces suggested here are examples only. Please consult with the vendor of the driver component to confirm the driver termination requirements.

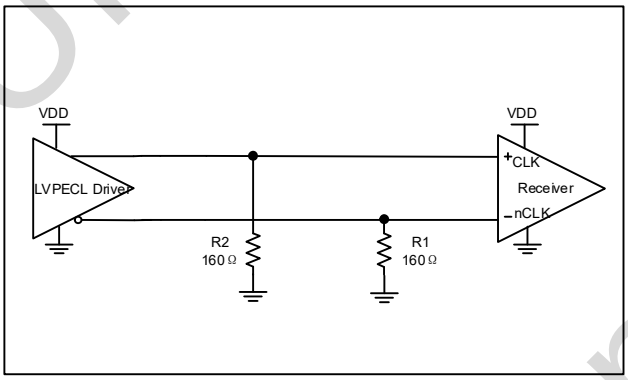


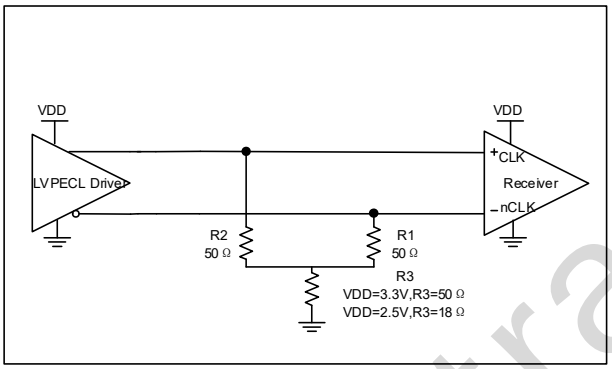


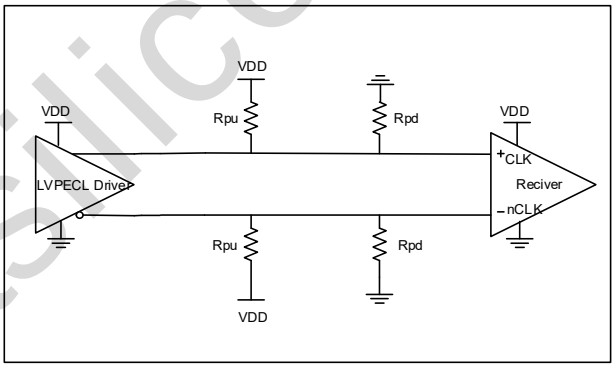


VDD	Rpu	Rpd
3.3V	120 Ω	82 Ω
2.5V	250 Ω	62.5 Ω

Figure5.LVPECL Driver(AC)

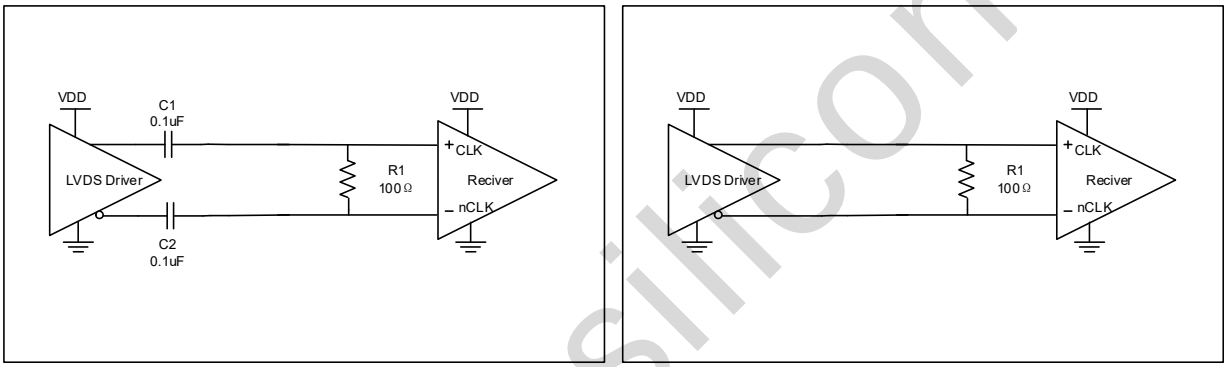






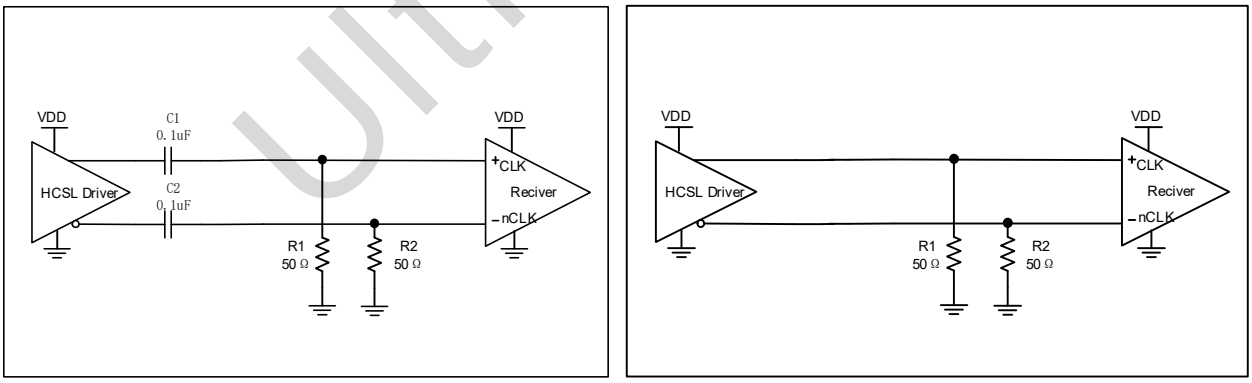
VDD	Rpu	Rpd
3.3V	120 Ω	82 Ω
2.5V	250 Ω	62.5 Ω

Figure6.LVPECL Driver(DC)



a)AC coupling **b)DC coupling**

Figure7.LVDS Driver



a)AC coupling **b)DC coupling**

Figure8.HCSL Driver

Output connection circuit

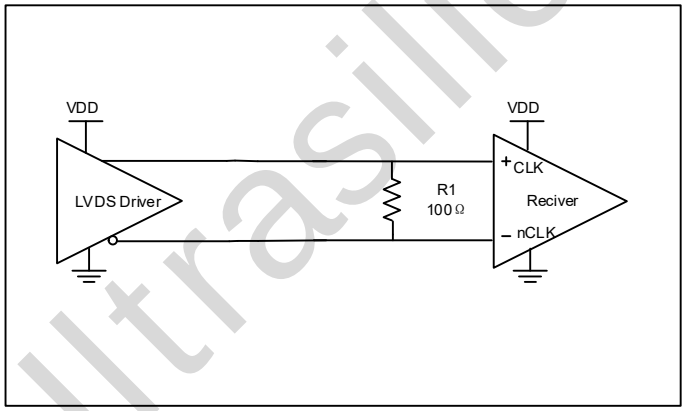
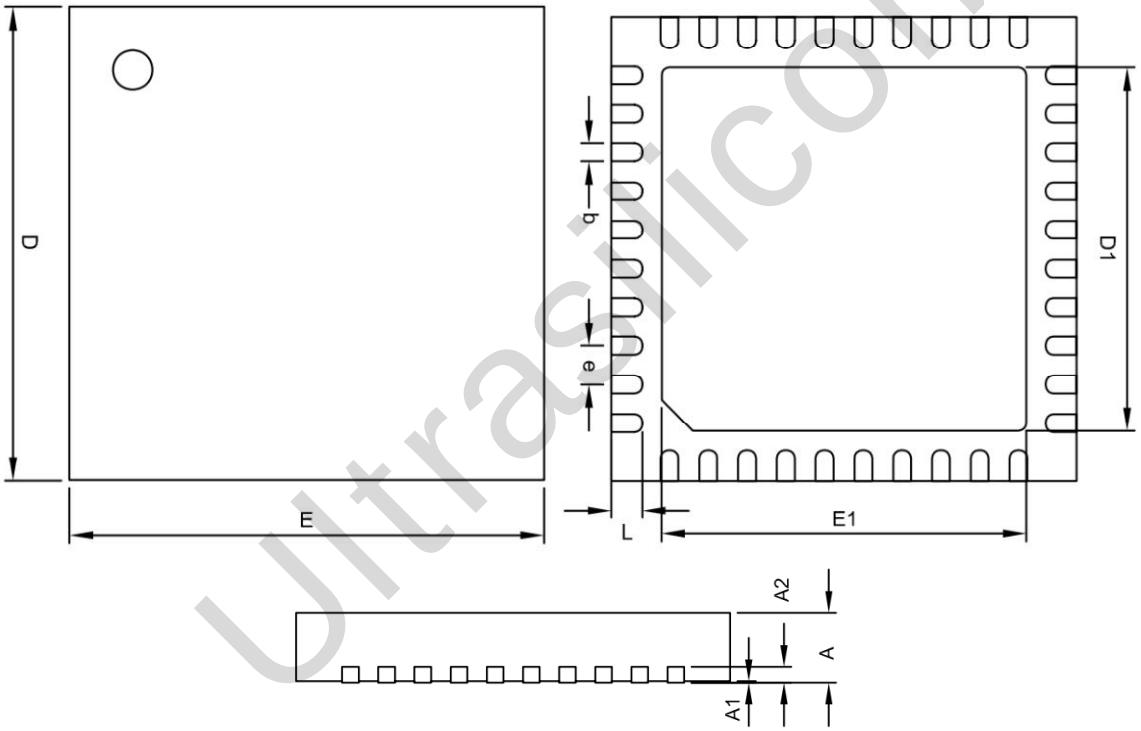


Figure9.LVDS Driver

PACKAGE DIMENSIONS(QFN-40)



Symble	DIMENSION IN MM			DIMENSION IN INCH		
	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.
A	0.80	0.90	1.00	0.0315	0.0354	0.0394
A1	0.00	- - -	0.05	0.0000	- - -	0.0020
A2	0.19	0.20	0.21	0.0075	0.0079	0.0083
D	5.95	6.00	6.05	0.2343	0.2362	0.2382
E	5.95	6.00	6.05	0.2343	0.2362	0.2382
D1	4.55	4.65	4.75	0.1791	0.1831	0.1870
E1	4.55	4.65	4.75	0.1791	0.1831	0.1870
b	0.18	0.23	0.28	0.0071	0.0091	0.0110
e	0.50 BSC			0.0197 BSC		
L	0.35	0.40	0.45	0.0138	0.0157	0.0177

Note：

1. Dimensioning and tolerancing conform to ASME Y14.5-2009.
2. All dimensions are in millimeters.
3. N is the total number of terminals.
4. The location of the marked terminal #1 identifier is within the hatched area.
5. ND and NE refer to the number of terminals on D and E side respectively.
6. Dimension b applies to the metallized terminal and is measured between 0.15mm and 0.30mm from the terminal tip.If the terminal has a radius on the other end of it, dimension b should not be measured in that radius area.
7. Colanarity applies to the terminals and all other bottom surface metallization.

Reflow profile

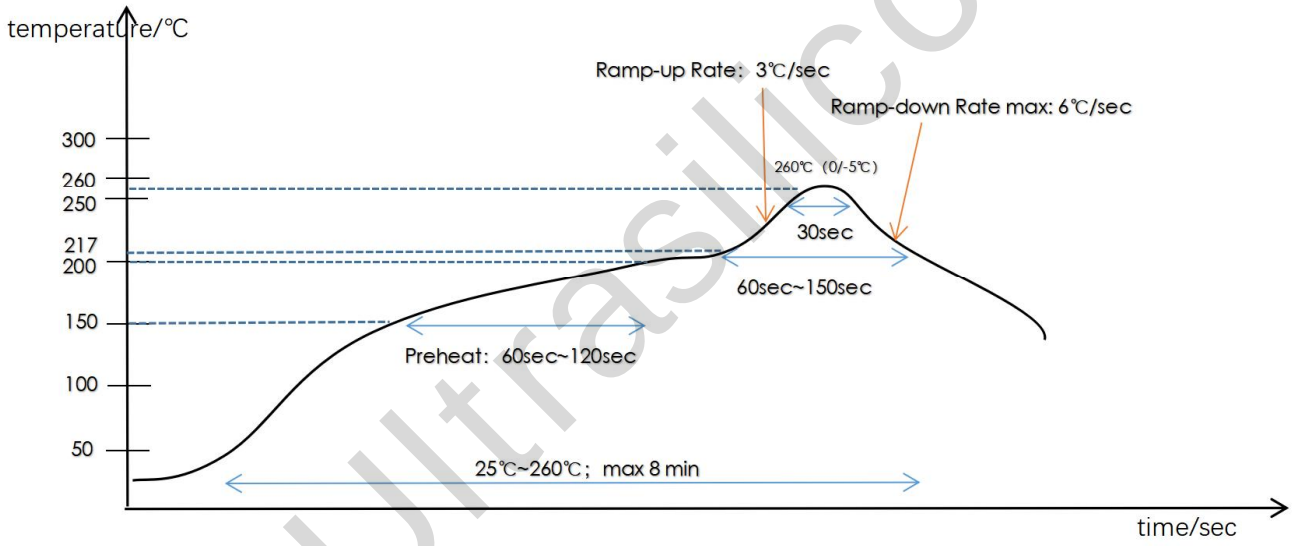


Figure10: Recommended Temperature(PB-Free)

Reflow Condition	Convection or IR/Convection
Average ramp-up rate(217℃ to Peak)	3℃/second max
Preheat temperature 175(±25)℃	60~120 seconds
Temperature maintained above 217℃	60~150 seconds
Time within 5℃ of actual peak temperature	30 seconds
Peak temperature range	260 +0/-5℃
Ramp-down rate	6℃/second max
Time 25℃ to peak temperature	8 minutes max
Maximum number of reflow cycles	≤3

Revision History

Date	Description of Change	Revision
2023.5.19	First Draft.	1.0
2023.08.01	Parameter value update.	1.5
2025.7.10	Update the current Characteristics.	2.0